LOW VOLTAGE, ENERGY EFFICIENT ANALOG CIRCUITS FOR LOW POWER APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by

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DECLARATION

I hereby ***declare*** that the Research Thesis entitled **LOW VOLTAGE, ENERGY EFFICIENT ANALOG CIRCUITS FOR LOW POWER APPLICATIONS** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me.*** The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to certify that the Research Thesis entitled **LOW VOLTAGE, ENERGY EFFICIENT ANALOG CIRCUITS FOR LOW POWER APPLICATIONS** submitted by **MUHAMMED MANSOOR C. B.** (Register Number: 177005EC007) as the record of the research work carried out by him, is accepted as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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Dedicated to

My beloved parents

Abstract

This thesis presents low voltage, compact and energy efficient linear/non-linear analog circuits for low power applications. Single branch and log domain filters, translinear RMS-DC converter and PTAT current reference have been explored. UMC 65 nm/UMC 180 nm CMOS technologies are used to design these circuits and simulations are carried out in Cadence Virtuoso tool.

Initial part of the thesis outlines compact, single branch and log domain filters. A novel, compact and energy-efficient biquad which is derived from a folded single branch transistorised g_m-C structure is proposed. The biquad has a small number of active devices stacked between V_{DD} and GND rails and hence can be used satisfactorily in a low-voltage environment. The filter also inherits the benefits of folding in the circuit which makes the tuning of the filter easier and power independent. A fourth-order low pass filter is used as a vehicle to illustrate the performance of the proposed biquad. The fully differential version of the filter operates with a supply voltage of 0.6 V, is biased with a current of 100 nA, has a -3 dB bandwidth of 15 kHz and shows a dynamic range as high as 61 dB.

A first order low pass filter employing the log-domain technique is also proposed. The filter design is based on the dynamic translinear principle which exploits the non-linear current-voltage relationship of MOSFETs operating in sub-threshold region. The core of the filter is a second order translinear loop. The filter consumes a power of 55 nW from a 0.9 V supply voltage. The cut-off frequency of the filter is 1 kHz for a bias current of 5 nA. The filter has a dynamic range of 56 dB and a FoM of 0.069 pJ.

This thesis also presents a novel current-mode true RMS-DC converter based on the dynamic translinear principle. The converter is designed using a third-order translinear loop, resulting in a very compact and simple circuit. The proposed circuit operates with 1 V power supply, has only 14 transistors and performs satisfactorily over a wide input current range of 300 nA - 950 nA and for a frequency range of 600 Hz - 650 kHz for a capacitance of 10 nF. The frequency range of operation can be tuned by varying the external off-chip capacitor and the bias current. The circuit

consumes 20 nW static power, 1.6 μW maximum dynamic power and offers the lowest FoM among the other RMS-DC converter circuits presented in the literature.

This work also proposes a low voltage, low power, fast settling switched capacitor based Proportional to Absolute Temperature (PTAT) current reference circuit. Unlike in a conventional resistor based PTAT current source, the proposed circuit saves a significant amount of silicon area on chip and hence the circuit becomes less susceptible to process variations. It creates a reference current of 1 nA from a 0.5 V power supply at room temperature ($27°C$). It has PTAT characteristics in the temperatures from $-10°C$ to $80°C$. The circuit draws a very low power of 1.5 nW and exhibits a good supply voltage sensitivity of 3.2 %/V. A startup circuit connected to the PTAT source improves the transient response by reducing the settling time.

A low power low frequency active-RC filter for ECG detection is also presented. A folded cascode Operational Transconductance Amplifier (OTA) with transistors operating in sub-threshold region at 1.2 V supply voltage is designed which consumes a power of 30 nW. A second order LPF with a cut-off frequency of 50 Hz is built with the designed OTA. To achieve this low bandwidth, current steering technique is used instead of traditional method of using large resistor and capacitor values and hence the design is area efficient. The filter consumes a power of 80 nW, has a dynamic range of 49 dB and shows a FoM of 0.4 pJ.

Keywords: Low voltage; Low power; Single branch; Sub-threshold region; Translinear loop; Dynamic translinear principle; RMS-DC; Log domain filter; PTAT current; Active-RC; Time constant enhancement.

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Abbreviations

G_m-C	Transconductor-Capacitor
Op-amp	Operational amplifier
OTA	Operational transconductance amplifier
CT	Continuous time
SC	Switched capacitor
SoC	System-on-chip
IC	Integrated circuit
EOG	Electrooculogram
EMG	Electromyogram
EEG	Electroencephalogram
ECG	Electrocardiogram
UMC	United Microelectronics Corporation
MOSFET	Metal oxide semiconductor field effect transistor
CMOS	Complementary metal oxide semiconductor
NMOS	N-Channel metal oxide semiconductor
PMOS	P-Channel metal oxide semiconductor
LPF	Low-pass filter
BPF	Band-pass filter
HPF	High-pass filter
SF	Source follower
VF	Voltage follower
UGB	Unity gain bandwidth
IRN	Input referred noise
THD	Total harmonic distortion
HD_2	Second harmonic distortion
HD_3	Third harmonic distortion
DR	Dynamic range
RMS	Root Mean square
FoM	Figure of merit
PVT	Process, voltage and temperature
CP	Compression point
IIP_3	Third order input intercept point
$IMFDR_3$	Third order intermodulation free dynamic range
PSD	Power spectral density

Notations

L	Channel length of the MOSFET
W	Channel width of the MOSFET
C_{ox}	Gate oxide capacitance per unit area
C	Capacitor
R	Resistor
V_{DD}	Supply voltage
GND	Ground
V_{DS}	Drain-source voltage of the MOSFET
V_{BS}	Bulk-source voltage of the MOSFET
V_{GS}	Gate-source voltage of the MOSFET
V_{th}	Threshold voltage of the MOSFET
q	Electronic charge
k	Boltzmann constant
T	Absolute temperature
V_T	Voltage equivalent of temperature or thermal voltage
τ	Time constant
f_c	Cut-off frequency
f_o	Unity gain frequency
f_p	Pole frequency
f_{-3dB}	-3 dB cut-off frequency
γ	MOSFET channel thermal noise coefficient
δ	MOSFET gate induced thermal noise coefficient
g_{ds}	Drain to source conductance
g_m	Gate transconductance
η	Sub-threshold slope factor

Chapter 1

INTRODUCTION

1.1 Analog IC design in low power applications

The use of portable, wearable and implantable devices among biomedical/consumer electronics has soared in recent years. Starting from a smart wristwatch to a pacemaker, this trend has impelled the enhancement of the performance of integrated circuits under very low power. Such systems also require small size and low noise (Harrison *et al.* 2006, Li *et al.* 2010, Wise *et al.* 2008). A typical SoC (System on Chip) has both digital and analog circuits coexisting together. Reduction in supply voltage largely reduces the power consumption of digital circuits since their dynamic power is directly related to the square of the supply voltage. However, the reduction in supply voltage adversely affects the performance of analog circuits on the chip. As supply voltage falls, the system's dynamic range, power supply rejection (PSR), noise immunity and other characteristics deteriorate, which is undesirable (Kinget *et al.* 2005). Moreover, nanoscale technologies have significant fluctuations in process parameters. So a classical design approach may be inadequate in designing ultra-low power analog circuits.

An example of low-voltage low-power system is a biological data acquisition/detection system, especially wearable or portable ones. A typical data acquisition system for biological signals is shown in Figure 1.1 (Solís-Bustos *et al.* 2000). The transducer converts biological signal into equivalent electrical signal. The pre-amplifier amplifies the signal above the noise floor of the filter such that the signal becomes less susceptible to noise. A continuous time (CT) filter selects the desired frequency band and rejects out-of-band interferences and noise. Further signal processing involves A/D

conversion, digital signal processing, storage and/or display.

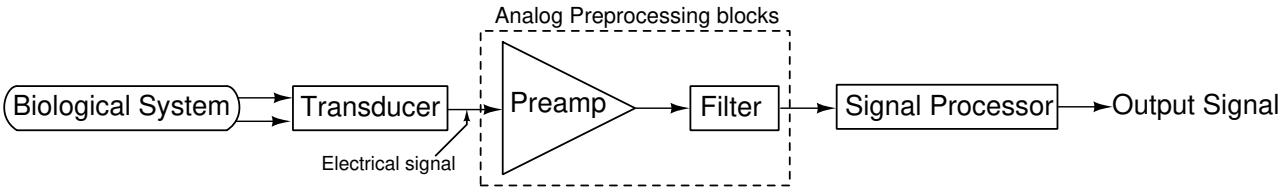


Figure 1.1: A general purpose biological data acquisition system

The focus of the research will be on developing low-power and energy-efficient analog circuits, such as continuous-time filters and other non-linear circuits like RMS-DC converter, that can be integrated into such SoC systems to meet the demands for low power consumption. The main challenges in the design of such analog circuits are as follows.

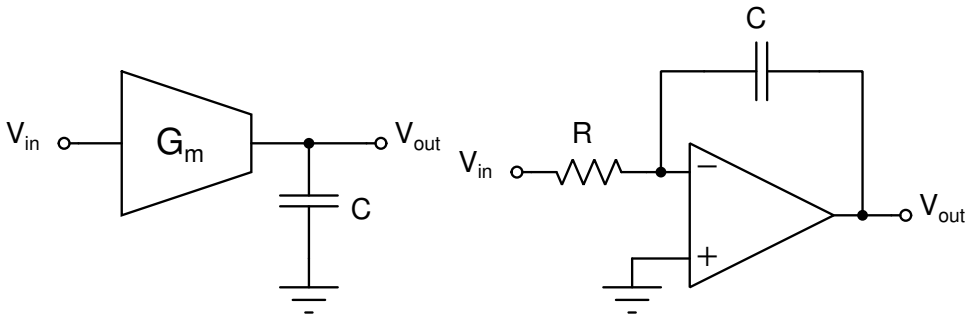
- The technology scaling necessitates integrated circuits (IC) to operate with low voltage to reduce the chip power density and to enhance reliability. With very low supply voltages, the performance of standard analog designs is typically impaired. The signals end up having restricted voltage headroom, which eventually gives a bottleneck on the linearity of the circuit.

- To prolong the battery life of implantable/portable medical devices and to comply with the safety requirements of the human body, the power consumption of the system should be as low as possible. To reduce the power consumption, MOS transistors in a circuit are operated in weak-inversion or sub-threshold region at very low bias currents (in the range of a few nA down to a few tens of pA) (Sawigun and Serdijn 2016). But, operating transistors in weak-inversion region with very low bias currents puts a limit on the bandwidth and the linearity of the circuit (Enz *et al.* 1995).

- To save the silicon area on the chip and hence the cost of production, the number and size of the devices should be small. This makes the design of low-frequency filters arduous, requiring large time constants to realize low cut-off frequency. Reducing the number of active devices to save area can also lead to the deterioration of other characteristics like operating range, and mirroring accuracy, especially in current-mode circuits.

The above-mentioned voltage, power, and area constraints make the design challenging. The results of this research will have a significant impact on the design and development of low-power electronic systems and will help to enable the next generation of portable and battery-powered devices.

1.2 Conventional filter designs



(a) G_m-C **(b)** Active-RC

(c) G_m-OTA-C

Figure 1.2: Integrators

There are various architectures for designing CT filters. G_m-C (also denoted as g_m-C) and active-RC are the classical analog design techniques (Tsividis 1994). There are many applications where we prefer the particular one over another. Generally, G_m-C filters are able to perform high-speed operation as the integrators are working in open loop. But they suffer from poor linearity due to stray capacitances as these parasitics appear in parallel with the integrating capacitor. Generally, G_m-C filters find applications where we require high speed such as in hard disk drives.

On the other hand, active-RC integrators can be linear when a "good" opamp/OTA is available. Compared to G_m-C filter, active-RC filter has very good dynamic range

for a given power dissipation. Generally, the active device used in such filter will be an operational amplifier (opamp). But in low voltage CMOS process, it is difficult to build an opamp with low output impedance which can support larger swings. Hence it is convenient to use an operational transconductance amplifier (OTA) as the active device in place of opamp especially when the load to be driven is capacitive.
Figure 1.2a shows G_m-C integrator whose transfer function and unity gain frequency are given by (1.1) and (1.2) respectively.

$$H(s) = \frac{G_m}{sC} \tag{1.1}$$

$$f_0 = \frac{G_m}{2\pi C} \tag{1.2}$$

Figure 1.2b shows active-RC integrator whose transfer function and unity gain frequency are given by (1.3) and (1.4) respectively.

$$H(s) = \frac{-1}{sRC} \tag{1.3}$$

$$f_0 = \frac{1}{2\pi RC} \tag{1.4}$$

Compared to G_m-C filter, an active-RC filter has less excess noise and supports larger swings which results in better dynamic range. Since every node of an active-RC filter is either a virtual ground or output of opamp/OTA, they are insensitive to stray capacitances. To design active-RC filters with low cut-off frequencies, the resistor and capacitor should be very large. These large resistors and capacitors occupy more area on the chip. Therefore, simple active-RC filters are not suitable for low frequencies. But many techniques are available in the literature to increase the time constant of the filter without increasing the resistance and/or capacitance values. This gives a prominent motivation to build low frequency filter using active-RC integrators.

On the other hand G_m-OTA-C is a hybrid design of both active-RC and G_m-C integrator and is shown in Figure 1.2c. It operates faster than active-RC but slower than its G_m-C counterpart. The stray capacitance sensitivity issue of G_m-C is solved by this design but it still suffers from limited dynamic range and higher power consumption. This leads to poor power efficiency.

In order to design compact and energy-efficient filters, the recent trend is to replace

transconductors in a $G_m - C$ topology with single MOSFETs (Baschirotto *et al.* 2000). These type of filters are called as single branch filters. Source followers (SFs) and voltage followers (VFs) are widely used to implement these single branch filters.

Alternatively, log-companding (Adams 1979) is another approach to design low voltage and low power CT filters. Filters designed using this approach are called as log domain filters. The basic principle of log domain filter is shown in Figure 1.3. Here, input current signal (I_{in}) is converted to a compressed voltage signal (V_{in}) by using log function. This compressed voltage signal is processed through non-linear filter and converted back to current signal (I_{out}) by using exponential function. Hence, log domain filters are internally nonlinear and externally linear. As the magnitude of compressed voltage signals (V_{in} & V_{out}) is far less than the DC biasing voltage, the internal circuit need not be linearized. The input current signal can be as large as the DC bias current. This improves the signal swing and hence the DR. Log domain circuits are discussed in detail in subsequent sections.

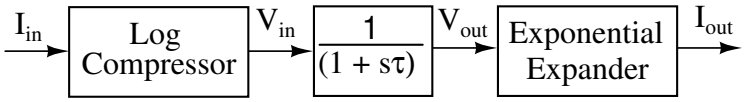


Figure 1.3: Principle of log domain filter

1.3 Prior works

1.3.1 Single branch filter

The design of continuous-time filters for biomedical and consumer electronics applications becomes difficult under very low power. Ultra-low power applications relegate conventional filter structures like active-RC and g_m-C owing to their increased circuit complexity and higher power consumption to realize higher-order filters. The high dynamic range in these filter structures is often concomitant with higher power consumption and the use of many active components. Moreover, the standard supply voltage scales down when the technology is scaled down. Circuits that satisfactorily work in higher CMOS technologies may not be sufficient to deliver the same performance in lower CMOS technologies. For instance, under low supply voltages, it is difficult to build an opamp/transconductor that can afford larger swings, so attaining

reasonable linearity in such filters is challenging. To operate satisfactorily under lower supply voltages, a compact energy efficient continuous time filter structure is introduced by Baschirotto *et al.* (2000), which has a single current-carrying branch and comprises two MOS devices and a capacitor to realize a first-order low pass function. This single-branch topology offers power-efficient analog signal filtering solutions than conventional designs for comparable or superior circuit performance in lower supply voltages. Later on, the trend of designing CT filters using a small number of devices for low-power applications gained traction.

To achieve a compact energy efficient circuit structure, this section explores the feasibility to realize CT filters from circuit structures capable of operating from a supply voltage of less than two gate–source voltages (V_{GS}) plus one saturation voltage (V_{dsat}) and employing only one branch of bias current (Sawigun *et al.* 2014).

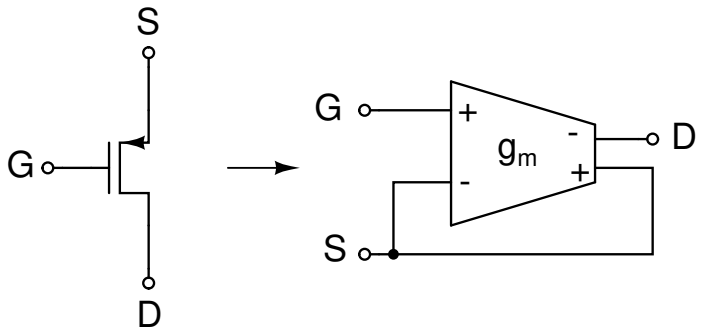


Figure 1.4: Single transistor and its macro model

The small signal operation a MOSFET that is properly biased in weak inversion saturation resembles that of a differential g_m cell connected in a negative feedback fashion as shown in Figure 1.4. To get rid of the body effect, a PMOS device is preferred in an n-well CMOS process. Neglecting channel length modulation, the transconductance of the transistor with zero V_{BS} (bulk and source terminals are connected) and carrying a current I_B (Enz *et al.* 1995) is given by

$$g_m = \frac{I_B}{\eta V_T} \tag{1.5}$$

Using this macro-model, several filter topologies can be found from circuit structures with a single branch bias current. An example is a source follower based LPF (SF

LPF) which is shown in Figure 1.5. The SF transfer function can be written as

$$H(s) = \frac{g_m}{g_m + g_{ds} + g_{do}} \cdot \frac{1}{1 + s.\frac{C_L}{g_m + g_{ds} + g_{do}}} \tag{1.6}$$

where g_{do} is the output conductance of the current source, g_m and g_{ds} are the transconductance and output conductance of transistor M_1. Because of its local feedback, SF LPF exhibits very good linearity even with a reduced overdrive. A second order

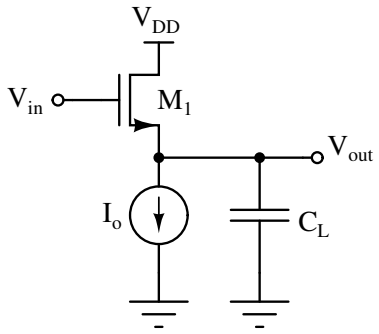


Figure 1.5: Source follower LPF

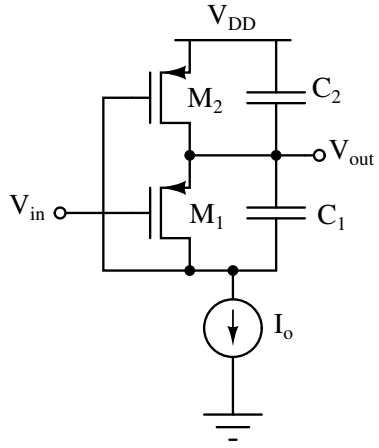


Figure 1.6: Flipped voltage follower LPF

LPF using flipped voltage follower (FVF) is shown in Figure 1.6. A supply voltage of less than 1 V is sufficient for the deep subthreshold operation of the circuit. Neglecting channel length modulation and parasitic capacitances of transistors, the transfer

function can be written as

$$H(s) = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}} \tag{1.7}$$

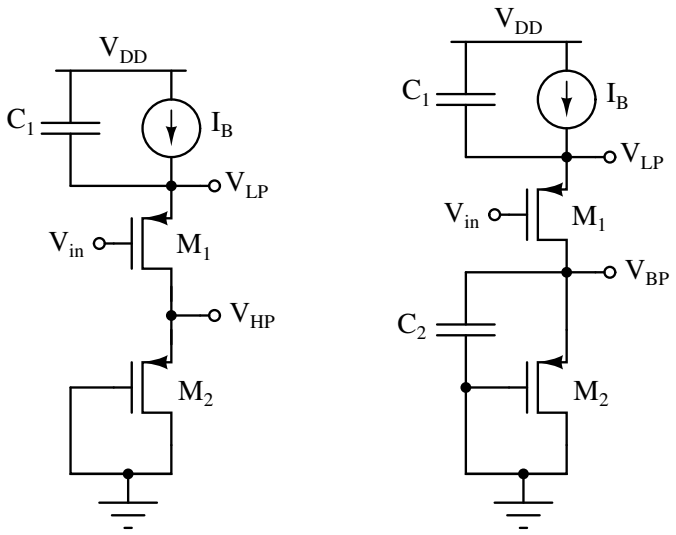


Figure 1.7: First order LP, HP and BP filters

Figure 1.7 shows some of other possible realizations of single-branch transistorized g_m–C filters. An LPF can be obtained from the circuits as shown in Figure 1.7 and HP filter from the former and BP filter from the latter. The circuits in Figure 1.7 are all formed by a cascode connection of transistors M_1 and M_2 and capacitors between source and AC ground terminals. Both transistors share the same bias current I_B. Replacing M_1 and M_2 by the macro-model of Figure 1.4, we can straight forwardly analyze that

$$H_{LP}(s) = \frac{V_{LP}(s)}{V_{in}(s)} = \frac{1}{1 + s(C_1/g_{m1})} \tag{1.8}$$

Without capacitor C_2, we obtain the following HP transfer function:

$$H_{HP}(s) = \frac{V_{HP}(s)}{V_{in}(s)} = \frac{-s(C_1/g_{m2})}{1 + s(C_1/g_{m1})} \tag{1.9}$$

By adding C_2 to the former HP output node, the following BP transfer function can

be achieved:

$$H_{BP}(s) = \frac{V_{BP}(s)}{V_{in}(s)} = \frac{-s(C_1/g_{m2})}{(1 + s(C_1/g_{m1}))(1 + s(C_2/g_{m2}))} \tag{1.10}$$

It can be seen that there are three filter topologies obtained from this single branch structure. Apart from the low current consumption, another advantage of these filters is that they feature a high impedance input node (being the gate of M_1).

Compact source follower-based low pass filter (SF LPF) with transistor biased in weak inversion region which is introduced by D'Amico *et al.* (2006) is used by Zhang *et al.* (2013) for biomedical applications. These transistorized g_m-C filters contain complementary devices and hence suffer from loss by bulk effect compromising the pass-band gain of the filter. Even though D'Amico *et al.* (2006) propose a compact folded filter topology whose minimum voltage is 1.25 V, it has two current-consuming branches and hence needs two current sources to realize a biquad function. This increases the number of active devices and can eventually contribute to the noise of the system. Zhang *et al.* 2013 use a gain compensation technique to compensate for pass-band attenuation; however, it requires extra circuitry, which demands more silicon area on the chip and higher power consumption. Single branch biquads using flipped voltage followers are presented by De Matteis and Baschirotto (2016), Sawigun and Pawarangkoon (2016), Xu *et al.* (2016). These are much more compact filter structures and can work under lower supply voltages. However, the driver and load in these structures are stacked and share the same current. Tuning of cut-off frequency requires tuning of bias current (I_B), which contributes to power dissipation. Moreover, stacking of input and driver devices, especially under lower voltages, offers a rigid choice of input and output common mode levels. Filter topology presented by Sawigun *et al.* (2014) can synthesize only real poles, and hence maximum Q factor which can be achieved is 0.5. Sawigun and Thanapitak (2018), Thanapithak and Sawigun (2018) also offer good attempts in the design of low-power, compact continuous time filters under low supply voltage. However, these structures exhibit a narrow linear range under lower supply voltages due to more active devices stacked between the power rails. They have both n-type and p-type devices, which lead to bulk-induced loss in the pass band. A literature survey was done on low frequency CT filter design. Since active-RC filters are found to be better than their G_m-C counterparts considering dynamic range and linearity, a comprehensive study was carried on realization of

large time constant (low bandwidth) in existing literature for building an active-RC filter for the acquisition of biological signals.

1.3.2 Log domain circuits

Most of the analog design techniques rely on the small-signal model of the transistor which attempts for linearization around an operating point. Thus, the linearity of the small-signal model imposes a limit on the maximum peak value of the input signal. Any futher attempts for linearization also lead to considerable power dissipation in these circuits. To overcome this drawback, it is essential to exploit the large-signal model of the transistor which eliminates the need for biasing and does not impose any restriction on the amplitude of the input signal.

Log domain filters or translinear filters are a class of filters which uses the logarithmic relation between the voltages and the currents. The translinear principle involves companding (compression and expanding) of the signal. So the dynamic range at different points of the signal path varies unlike in a conventional signal processing system. Figure 1.8 shows a traditional companding system (Mulder *et al.* 2012). C is the compressor which compresses the signal, i.e., at upper level large signals are attenuated by the compressor C where they can be processed by H without much distortion. At lower level, small inputs are amplified by C to a level much above the noise floor of H making the signal less susceptible to noise. E is the expander and expands the signal back to initial level. Its transfer function is $E = C^{-1}$.

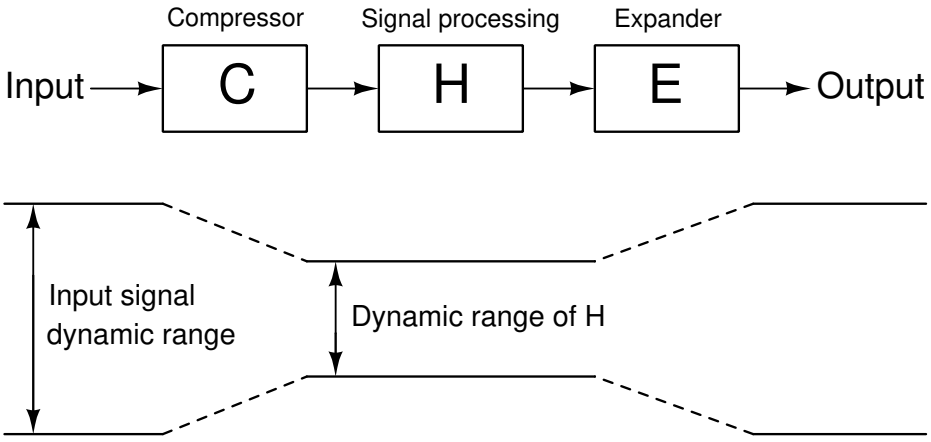


Figure 1.8: A typical setup of companding system

From Figure 1.8, we can conclude that a system having low dynamic range can process a signal that falls out of this range without any distortion by companding technique. These log domain/translinear circuits exploit the exponential large-signal behaviour of the bipolar transistor or the MOS transistor operating in the sub-threshold region. This enables the circuit to operate satisfactorily at extremely low voltages. A wide range of linear and non-linear functions can be implemented using the translinear circuits.

The concept of log-companding technique is explained by Seevinck *et al.* (2000). For a MOSFET operating in subthreshold region, the gate to source voltage is logarithmically related to its drain current.

For an NMOS transistor operating in sub-threshold region, the drain current is given by (1.11) (Taur and Ning 2013). Analysis of sub-threshold operation of the transistor with similar mathematical model is discussed in the appendix and is mentioned in subsequent chapters.

$$I_{Dn} = A_n exp\left[B_n\left(V_{GSn} - V_{thn}\right)\right]\left[1 - exp\left(\frac{-V_{DSn}}{V_T}\right)\right] \tag{1.11}$$

where,

$$A_n = \mu_n C_{ox}\frac{W}{L}(m_n - 1){V_T}^2$$

$$B_n = \frac{1}{m_n V_T}$$

where

$$V_T = \frac{kT}{q}$$

is the volt equivalent of temperature and m_n is the body-effect coefficient.

For $V_{DSn} \geq 4V_T$, the current I_{Dn} can be assumed to be independent of V_{DSn}. Then (1.11) can be simplified to (1.12).

$$I_D \approx Aexp\left[B\left(V_{GS} - V_{th}\right)\right] \tag{1.12}$$

1.3.2.1 Static translinear loop

Translinear loops are instantaneously companding and are broadly classified into two: static and dynamic translinear loop (Roberts and Leung 1999). Static Translinear Loop (STL) principle is used to implement frequency independent transfer functions.

For example, current multiplication or division can be implemented using voltage addition or subtraction. The schematic of STL is shown in Figure 1.9.

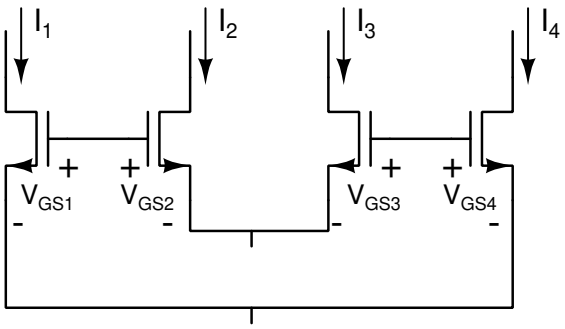


Figure 1.9: Static translinear loop

From the translinear loop, it can be written as follows

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \tag{1.13}$$

Since the transistor is operating in weak inversion region, its output current is exponentially related to input voltage given by

$$I_D = Aexp\left[B\left(V_{GS} - V_{th}\right)\right]\left[1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right] \tag{1.14}$$

When V_{DS} is large, (1.14) can be approximated to (1.15).

$$I_D \approx Aexp\left[B\left(V_{GS} - V_{th}\right)\right] \tag{1.15}$$

So $V_{GS} - V_{th}$ can be written as

$$V_{GS} - V_{th} = \frac{lnI_D - lnA}{B} \tag{1.16}$$

$$V_{GS} = \frac{lnI_D - lnA}{B} + V_{th} \tag{1.17}$$

V_{GS} from (1.17) is substituted in (1.13). All transistors are assumed to be identical so that the terms lnA, B and V_{th} can be eliminated from the equation.

$$I_{D1}I_{D3} = I_{D2}I_{D4} \tag{1.18}$$

This is the static translinear principle and is independent of process and temperature. This shows that addition of voltages as shown by (1.13) is equivalent to multiplication of currents as in (1.18).

1.3.2.2 Dynamic translinear loop

Dynamic Translinear Loop (DTL) is used to implement differential equations or frequency dependent transfer functions (Roberts and Leung 1999). DTL circuits are derived from STL circuits by adding capacitor in translinear loops. Consider the current mirror circuit shown in Figure 1.10. The capacitor C is connected in parallel with the diode connected transistor. The transistors are biased with a dc current of I_{dc}. I_{in}, I_{out} and I_C are the input, output and capacitor currents respectively.

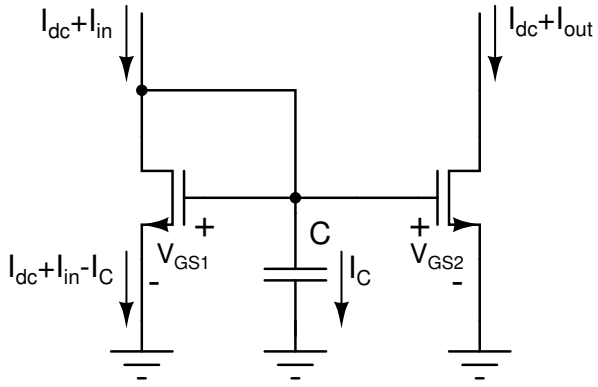


Figure 1.10: Dynamic translinear loop

From Figure 1.10, it can be seen that V_{GS} of the transistor is equal to the capacitor voltage V_C. Then (1.12) can be written as follows.

$$I_D \approx Aexp\left[B\left(V_C - V_{th}\right)\right] \tag{1.19}$$

Taking log on both sides of (1.19), we get

$$lnI_D = lnA + B\left(V_C - V_{th}\right) \tag{1.20}$$

where the capacitor voltage and current are related as

$$I_C = C\dot{V_C} \tag{1.21}$$

where $\dot{V_C}$ is the first order differential of V_C. Differentiating (1.20) and rearranging the terms, we get

$$\dot{I_D} = \left(\frac{B}{C}\right) I_D I_C \tag{1.22}$$

This is the dynamic translinear principle and states that a differential of a current is equal to the product of that current and a capacitor current. Similarly we can derive higher order differentials using same technique. This principle can be used to build vast variety of circuits like amplifiers, filters, RMS-DC converters etc.

1.3.2.3 RMS-DC converter

The root-mean-square (RMS) value of an electrical signal is a statistical measure of the signal. It represents the average energy content in the signal. An RMS-DC converter circuit measures the RMS value of the input signal. The RMS-DC converter finds applications in automatic gain control, digital multimeters, biomedical ICs, instrumentation devices and syllabic companding systems (Haddad *et al.* 2003, Richman 1967, Zidi *et al.* 2015). Many integrated RMS-DC converter circuits have been presented in the literature. Some of these are based on the bipolar translinear loops (Mulder *et al.* 1997, 1996, Surakampontorn and Kumwachara 1998). However, bipolar circuits are not suitable for the stringent low-voltage, low-power requirements of modern-day ICs. Also, in mixed analog-digital systems, it is desirable to implement circuits in standard CMOS technology. RMS-DC converters based on square-root domain (SRD) translinear loop (Asiaban and Farshidi 2010, López-Martín and Carlosena 2003) and linear class-AB transconductance (De la Cruz-Blas *et al.* 2005) have been designed in CMOS technology. However, these circuits suffer from two drawbacks: the first one, these circuits have MOS transistors operating in the strong inversion region and hence their power consumption is high; and the second, low supply voltage requirements restrict the dynamic range in these circuits. So a classical design approach, where the input range of operation deteriorates when the supply voltage decreases, is inadequate in such circumstances.

Log domain or translinear circuits are a class of circuits which use the logarithmic relation between the voltages and the currents. This design technique is a promising method towards the design of low power high dynamic range analog circuits. Attempts have been made towards the design of RMS-DC converters using FG-MOS transistors in log-domain (Farshidi and Sayedi 2007) and square-root domain (Farshidi and Nejad

2012). However, in these circuits, the capacitors at the floating gate of the transistors occupy large area. Also, removal of residual charges trapped in the floating gate during the fabrication process requires complex technology (Rodriguez-Villegas and Barnes 2003).

There are mainly two methods to design an RMS-DC converter. They are given below.

- Explicit method
- Implicit method

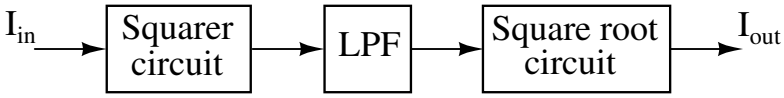


Figure 1.11: Block diagram of explicit RMS-DC converter

The block diagram of the explicit RMS-DC converter is shown in Figure 1.11. Squarer, LPF and square root circuit are cascaded in this technique. This technique always inherits the drawbacks of high circuit complexity, narrow bandwidth, and high power consumption. The implicit method of building an RMS-DC converter is discussed in detail in chapter 4 and some of the existing implicit realizations are discussed below.

RMS-DC converters based on the translinear principle, using MOS transistors operating in the sub threshold region, have been designed by Arraiza *et al.* (2019), Farshidi and Nejad (2012), Talkhouncheh *et al.* (2019). However, these implicit implementations which are based on the cascading of squarer-divider cells and low-pass filter use significant number of transistors, thus leading to increased circuit complexity. Current-mode RMS-DC converters based on explicit computation method are presented by Danesh *et al.* (2013), Kompitaya and Kaewdang (2011), Shaterian *et al.* (2015). These converters use the translinear principle to individually realise and cascade current-mode absolute-value circuit, squarer circuit, averaging circuit and square root circuit. This compromises the compactness and simplicity of the circuit and they suffer from high power consumption. RMS-DC converter using symmetric cascode MOS translinear loop cell (SCMC) is discussed by Shaterian *et al.* (2015). Explicit and implicit realisations presented in this paper require 31 and 18 transistors respectively which occupy significant silicon area on chip.

Mohammad Hadi *et al.* (2013), Minaei and Psychalinos (2015) and Maryan and Azhari (2018) present much more compact implicit realisation of RMS to DC converters.

However their designs are based on cascading of squarer divider and a low pass filter which still require significant number of transistors. Eventhough Minaei and Psychalinos (2015) present a fully integrable design, this limits the external tunability of the RMS-DC converter. Maryan and Azhari (2018) implement the converter with four $\frac{I_N}{2}$ sources instead of a single input current source (I_N). This needs additional circuitry apart from the main converter circuit. Design proposed by Maryan *et al.* (2019) shows better FoMs compared to other designs. However, the design uses two input current sources to achieve very low circuit complexity and hence needs additional transistors for copying input current. Design of the proposed translinear RMS-DC converter is discussed in detail in chapter 4.

1.3.2.4 Log domain filter

Log domain filter design is also promising technique in building compact CT filters. The idea of log domain filtering is first introduced in (Adams 1979) and thoroughly investigated in (Frey 1993, Seevinck 1990, Seevinck *et al.* 2000). In log-domain filters, the voltage at the integrating node is obtained by compressing the current, which results in a lower signal swing at the capacitor node, implying low voltage operation. Large dynamic range and electronic tunability using current sources are the important characteristics of log-domain filters. Numerous attempts have been made towards the design of log-domain filters using BJTs (Frey 1993, Mulder *et al.* 2001, 1998, Prommee and Dejhan 2013, Seevinck 1990). However, the use of BJTs requires larger bias currents and hence leads to relatively larger power consumption. Log-domain filters using MOSFETs operating in sub-threshold region allow lower bias currents as compared to BJTs (El-Masry and Wu 1999, Jain and Singh 2016, Python *et al.* 1999, Toumazou *et al.* 1994, Zhang *et al.* 2017). In the designs presented by Gerosa *et al.* (2004), La Croz-Blas *et al.* (2005), Tsirimokou and Psychalinos (2014), Zhang *et al.* (2017), low-frequency log domain filters are implemented for biomedical applications. However, these filters employed very large capacitors, which occupy large area on the chip.

1.3.3 PTAT current reference

Log-domain filters and transconductance-capacitor ($G_m - C$) filters can be used in biological data acquisition system which involves low frequency signals like ECG (electrocardiogram) and EEG (electroencephalogram). Since the transistors in these log-domain filters are working in sub-threshold mode of operation (weak-inversion), a low cut-off frequency can be achieved with low values of bias currents (order of nA).

The cut-off frequency (f_c) of log-domain and $G_m - C$ filters is given by (1.23) (Gerosa *et al.* 2004, Schaumann *et al.* 2009).

$$f_c = \frac{G_m}{2\pi C} = \frac{I_o}{2\pi\eta V_T C} \tag{1.23}$$

where η, I_o and V_T are sub-threshold slope factor, bias current and thermal voltage respectively. (1.24) gives the expression for thermal voltage.

$$V_T = \frac{kT}{q} \tag{1.24}$$

where k, T and q have their usual meanings. (1.23) shows the direct relation between cut-off frequency and bias current. I_o is usually generated from a current reference circuit. The current reference should be stable against variations in process and supply voltage. Supply voltage sensitivity is the parameter which shows the stability of the current reference against supply voltage variations. Lower supply voltage sensitivity indicates a better current reference. Depending on the mode of operation of transistors in the circuit or the topology of the filter architecture, the current reference can be a temperature independent or Proportional to Absolute Temperature (PTAT) current reference. From (1.23) and (1.24), in log-domain and $G_m - C$ filters, it is evident that f_c has an inverse relationship with temperature. To fix this problem, I_o is generated in such a way that it has also a linear relationship with temperature. Thus a PTAT current reference is used to bias log-domain/$G_m - C$ filters. As a cumulative effect, the filter cut-off frequency remains constant over temperature variations.

Many PTAT current reference designs are explored in the literature. Beta-multiplier based circuits discussed by Gray *et al.* (2001), Razavi (2005), Vittoz and Fellrath (1977) have adequate PTAT current characteristics. However, to generate low reference currents under low supply voltage for low frequency filters used in biological data acquisition system, larger values of resistors are needed which occupies large

area on chip. Moreover the control over temperature coefficient of resistance also becomes difficult. A comprehensive research has been carried out on the conventional PTAT designs to tackle such shortcomings (Camacho-Galeano *et al.* 2005, Magnelli *et al.* 2011, Serra-Graells and Huertas 2003). Camacho-Galeano *et al.* (2005) use self-cascode transistors used instead of resistor in PTAT circuit. This improves supply variation rejection, but linearity in current versus temperature characteristic has been compromised. Composite transistors are used in the PTAT circuit presented by Rao *et al.* (2019) to enhance the supply voltage sensitivity, but large resistor values are needed to generate smaller currents. Gerosa *et al.* (2004), Malik *et al.* (2001) use switched capacitors in place of resistor. But PTAT current is generated from PTAT voltage using opamp circuits like voltage to current converter which in turn increases the overall power dissipation of the circuit. Rao and Rekha (2019) present a good switched capacitor based PTAT reference. But the settling time of the reference current is compromised.

1.3.4 Realization of large time constant

Since this thesis focuses on building energy efficient circuits that can be integrated into biomedical devices/ implants, such circuits need to handle many of physiological signals/electrical activities. The electrical activity within the human body has slow propagation times such that these signals typically range from 1 Hz to 1 kHz (Stotts 1989). Biological signals such as electrocardiogram (ECG), electroencephalogram (EEG), electromyogram (EMG), electrooculogram (EOG) etc., are often small signals having amplitude varying from a few microvolts to a few millivolts of low frequency. The typical frequency range of these signals and their amplitudes are shown in Table 1.1 (Webster 2009).

Table 1.1: Biological Signals

Signal	Frequency (Hz)	Amplitude (mV)
ECG	0.01 - 250	0.05 - 4
EEG	0 - 150	0.005 - 0.3
EMG	0 - 10 k	0.1 - 5
EOG	0 - 50	0.05 - 3.5

To handle such low frequency signals, the filters in such circuits should have very less bandwidth. To design CT filters with low cut-off frequency (large time constant), the resistor and capacitor should be very large. These large resistors and capacitors occupy more area on the chip. To save silicon area on the chip, many unconventional circuit techniques are presented in the literature to enhance the time constant of CT filters. They can be extended to the design of low value current reference circuits as well (order of nA) which is discussed in detail in chapter 6. Some of the time constant enhancement techniques are discussed below.

- Current Steering
- Pseudo Resistor
- R-2R Ladder Network
- Capacitance Scaling

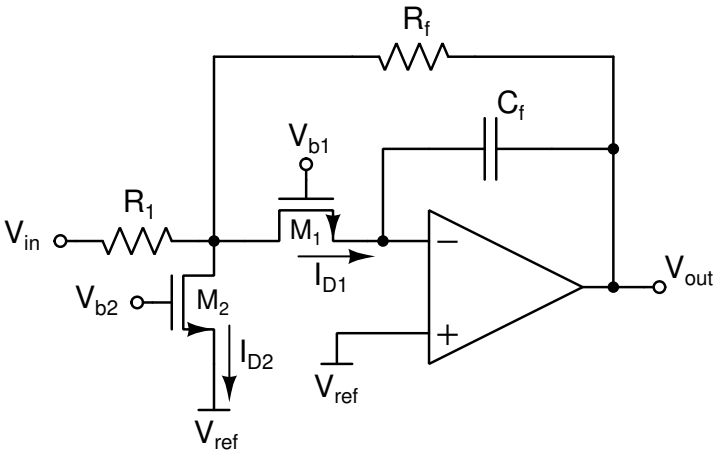


Figure 1.12: Current steering in low-pass filter

A first order active-RC LPF using current steering technique is shown in Figure 1.12 and the original idea was introduced by Moon and Song (1993). A small fraction of input current (I_{D1}) is flowing through M_1 to charge and discharge the output capacitor (C_f) and most of the current (I_{D2}) is bypassed through M_2. Thus, the cut-off frequency can be reduced compared to traditional active-RC filters without employing very large capacitors and resistors.

The transistors M_1 and M_2 are operating in triode region and work as voltage controlled resistors. The cut-off frequency of the filter can be tuned by varying V_{b1}

or V_{b2}. The transfer function and the cut-off frequency of the circuit shown in Figure 1.12 are given by (1.25) and (1.26) respectively.

$$H(s) = \frac{-\frac{R_f}{R_1}}{1 + s\frac{R_f C_f}{\alpha}} \tag{1.25}$$

$$f_c = \frac{\alpha}{2\pi R_f C_f} \tag{1.26}$$

where

$$\alpha = \frac{I_{D1}}{I_{D1} + I_{D2}} \approx \frac{I_{D1}}{I_{D2}} \ll 1$$

A second order active-RC LPF with cut-off frequency of 18 Hz for heart rate measurement using current steering technique is implemented by Wong *et al.* (2005). A fully integrated 5 mHz first order high-pass filter for electrophysiological signal acquisitions using current steering technique is implemented by Li *et al.* (2012) with a power consumption of 15 mW.

In active-RC filters, the resistor can be replaced with MOSFET operating in triode or weak-inversion region. These types of filters are called MOSFET-C filters. The resistor implemented employing the transistor in weak-inversion region is called as pseudo resistor. Resistance value can be controlled by varying V_{GS} of the transistor. By properly biasing the transistor with V_{GS}, resistance value in the order of giga ohms can be implemented with this technique. As the resistance depends on V_{GS}, its value is sensitive to bias conditions and any variations in supply voltage can affect its value which could lead to distortion (Li *et al.* 2012).

A tunable pseudo resistor (several MΩ to hundreds of GΩ) featuring a wide input voltage range and auto-tuning circuit is proposed by Shiue *et al.* (2011). However, this circuit needs more number of transistors, which produces extra noise. A pseudo resistor based second order MOSFET-C filter with cut-off frequency tuned over 20 Hz - 184 kHz has been implemented by Tajalli and Leblebici (2012). Khumsat and Worapishet (2012) propose a 5^{th} order R-MOSFET-C low-pass filter with the cut-off frequency tunable from 91 - 268 kHz. The circuit consumes a power of 0.6 mW.

R-2R ladder shown in Figure 1.13 (Roy 2015) is capable of achieving large time constant because their equivalent-resistance (transfer-resistance) is much greater than

their total actual resistance. They preserve high linearity (because of poly resistor) compared to resistors formed by MOSFET.

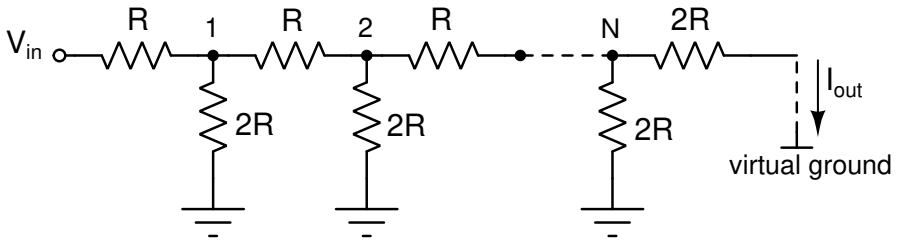


Figure 1.13: R-2R ladder network

At each node, the current is bypassed through 2R and finally small amount of current (I_{out}) is flowing into the opamp virtual ground. The transfer-resistance, R_T is given by

$$R_T = \frac{V_{in}}{I_{out}} = 2^{N+1}R \tag{1.27}$$

where N is the length of the ladder network.

The total resistance, $R_{total} = (3N + 2)R$ and the area saving factor,

$$S_A = \frac{2^{N+1}}{3N + 2}$$

.

A 4^{th} order R-2R ladder based active-RC notch filter is proposed by Alzaher *et al.* (2013). This achieves an area saving of approximately 120 times. A generalized R-αR ladder network is proposed by Roy (2015) to increase the transfer-resistance in small area. The gain error and cut-off frequency error depend on number of stages of the ladder and α. Roy (2015) shows that the R-0.5R ladders provide more area efficient solution leading to low frequency implementations. But, a large number of resistors can contribute to the thermal noise of the circuit which compromises the dynamic range and linearity of the circuit.

Similar to resistance scaling techniques as discussed above, capacitance scaling techniques can also be employed to realize a large time constant. One such circuit is proposed by Silva-Martinez and Vazquez-Gonzalez (1998). Figure 1.14 shows an impedance scaling down (admittance scaling up) circuit.

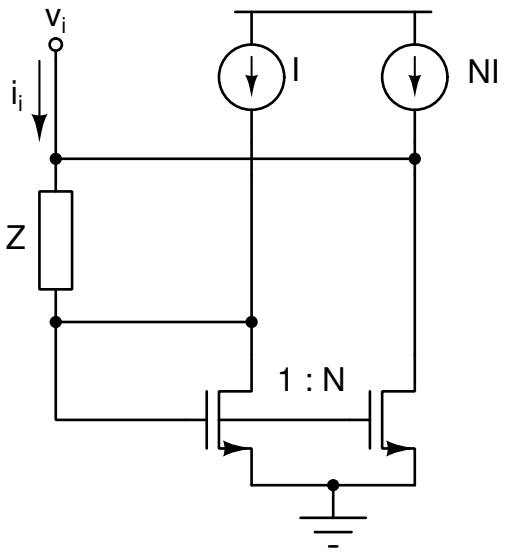


Figure 1.14: Impedance scaling down technique

If the transconductance of diode-connected transistor is large, the input current can be written as in (1.28).

$$i_i = \frac{N+1}{Z} v_i \tag{1.28}$$

Therefore, equivalent impedance is scaled down by a factor of (N+1) and can be written as follows.

$$Z_{eq} = \frac{Z}{N+1} \tag{1.29}$$

If the impedance is capacitive, the capacitance value is scaled up by a factor of (N+1). i.e., if

$$Z = \frac{1}{j\omega C}$$

then

$$C_{eq} = (N+1)\, C \tag{1.30}$$

(1.30) implies the realization of larger value of capacitance without consuming much silicon area and is desirable for low-frequency applications.

Unlike the techniques discussed above, a low power low voltage OTA for ECG detection is given by Chung *et al.* (2006). A HPF with a cut-off frequency of 50 mHz and a LPF filter with a cut-off frequency of 45 Hz are used to process the ECG signals in the above range.

As a summary of the literature review carried out by this research, the major architectures of all the above mentioned circuits are consolidated and is shown in Table 1.2.

Table 1.2: Existing works related to the circuits proposed in this thesis

Circuit	Architecture	Reference
Single branch filter	SF LPF (transistorized g_m-C)	D'Amico *et al.* (2006)
	FVF	Sawigun and Pawarangkoon (2016)
	SF LPF (with gain compensation)	Zhang *et al.* (2013)
Log-domain filter	Diode based	Adams (1979)
	BJT based	Frey (1993)
	Subthreshold MOS	Zhang *et al.* (2017)
RMS-DC converter	FG-MOS	Farshidi and Sayedi (2007)
	Square root domain	Farshidi and Nejad (2012)
	Subthreshold MOS (Explicit method)	Kompitaya and Kaewdang (2011)
	Subthreshold MOS (Implicit method)	Mohammad Hadi *et al.* (2013)
PTAT reference	Resistor based beta multiplier	Gray *et al.* (2001)
	Self cascode transistor	Camacho-Galeano *et al.* (2005)
	Composite transistor	Rao *et al.* (2019)
	Switched capacitor	Gerosa *et al.* (2004)
Realization of large time constant	Current steering	Moon and Song (1993)
	R-2R ladder	Roy (2015)
	Pseudo resistor	Shiue *et al.* (2011)
	Impedance scaling	Silva-Martinez and Vazquez-Gonzalez (1998)

1.4 Thesis Contributions

1.4.1 Research gap and Motivation

From the above subsections, it is clear that the existing designs are not sufficiently efficient in terms of energy consumption. If energy is taken as cost, the dynamic range, cut-off frequency, order and Q of the filter etc. can be accounted as the performance of the circuits. This research attempts to push the performance boundary of such circuits

either by proposing a novel architecture or by addressing a performance shortcoming in an existing design. Thus, the energy efficiency of these circuits can be improved.

Attaining motivation from the shortcomings of conventional filter design under low supply voltages which are detailed in previous sections, this research attempts to bridge the gap in the area of power-efficient signal filtering compatible with a low-voltage environment. This research contributes to the literature by proposing a novel biquad cell that uses folded single branch transistorized g_m-C topology and contains only PMOS devices. Thus, passband gain is no longer affected by the bulk effect of the devices, and the filter has low 1/f noise. This structure shows enhanced output swing and, at the same time, uses only a single current source to realize a biquad function. Since the driver and load devices appear in different branches, a convenient choice of input common mode level can be made, and tuning of frequency response can be done by programming the current levels in the branches. This improves the tuning flexibility of the circuit and makes it easier to cascade with other blocks inside the System on Chip (SoC). This filter structure is highly compact, energy-efficient and exhibits better dynamic range for a given supply voltage compared to other designs in the literature and can be used in low voltage, high dynamic range applications like biomedical signal processing. This thesis also explores translinear principle in filter design and a compact LPF is proposed. Their details are given in chapters 2 and 3.

Considering all the drawbacks in the existing literature of RMS-DC converters which are discussed in previous sections, this work identifies a research gap in the design of low-power, compact circuits for RMS-DC conversion. This work contributes to the literature by developing a current-mode RMS-DC converter based on the dynamic translinear principle. The proposed circuit uses a third-order translinear loop employing MOS transistors operating in the weak inverted saturation region. A squarer divider and a low pass filter are together realized within a third-order translinear loop instead of cascading individual blocks. Hence, the proposed circuit offers the benefits of low power consumption as well as reduced circuit complexity. The translinear nature of the circuit allows it to handle currents larger than the bias current of the circuit. Moreover, the proposed converter is externally programmable by offering provisions for tuning the lower and higher ends of bandwidth. Details are discussed in chapter 4.

Settling time of current reference becomes a significant aspect especially in high speed applications. When the settling time of the reference current increases, the

circuit which uses this reference current to generate its bias current also takes a significant amount of time to settle its bias current to steady state value. In case of a filter used in a wireless communication system, it takes a significant time to fix its cut-off frequency which may lead to attenuation of relevant signal information. For example, the circuit presented by Rao and Rekha (2019) requires 8 ms to stabilise its current which means that it takes around 8 ms for the subsequent filter to fix its cut-off frequency which is biased by this reference current source. This thesis proposes a feasible solution to this problem. This is discussed in chapter 5.
Transistors in all the above mentioned proposed circuits are operated in sub-threshold region with current in the range of a few nAs hence resulting in very less power consumption. All the circuits are designed and simulated using Cadence Virtuoso tool. To check the robustness of these proposed designs, Monte Carlo simulations (for process variations and device mismatch) and simulations across Process, Voltage and Temperature (PVT) variations are performed. All the designs are found to be robust across these variations.

1.5 Thesis Organization

This thesis is organized as follows.

- In chapter 2, a biquad cell using folded single branch structure is proposed which works under a supply voltage of 0.6 V. To illustrate the energy efficiency of the biquad, a fourth order differential LPF is designed and performance is studied.
- In chapter 3, an area efficient compact log domain filter is proposed which uses a second order translinear loop which operates under a supply voltage of 0.9 V. A second order LPF is designed using the proposed first order cell. This chapter discusses how a differential equation is translated into the building of circuits using the log-domain principle.
- Chapter 4 presents a current mode true RMS-DC converter based on a third order translinear loop. This chapter also studies the performance of the converter in a real world application.
- Chapter 5 presents a switched capacitor based PTAT current reference circuit that has a shorter settling time.

- In chapter 6, an active-RC filter is designed which can be used for the detection of ECG signals. To achieve low bandwidth, this chapter explores the technique of current steering in CT filter design.
- Conclusions and future directions are given in chapter 7.

Chapter 2

FOLDED SINGLE BRANCH BIQUAD

This chapter proposes a novel biquad cell that is derived from a single branch transistorized g_m-C filter which was discussed in the previous chapter. SF based single branch cells are able to synthesize only real poles so that a quality factor (Q factor) higher than 0.5 is unattainable. In this chapter, a novel design of single branch filter is introduced such that a Q factor higher than 0.5 is obtained. Discussions are given in subsequent sections.

2.1 Folded single branch biquad

2.1.1 Principle of folding in filters

The basic idea of single branch filter is developed by Baschirotto *et al.* (2000) where a single transistor is considered as a transconductor (G_m). A first order single branch filter is shown in Figure 2.1. Neglecting channel length modulation, the transfer function of this filter can be determined by the small signal equivalent and is given by,

$$H(s) = -\frac{\frac{g_{m1}}{g_{m2}}}{1 + s\frac{C_L}{g_{m2}}} \tag{2.1}$$

Since same type of devices are used as the driver and the load, driver non linearity is intrinsically compensated by the load linearity, delivering a high overall linear range even with a low device overdrive. However, the load and the driver are stacked between

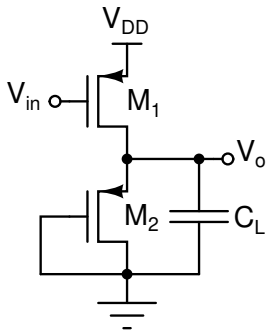


Figure 2.1: First order single branch cell

the two power rails, V_{DD} and ground. This gives a constraint on the minimum supply voltage. An independent tuning is also impossible since current tuning affects both pole frequency and dc gain. To overcome these drawbacks, single branch filter is folded so as to facilitate flexible tuning. The folded first order cell is shown in Figure 2.2. The transfer function and all other features remain same in this folded topology

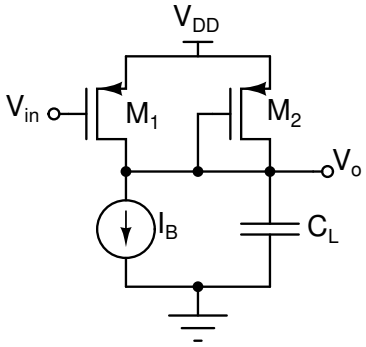


Figure 2.2: Folded first order single branch cell

except the current sharing.

2.1.2 Proposed folded biquad

This work proposes a biquad by extending the folded first-order cell. As a result, this biquad structure inherits the circuit benefits of "folding". The proposed biquad is shown in Figure 2.3. For a better transconductance efficiency and lower power consumption, all transistors are operated in the weak-inversion saturation region ($|V_{GS}| < |V_{th}|$ and $|V_{DS}| > 3V_T$). M_1 and M_2 are the driver and load devices respectively. I_B is the bias current which is fixed at 100 nA for a cut-off frequency of

15 kHz. To synthesize a pair of complex poles, the transistor M_3 and the capacitor C_2 are introduced in the load branch consisting of M_2 and capacitor C_1. M_3 is biased with voltage V_b.

The simplified small signal model of the proposed circuit is shown in Fig. 2.4. r_o rep-

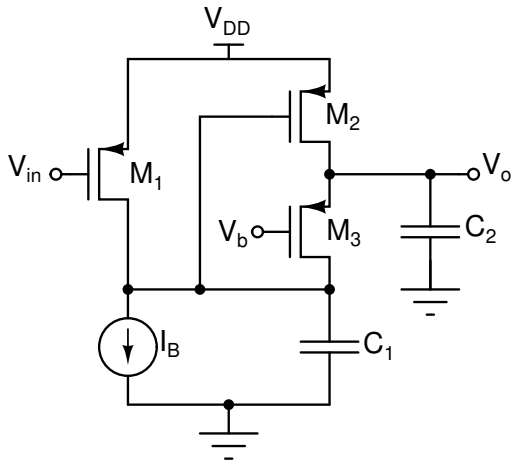


Figure 2.3: Proposed biquad cell

resents the finite output resistance due to channel length modulation. From the small

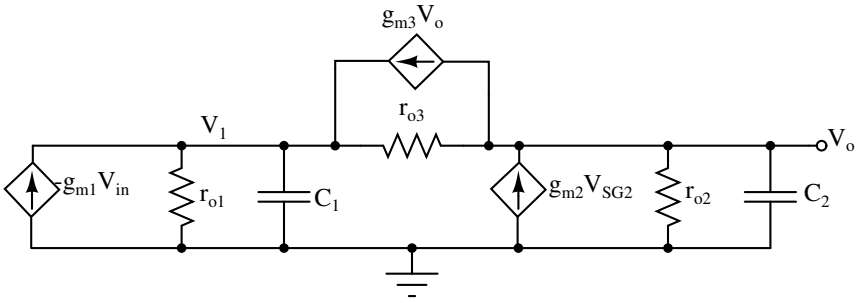


Figure 2.4: Small signal equivalent of the proposed biquad

signal equivalent of the circuit, the nodal equations can be written. If the voltage at the drain of M_1 is V_1, the KCL equations can be written as the following.

$$g_{m1}V_{in} - g_{m3}V_o + \frac{V_1}{r_{o1}} + sCV_1 + \frac{V_1 - V_o}{r_{o3}} = 0 \tag{2.2}$$

$$g_{m3}V_o - g_{m2}V_{SG2} + \frac{V_o}{r_{o2}} + sC_2V_o + \frac{V_o - V_1}{r_{o3}} = 0 \tag{2.3}$$

Note that V_{SG1}=-V_{in} and V_{SG3}=V_o. By solving the above KCL equations and doing necessary approximations, the transfer function of this biquad is given by,

$$H(s) = \frac{V_o}{V_{in}} = -\frac{g_{m1}g_{m2}r_{o1}r_{o2}r_{o3}}{s^2(r_{o1}r_{o2}r_{o3}C_1C_2) + s(g_{m2}g_{m3}{r_{o1}}^2r_{o2}r_{o3}C_1) + g_{m2}g_{m3}r_{o1}r_{o2}r_{o3}} \quad (2.4)$$

From the above equation, the pole frequency (ω_o), quality factor (Q) and the DC gain (H) of the proposed biquad can be written as,

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_1C_2}} \quad (2.5)$$

$$Q = \frac{1}{r_{o1}} \cdot \sqrt{\frac{C_2}{C_1\left(g_{m2}g_{m3}\right)}} \quad (2.6)$$

$$H = \frac{g_{m1}}{g_{m3}} \quad (2.7)$$

Since M_2 and M_3 share same current and having same size, g_{m2}=g_{m3}. If C_2=kC_1, then

$$\omega_o = \frac{g_{m2}}{C_1\sqrt{k}} \quad (2.8)$$

g_{m2} depends on the current flowing through M_2 branch and hence ω_o can be tuned by programming the current levels in the branches without affecting the total power dissipation. Similarly, Q factor can be simplified as,

$$Q = \frac{\sqrt{k}}{g_{m2}r_{o1}} \quad (2.9)$$

By tuning the output resistance of M_1, the Q factor can be tuned, and this can be done by properly choosing the length of the device. For example, to design the filter for a cut-off frequency of 15 kHz and a Q factor of 0.6 with a bias current of 100 nA and same value capacitors (k=1), the following steps can be adopted.

$$Q = \frac{1}{g_{m2}r_{o1}} \quad (2.10)$$

$$r_{o1} = \frac{1}{g_{ds1}} = \frac{1}{\lambda I_{D1}} \quad (2.11)$$

$$g_{m2} = \frac{I_{D2}}{\eta V_T} \quad (2.12)$$

For simplicity, assume I_{D1}=I_{D2}=50 nA and V_T=26 mV at room temperature and η ≈2.

$$\therefore g_{m2} = 1\ \mu S \tag{2.13}$$

For a Q=0.6, r_{o1}= 1.66 MΩ and since $\lambda \propto \frac{1}{L}$, from (2.11), length of M_1 can be fixed at 300 nm. For f_c=15 kHz,

$$f_c = \frac{g_{m2}}{2\pi C_1} = 15\ kHz \tag{2.14}$$

$$C_1 = C_2 = \frac{g_{m2}}{2\pi f_c} \approx 10\ pF \tag{2.15}$$

Since I_{D1}=I_{D2}=50 nA, $g_{m1} \approx g_{m2}$. ∴ DC gain H=1. Width of the devices are optimised to allow the subthreshold region of operation for 50 nA current in each branch of the biquad. Since the input and load devices appear in separate branches, unlike in many of the similar existing designs whose common mode voltage is near to one of the power rails, a relatively more convenient choice of input common mode level can be made. This feature of the filter facilitates easier cascading with other blocks in the chip.

2.1.3 Noise analysis

To study the effect of noise in the proposed biquad, it is necessary to develop its corresponding noise model. The noise behavior of the circuit is studied by exciting the ideal noiseless circuit with the equivalent noise generated by the circuit and is shown in Figure 2.5. To estimate the equivalent input noise and noise response of the

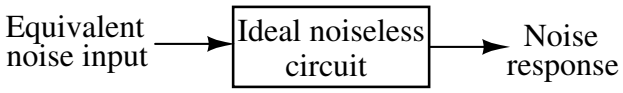


Figure 2.5: Noise behaviour

filter, MOSFET noises are considered and the major contributors of MOSFET noises are : (a) MOSFET channel thermal noise, which can be modeled as a current source connected between drain and source and is expressed as

$$\frac{\overline{i_{cn}{}^2}}{\Delta f} = 4kT\gamma g_{do} \tag{2.16}$$

where γ is 2/3 or higher and g_{do} is zero bias drain conductance, the remaining symbols have their usual meanings. (b) Flicker noise or 1/f noise, which can be modeled as a current source connected between drain and source and is expressed as

$$\frac{\overline{i_f{}^2}}{\Delta f} = \frac{K_f}{f}\frac{g_m{}^2}{C_{ox}WL} \tag{2.17}$$

where K_f is the device-specific constant which is typically less for PMOS devices, W and L are the effective width and length of the device. (c) MOSFET gate-induced thermal noise, which can be modeled as a current source between gate and source and is expressed as

$$\frac{\overline{i_g{}^2}}{\Delta f} = 4kT\delta g_g \tag{2.18}$$

where δ is 4/3 or higher and $g_g = \frac{\omega^2 C_{gs}{}^2}{5g_{d0}}$. However, all the devices used in the filter are PMOS; hence, 1/f noise or flicker noise can be discarded since the order of 1/f noise of PMOS devices is less than that of NMOS devices. Gate-induced thermal noise becomes a significant contributor only at higher frequencies when channel charge in the inversion region fluctuates. So the prominent contributor of MOSFET noise is channel thermal noise and will be denoted as $\overline{i_n{}^2}$ in the succeeding discussions. Assuming the capacitors are lossless, a noise equivalent of the proposed biquad is presented in Figure 2.6. Transistors M_1 and M_2 are the major noise contributors,

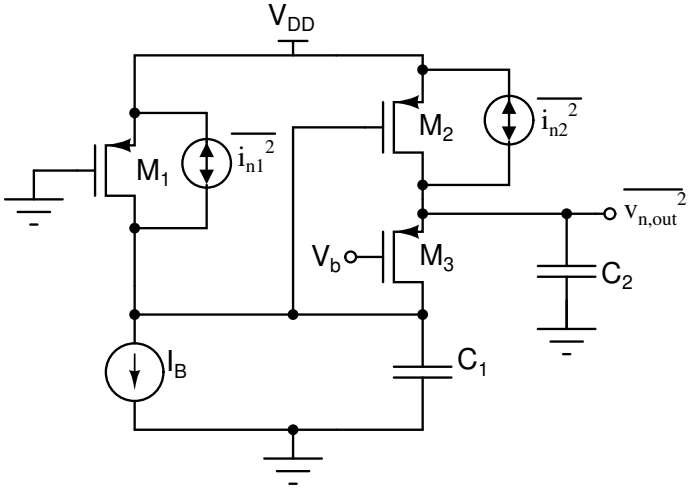


Figure 2.6: Noise model of the filter

and their noise currents are shown in parallel with the devices. Since transistor M_3

is a cascode device, due to source degeneration which introduces negative feedback at relatively lower frequencies, noise gain is divided by a factor of approximately $g_{m3}r_{o3}$ and hence is negligible compared to the contribution of M_2. The noise power spectral density at the output is expressed as

$$\overline{v_{n,out}{}^2} = \overline{v_{n1,out}{}^2} + \overline{v_{n2,out}{}^2} \tag{2.19}$$

where $\overline{v_{n1,out}{}^2}$ and $\overline{v_{n2,out}{}^2}$ contributed by $\overline{i_{n1}{}^2}$ and $\overline{i_{n2}{}^2}$ respectively.

$$\overline{v_{n1,out}{}^2} = \frac{\overline{i_{n1}{}^2}}{g_{m1}{}^2} \cdot |H(s)|^2 \tag{2.20}$$

The maximum noise spectral density occurs in the pass band, where the filter gain is unity. Hence,

$$\overline{v_{n1,out}{}^2} = \frac{\overline{i_{n1}{}^2}}{g_{m1}{}^2} \tag{2.21}$$

$$\overline{v_{n1,out}{}^2} = \frac{\overline{i_{n1}{}^2}}{g_{m1}{}^2} = \frac{4kT\gamma g_{do}}{g_{m1}{}^2} \tag{2.22}$$

For ease of analysis, g_{do} is approximately equated to g_m, transconductance in saturation. So (2.22) becomes,

$$\overline{v_{n1,out}{}^2} = \frac{4kT\gamma}{g_{m1}} \tag{2.23}$$

γ is taken as 2/3 (the real theoretical determination of γ is complex), and the transconductance in weak inversion region is given by

$$g_m = \frac{I_B}{\eta V_T} \tag{2.24}$$

Considering the current flowing through M_1 is a fraction of the total bias current (αI_B), (2.23) becomes

$$\overline{v_{n1,out}{}^2} = \frac{8q\eta {V_T}^2}{3\alpha I_B} \tag{2.25}$$

Similarly,

$$\overline{v_{n2,out}{}^2} = \overline{i_{n2}{}^2} \cdot {R_{out}}^2 \tag{2.26}$$

where R_{out} is the output impedance. Approximating for g_{do} and rearranging the terms,

$$\overline{v_{n2,out}{}^2} = \frac{8kTg_{m2}}{3} \cdot {R_{out}}^2 \tag{2.27}$$

$$\overline{v_{n2,out}{}^2} = \frac{8q(1-\alpha)I_B}{3\eta} \cdot R_{out}{}^2 \tag{2.28}$$

The total noise power spectral density at the output is obtained by adding (2.25) and (2.28).

$$\overline{v_{n,out}{}^2} = \frac{8q\eta V_T{}^2}{3\alpha I_B} + \frac{8q(1-\alpha)I_B}{3\eta} \cdot R_{out}{}^2 \tag{2.29}$$

Note that the input noise power spectral density is same as (2.29) since the filter has unity gain. The output impedance (R_{out}) has an inverse relationship with the current, and hence the total noise PSD decreases with an increase in bias current; however, this contributes to power dissipation.

2.2 Fourth order filter

To test the power efficiency of the proposed biquad, a fourth order filter is realized by cascading two such biquads. A fully differential version of the fourth order filter is shown in Figure 2.7. $M_{1a,b}$ are the input devices, and the differential output is taken across capacitor C_4. The sizes of all transistors used are given in Table 2.1.

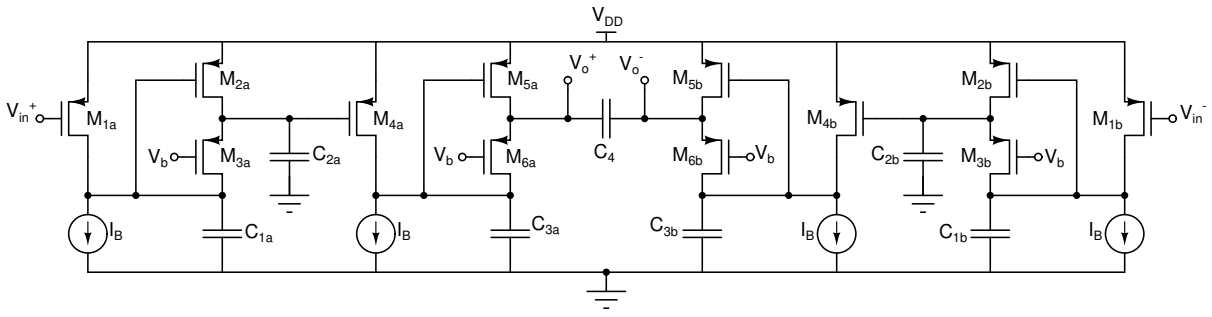


Figure 2.7: Fully differential fourth order filter

Table 2.1: Size of transistors in Figure 2.7

Transistors	W/L (μm/μm)
$M_{1a,b}$, $M_{4a,b}$	8/0.3
$M_{2a,b}$, $M_{3a,b}$, $M_{4a,b}$, $M_{5a,b}$	2/0.5

2.2.1 Post layout simulation results

The proposed fourth order filter in Figure 2.7 is designed in UMC 65 nm CMOS technology and post layout simulations are carried out. The layout is shown in Figure 2.8. The circuit consumes a layout area of 347 μm $\times$ 245 μm with an active area of 36 μm $\times$ 17 μm. The active area is shown in Figure 2.9. The circuit operates at a supply voltage of 0.6 V and with a bias current (I_B) of 100 nA. The bias voltage V_b for the cascode transistors is fixed at 100 mV. The fully differential version of the circuit consumes a power of 300 nW. For a cutoff frequency of 15 kHz, the capacitances $C_{1a,b}$, $C_{2a,b}$, $C_{3a,b}$ and C_4 are chosen to be 9.6 pF.

Figure 2.10 shows the frequency response of the filter. It has a cut-off frequency

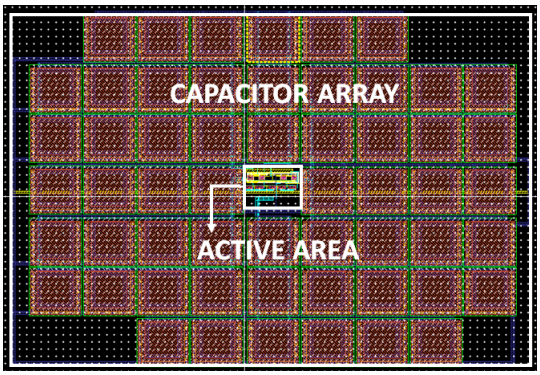


Figure 2.8: Layout of the filter

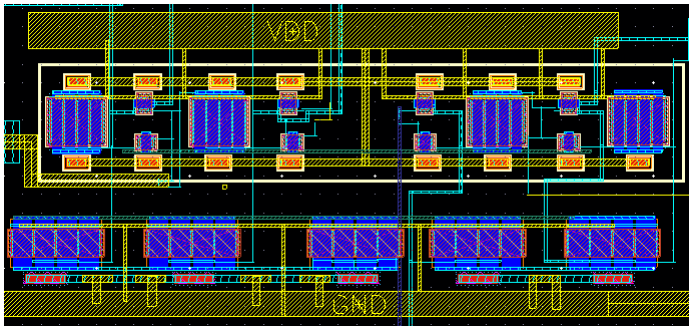


Figure 2.9: Enlarged view of the active area

(f_c) of 15 kHz with 0 dB pass band gain, and a roll-off rate of -80 dB/decade which implies a four-pole system response. The variation of fc is plotted for different I_B values. The nominal current value (I_o) is fixed at 100 nA and I_B/I_o is varied from 0.25 to 1.5. This is shown in Figure 2.11. The plot shows that f_c varies linearly with

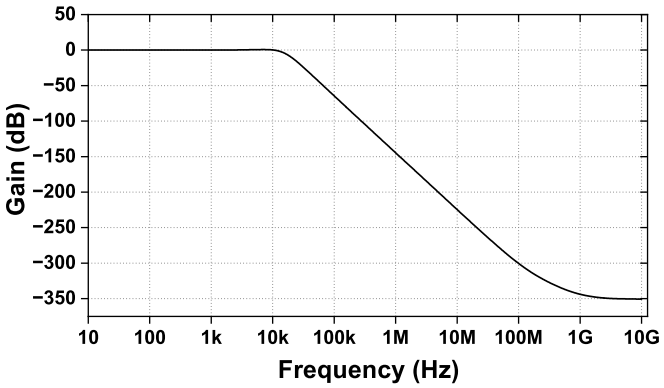


Figure 2.10: Frequency response of the filter

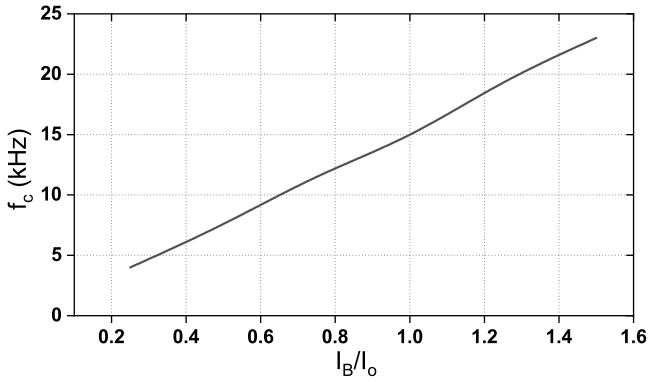


Figure 2.11: f_c variations with I_B

bias current. A THD of 1 % and 5 % are recorded for input voltages of 30 mV_p and 35 mV_p respectively.

As discussed in previous sections, the filter shows superior linearity and has a high dynamic range. To confirm this intuition, a comprehensive quantitative study on filter linearity is carried out (non-linearities in a system is discussed in detail in appendix). The filter is excited by a 1 kHz, 30 mV_p sinusoidal signal to get a THD of -40 dB (1 %) at the output. The significant harmonics in the output power spectrum is plotted as shown in Figure 2.12. Even harmonics are negligible since the filter operation is differential. The significant contributor is HD_3 which is recorded at -45 dB. The variation of THD and HD_3 with respect to input voltage for a 1 kHz sinusoidal signal is plotted and is shown in Fig. 2.13. IP_3 curves for two closely spaced tones (f_1 and f_2) are plotted in Figure 2.14 to investigate filter linearity further. Tones f_1 and f_2

are selected so that their third-order intermodulation products ($2f_1$-f_2 and $2f_2$-f_1) fall in the passband and appear close to f_1 and f_2. In this test, f_1 and f_2 are chosen as 1 kHz and 1.1 kHz respectively for 30 mV_p sinusoidal signals. The noise floor is plotted in the figure, and IMFDR$_3$ is found to be 58 dBm. Fundamental and the third order harmonics(IM$_3$) are extrapolated, and IIP$_3$ is found to be 16.1 dBm. From the linearity parameter numbers, it is evident that the filter exhibits excellent linearity.

Figure 2.15 shows the output noise spectral density of the filter and input referred

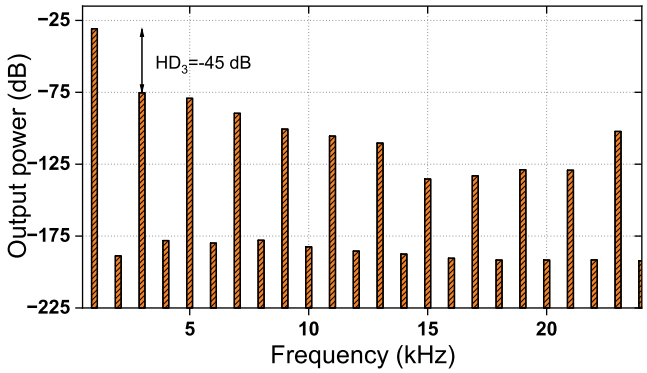


Figure 2.12: Harmonic distortion for 1 % THD

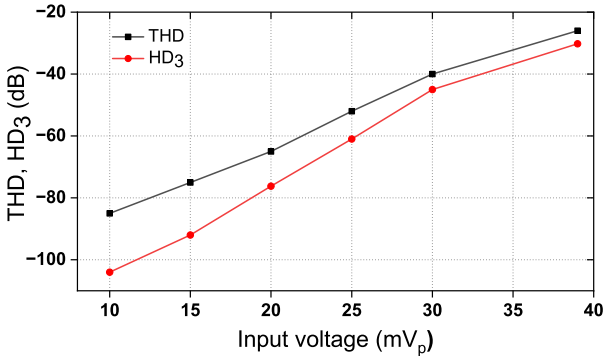


Figure 2.13: THD and HD$_3$ response

noise integrated over filter bandwidth is found to be 28 μV_{rms}. The filter's dynamic range (DR) for 1 % THD is 61 dB.

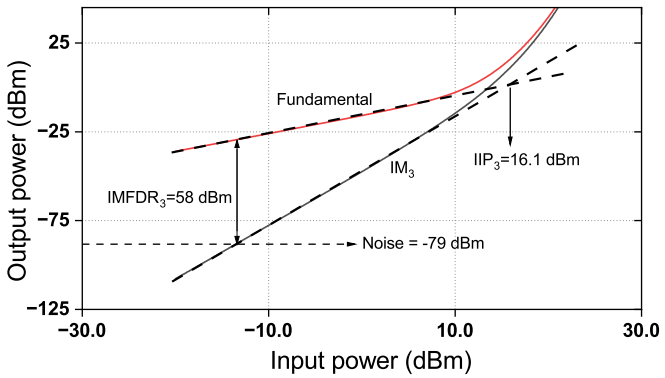


Figure 2.14: IP_3 curves

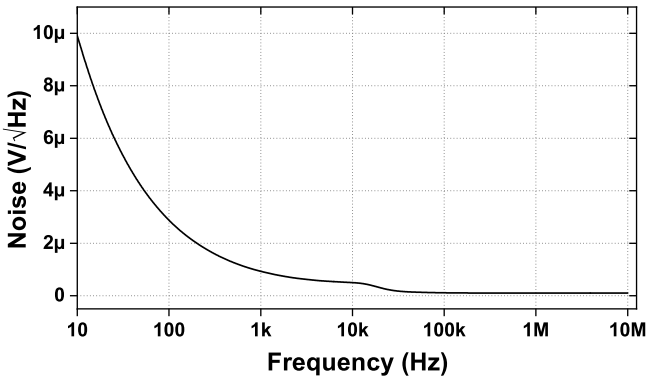


Figure 2.15: Output noise PSD of the filter

2.2.2 PVT variations and second order effects

It is essential to verify the robustness and reliability of the proposed circuit, along with its stability against PVT variations. For this, the behaviour of the filter is studied by varying the supply voltage, temperature and process corners. Simulations show that the circuit is immune to power supply variations, stable over a range of temperatures and exhibits negligible shifts in cut-off frequency (f_c) for various process corners. A 10 mV, 1 kHz sinusoidal signal is applied to the filter and variations in f_c are observed. For ±10% change in supply voltage, the filter's cut-off frequency deviates around ±6% from its ideal value. The filter shows good stability in the temperature range of 0-70^{o}C where cut-off frequency shifts within ±5%. The process corner deviation is also negligible where a maximum deviation of 6% is observed for ff corner. The summary of PVT variations is listed in Table 2.2. Monte Carlo analysis is done for

Table 2.2: Summary of PVT variations on f_c

Corners	ss	ff	snfp	fnsp
f_c (kHz)	14.2	15.9	15.85	14.3
V_{DD} (V)	0.54		0.6	0.66
f_c (kHz)	15.95		15	14.1
Temp (^{o}C)	0	27	50	70
f_c (kHz)	15.8	15	14.4	14.25

cut-off frequency against the transistor process variations and device mismatches. The histogram is plotted in Figure 2.16. Simulation is carried out for 200 runs, and mean f_c was found to be 14.8 kHz with a standard deviation of 0.9 kHz. These results imply that the proposed filter is a robust, reliable and stable solution for analog signal filtering.

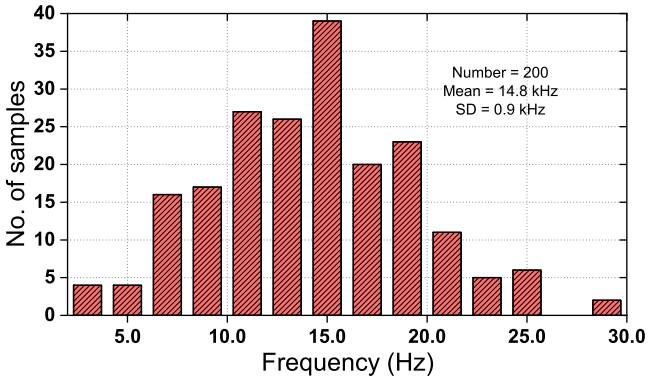


Figure 2.16: Monte Carlo analysis of f_c

2.2.3 Performance summary and comparison with state-of-the-art

A summary of the filter parameters is listed in Table 2.3. Dynamic range for 1% and 5% THD are 61 dB and 63.5 dB respectively. Since the filter is targeted for low power applications like wearable/implantable medical devices, achieving a high DR under a very low supply voltage of 0.6 V is impressive. For a bias current of 100 nA and capacitor values of 9.6 pF, the fourth order filter achieves a cut-off frequency of 15 kHz. A fair and just comparison is done with similar compact filters in the literature

and is shown in Table 2.4. The proposed circuit shows the benefits of low voltage operation, better dynamic range, circuit compactness, and flexibility in tuning. For a quantitative analysis and to prove the performance superiority of the proposed circuit, a Figure of Merit (FoM) is defined as follows.

$$FoM = \frac{P}{N \times f_c \times DR} \tag{2.30}$$

where P, N, f_c, DR are the power, order, cut-off frequency and dynamic range of the filter. The performance metrics are detailed in appendix. The FoMs of the filters mentioned in Table 2.4 are calculated as per (2.30). Lesser the FoM number, better the circuit is in terms of energy efficiency. From the FoM numbers, the proposed filter exhibits exceptional performance compared to other similar filters. Low value of FoM is achieved as a result of single branch circuit and folding techniques explored in filter design which are discussed in detail in previous sections. The filter is energy efficient, compact, easy to tune, able to operate under low voltage and can be used for low-power applications. For further ease of comparison, FoM vs. V_{DD} is also plotted and is shown in Figure 2.17. The proposed filter exhibits the lowest FoM while operating at a very low voltage.

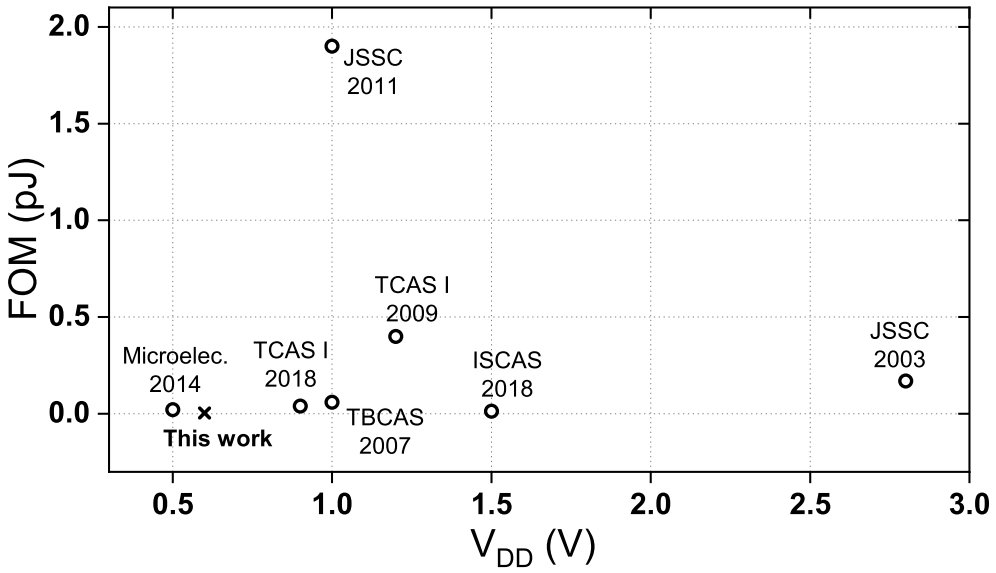


Figure 2.17: FoM vs. V_{DD}

Table 2.3: Performance summary

Fourth order low pass filter	
I_B (nA)	100
f_c (kHz)	15
DC gain (dB)	0
IRN (μV_{rms})	28
$V_{in,p}$ (mV)	30 @1 % THD; 39 @5 % THD
DR (dB)	61 @1 % THD; 63 @5 % THD
IIP_3 (dBm)	16.1
$IMFDR_3$ (dBm)	58
1 dB CP (dBm)	2.8
FoM (pJ)	0.0044

Table 2.4: Performance summary and comparison with similar filters

Ref.	Technology (μm)	Supply voltage (V)	Power (nW)	f_c (Hz)	Order	DC gain (dB)	IRN (μV_{rms})	DR @1 % THD (dB)	FoM (pJ)	Chip area (mm^2)
JSSC, 2003 Salthouse and Sarpeshkar (2003)	1.5	2.8	230	141	4	-	776	67.5	0.17	-
TBCAS, 2007 Corbishley and Rodriguez-Villegas (2007)	0.35	1	68	671	6	0	50	49	0.06	0.234
TCAS I, 2009 Tuckwell and Papavassiliou (2009)	0.18	1.2	875	3.5 k	8	-	-	37	0.4	0.11
IET, 2010 Yang *et al.* (2010)	0.18	1	14.4	732	4	-	50	55	0.0087	0.132
JSSC, 2011 Casson and Rodriguez-Villegas (2011)	0.35	1	0.06	2	7	-	51	43	1.9	0.216
Microelec., 2014 Sawigun *et al.* (2014)	0.18	0.5	2	1 k	4	-	78	47	0.022	0.0144
APCCAS, 2016 Sawigun and Pawarangkoon (2016)†	0.35	0.6	0.36	100	2	0	52	52.2	0.0044	-
ISCAS, 2018 Thanapithak and Sawigun (2018)	0.35	1.5	5.2	99	4	0.06	43.9	59.7	0.013	0.027
TCAS II, 2018 Sun and Lee (2017)	0.18	1	350	50	5	-6	194	49.9	4.4	0.12
TCAS II, 2017 De Matteis and Baschirotto (2016)	0.18	1.8	2.3 $\times 10^6$	1 G	3	-2.9	213	62.4	0.00058	-
TCAS I, 2018 Thanapitak and Sawigun (2018)	0.35	0.9	4.26	100	4	-0.05	80.5	48.2	0.04	0.11
This work‡	**0.065**	**0.6**	**300**	**15 k**	**4**	**0**	**28**	**61**	**0.0044**	**0.085**

†schematic simulation; ‡post layout simulation ; rest are measured results

2.3 Summary

A novel folded single branch biquad is proposed in this chapter and its application to a fourth order low pass filter is demonstrated. The filter is highly compact and power efficient, has high dynamic range, and shows better flexibility in tuning due to its folded nature. The stability of the circuit over PVT variations shows the robustness of the design. The filter shows superior performance when compared to similar filters and this is validated by the FOM numbers. This filter is an appealing choice for low voltage, high dynamic range applications that require flexible tuning, such as medical imaging systems.

An entirely different approach of designing continuous time filters is the filter design in log domain. When the transistors are operating in sub-threshold region, an exponential relationship exists between the output current and input voltage. This feature can be exploited to design filter circuits and the same is adopted in the filter explained in the next chapter.

Chapter 3

LOG DOMAIN FILTER

This chapter presents a CT LPF using log companding technique discussed in chapter 1. The general block diagram of a log-domain filtering setup is shown in Figure 3.1. The system is internally non-linear, but externally linear. To illustrate how this idea can be explored in filter design, a basic RC circuit is used and translated into log domain using diodes.

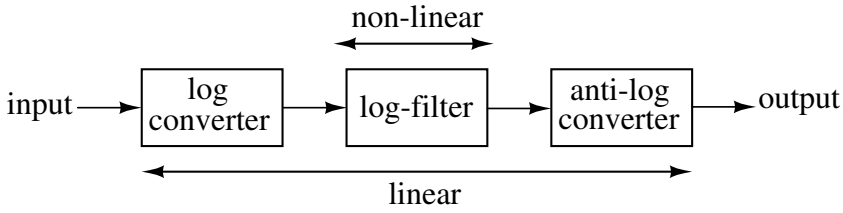


Figure 3.1: Concept of log domain filter

3.1 Log domain conversion using diodes

The first order RC LPF is shown in Figure 3.2. The differential equation of this filter is

$$V_o + RC.V_o^{'} = V_{in} \tag{3.1}$$

where V_{in} and V_o are the inputs and outputs of the filter, respectively. $V_o^{'}$ represents the first order time derivative of V_o. To convert this into log domain, Adams (1979) suggested the circuit as shown in Figure 3.3. Log and anti-log converters are also shown in Figure 3.4.

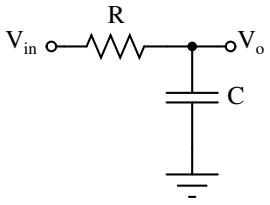


Figure 3.2: RC LPF

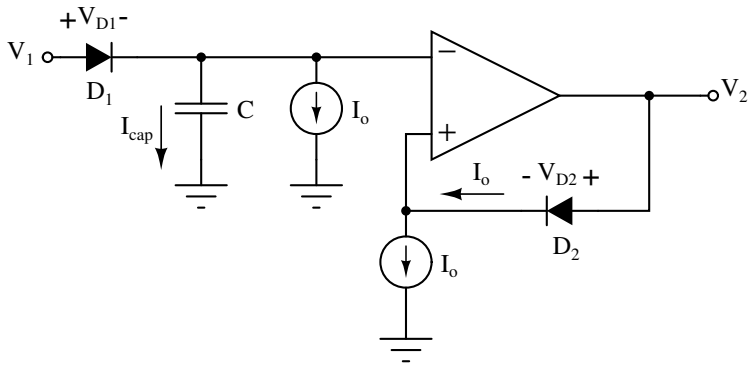


Figure 3.3: Corresponding log-filter

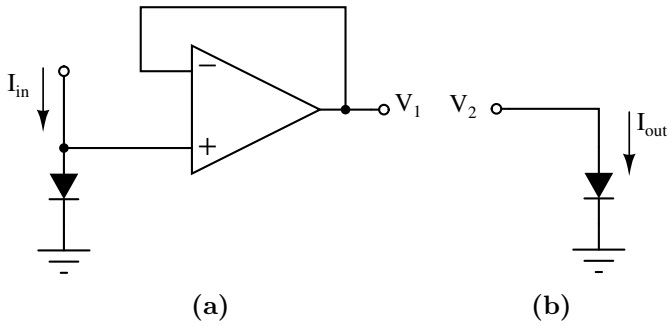


Figure 3.4: (a) log converter (b) anti-log converter

Figure 3.3 can be seen as a counterpart of RC LPF where the resistor is replaced by diode D_1. The remaining parts of the circuit work as a level shifter to compensate for the diode drop of D_1. Applying KCL at capacitor node,

$$I_{cap} = I_{D1} - I_o \tag{3.2}$$

Capacitor current (I_{cap}) is written as,

$$I_{cap} = C\frac{d}{dt}(V_2 - V_{D2}) = C\frac{d}{dt}V_2 \tag{3.3}$$

V_{D2} is a constant voltage drop across diode D_2 due to bias current I_o, and it is time-invariant so that its derivative is zero. It is given by,

$$V_{D2} = V_T \cdot ln(\frac{I_o}{I_s}) \tag{3.4}$$

where I_s and V_T are diode saturation current and thermal voltage, respectively. The current through diode D_1 can be written as,

$$I_{D1} = I_s \cdot e^{V_{D1}/V_T} \tag{3.5}$$

(3.5) can be written as

$$I_{D1} = I_s \cdot e^{\frac{[V_1-(V_2-V_{D2})]}{V_T}} = I_s \cdot e^{\frac{V_1-V_2}{V_T}} \cdot e^{\frac{V_{D2}}{V_T}} \tag{3.6}$$

Substituting (3.4) in (3.6), we get

$$I_{D1} = I_o \cdot e^{\frac{V_1-V_2}{V_T}} \tag{3.7}$$

Substituting (3.7) and (3.3) in (3.2), we can arrive at

$$C\frac{d}{dt}V_2 = I_o \cdot e^{\frac{V_1-V_2}{V_T}} - I_o \tag{3.8}$$

Multiply both sides by $e^{\frac{V_2}{V_T}}$ and rearranging terms, we get

$$I_o \cdot e^{\frac{V_2}{V_T}} + e^{\frac{V_2}{V_T}} \cdot C\frac{d}{dt}V_2 = I_o \cdot e^{\frac{V_2}{V_T}} \tag{3.9}$$

Further simplifying and multiplying both sides by I_s, we get

$$I_s \cdot e^{\frac{V_2}{V_T}} + \frac{V_T C}{I_o} \cdot \frac{d}{dt}\left[I_s \cdot e^{\frac{V_2}{V_T}}\right] = I_s \cdot e^{\frac{V_1}{V_T}} \tag{3.10}$$

We can write input and output currents as follows.

$$I_{in} = I_s \cdot e^{\frac{V_1}{V_T}} \qquad and \qquad I_{out} = I_s \cdot e^{\frac{V_2}{V_T}} \tag{3.11}$$

Thus (3.10) can be written as

$$I_{out} + \frac{V_T C}{I_o} \cdot I_{out}{}' = I_{in} \tag{3.12}$$

(3.12) is in the form of (3.1) and represents an LPF function. The above analysis used a diode based log-domain conversion. This chapter explores log-domain filter design using MOSFETs and is discussed in the subsequent sections along with the detailed mathematical analysis.

3.2 Filter realization using MOSFETs

In this section, we try to realize LPF function using MOSFETs biased in weak inversion region. The transfer function of a first order LPF is

$$H(s) = \frac{Y(s)}{X(s)} = \frac{\omega_o}{s + \omega_o} \tag{3.13}$$

where ω_o is the cut-off frequency of the filter. The corresponding time domain differential equation is given by

$$\frac{dY(t)}{dt} + \omega_o Y(t) = \omega_o X(t) \tag{3.14}$$

where X(t) and Y(t) are input and output of the filter respectively. Since log-domain filters are current mode circuits, input and output are mapped to current quantities as given below.

$$X(t) = I_{in} = I_o \exp\left(\frac{V_{in}}{\eta V_T}\right) \tag{3.15}$$

$$Y(t) = I_{out} = I_o \exp\left(\frac{V_{out}}{\eta V_T}\right) \tag{3.16}$$

where I_{out} and I_{in} consist of DC as well as signal components. The time derivative of the output $Y(t)$ is given by

$$\frac{dY(t)}{dt} = \frac{I_o \exp\left(\frac{V_{out}}{\eta V_T}\right)}{\eta V_T} \frac{dV_{out}}{dt} \tag{3.17}$$

Substituting (3.16), (3.15) and (3.17) in (3.14) gives

$$\frac{\exp\left(\frac{V_{out}}{\eta V_T}\right)}{\eta V_T} \frac{dV_{out}}{dt} + \omega_o \exp\left(\frac{V_{out}}{\eta V_T}\right) = \omega_o \exp\left(\frac{V_{in}}{\eta V_T}\right) \tag{3.18}$$

Multiplying both sides by capacitance C gives

$$C\frac{dV_{out}}{dt} + \omega_o C \eta V_T = \omega_o C \eta V_T \exp\left(\frac{V_{in} - V_{out}}{\eta V_T}\right) \tag{3.19}$$

Substituting $\omega_o C \eta V_T$ as I_{dc} yields

$$C\frac{dV_{out}}{dt} + I_{dc} = I_{dc} \exp\left(\frac{V_{in} - V_{out}}{\eta V_T}\right) \tag{3.20}$$

where I_{dc} can be obtained from a MOSFET as follows

$$I_{dc} = I_o \exp\left(\frac{V_{dc}}{\eta V_T}\right) \tag{3.21}$$

$$\therefore C\frac{dV_{out}}{dt} + I_o \exp\left(\frac{V_{dc}}{\eta V_T}\right) = I_o \exp\left(\frac{V_{dc} + V_{in} - V_{out}}{\eta V_T}\right) \tag{3.22}$$

(3.22) can be interpreted as

$$I_C + I_{dc} = I_K \tag{3.23}$$

where I_K consists of DC current and the capacitor current I_C.

$$I_K = I_o \exp\left(\frac{V_{dc} + V_{in} - V_{out}}{\eta V_T}\right) = I_o \exp\left(\frac{V_K}{\eta V_T}\right) \tag{3.24}$$

The voltage V_K is related to V_{in} and V_{out} as follows

$$V_K + V_{out} = V_{dc} + V_{in} \tag{3.25}$$

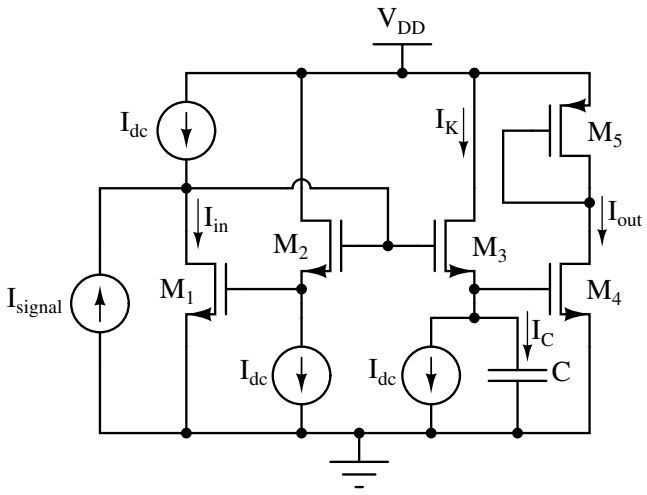


Figure 3.5: First order log-domain cell

Rewriting above equation in terms of current quantities gives

$$I_K I_{out} = I_{dc} I_{in} \tag{3.26}$$

Equation (3.26) is of the form of (1.18) and hence can be realized using four transistors forming a translinear loop. The first order filter is designed using the KCL equation (3.23) and the translinear equation (3.26). These equations can be implemented in the form of a translinear circuit as shown in Figure 3.5. In this design, the MOSFETs M_1–M_4 form the translinear loop. The DC current sources are adjusted to ensure operation of transistors in sub-threshold region. The signal current (I_{signal}) is added to the DC current (I_{dc}) to ensure that the input current (I_{in}) passing through transistor M_1 is always positive. This input current is compressed to voltage V_{in} at the gate of M_1 according to (3.15). Since the DC currents flowing through transistors M_2 and M_3 are equal, the gate-source voltages of these transistors are also equal. The transistor M_2 acts as a level shifter causing current I_k to flow through M_3. The signal component of I_k which is I_C, flows through the capacitor C. The capacitor performs the integrating operation and generates a voltage V_{out} at the gate of transistor M_4. This voltage is expanded to get the output current I_{out}. The cut-off frequency of the filter can be tuned by varying the DC current and is given by following (Mulder *et al.* 2012).

$$f_c = \frac{I_{dc}}{2\pi\eta V_T C} \tag{3.27}$$

Table 3.1: Size of transistors in Figure 3.6

Transistors	W/L (μm/μm)
M_{1-8}	1/0.4
M_{9-29}	5/1

For instance, to build a first order cell having cut-off frequency of 1 kHz and a bias current of 5 nA, from (3.27), the capacitor value can be calculated and is approximately equal to 12 pF. A second-order filter is realised by cascading two first order cells discussed above and is shown in Figure 3.6. Transistors M_{1-4} and M_{5-8} form the second-order translinear loop for the first and second stages of the filter respectively. For better current mirroring accuracy, cascode current mirrors are used. The sizes of all transistors used are given in Table 3.1.

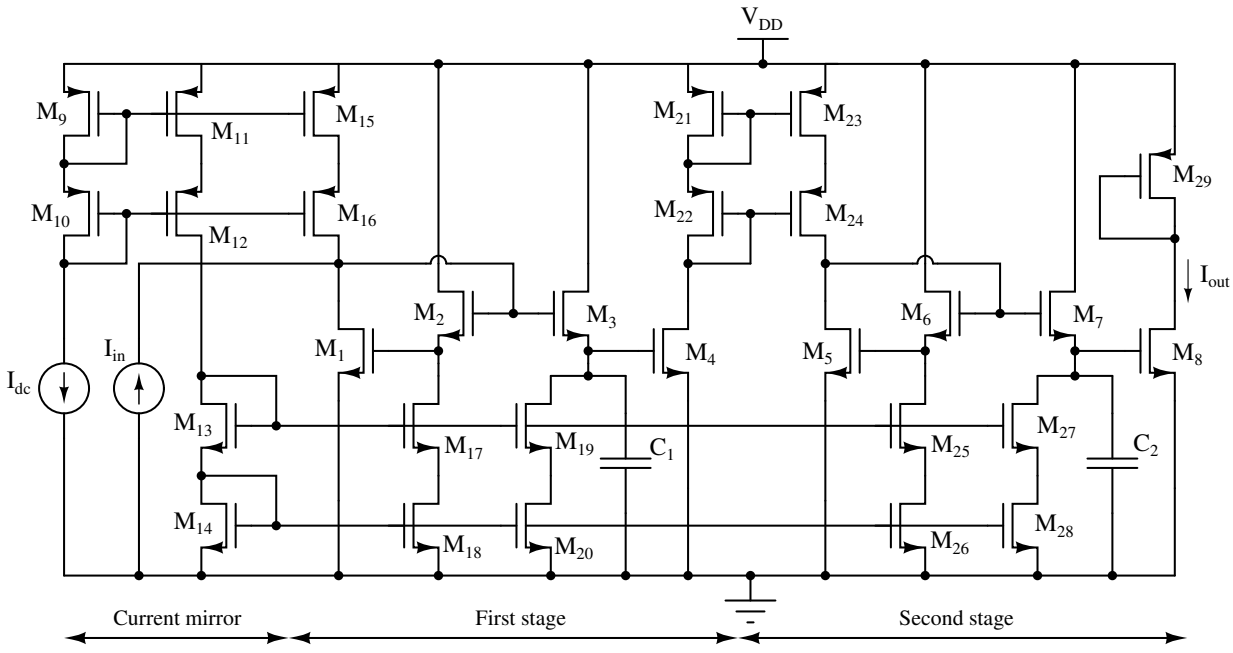


Figure 3.6: Second order log-domain filter

3.3 Post layout simulation results

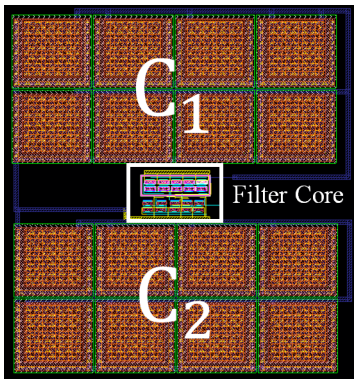


Figure 3.7: Layout of the filter

The layout of the filter is shown in Figure 3.7. The circuit consumes a layout area of 176 μm $\times$ 187 μm with an active area of 34 μm $\times$ 25 μm. The enlarged active area is shown in Figure 3.8. The circuit operates at a supply voltage of 0.9 V and a bias current (I_B) of 5 nA. The filter consumes a power as low as 55 nW. The frequency response of the second order filter is shown in Figure 3.9. For a cut-off frequency of 1 kHz, capacitors C_1 and C_2 are chosen as 12 pF.

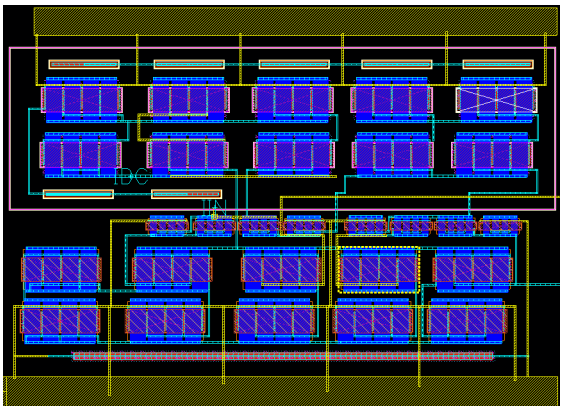


Figure 3.8: Enlarged view of active area

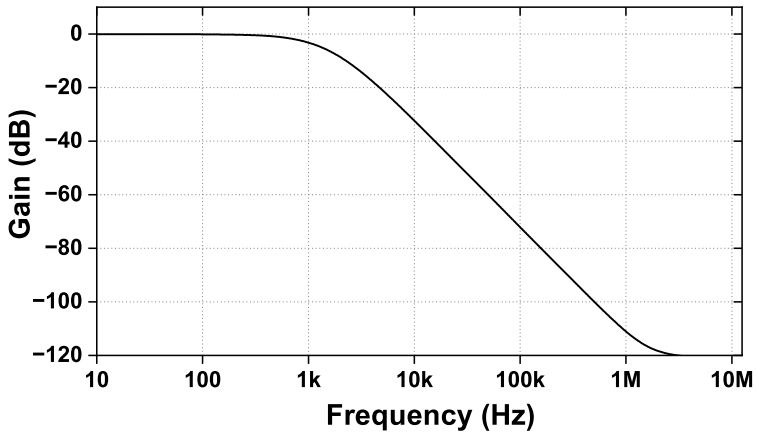


Figure 3.9: Frequency response of second order filter

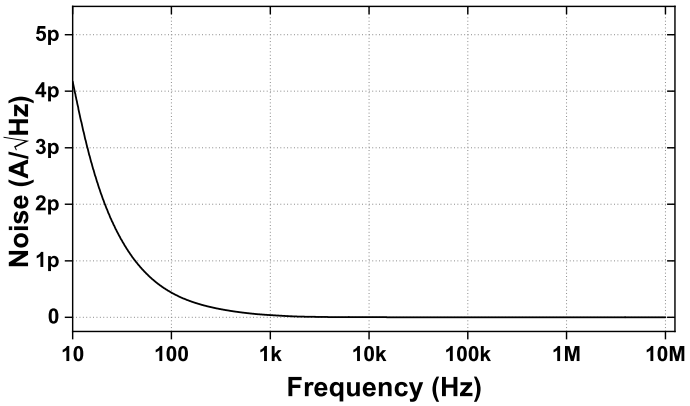


Figure 3.10: Output noise PSD

The output noise spectral density of the filter is shown in Figure 3.10. The integrated noise over the passband is calculated and found to be 6.5 pA_{rms}. Since the pass band gain is unity, this is equated to the IRN of the filter. Figure 3.11 shows the variation of filter response against supply voltage changes. For ± 10 % change in V_{DD}, the maximum variation in f_c is within 2%. Filter shows good stability in the temperature range of 0-70^o where the deviation of f_c is within 2%. This is shown in Figure 3.12. Figure 3.13 shows the filter response for various process corners. The filter shows a maximum deviation of 4 % in f_c for ss and ff corners. To check the robustness of the design, Monte carlo analysis is carried out. Simulations are done for 200 runs against process variations and device mismatches. The mean f_c was found

to be 0.93 kHz with a standard deviation of 350 Hz. Histogram is shown in Figure 3.14.

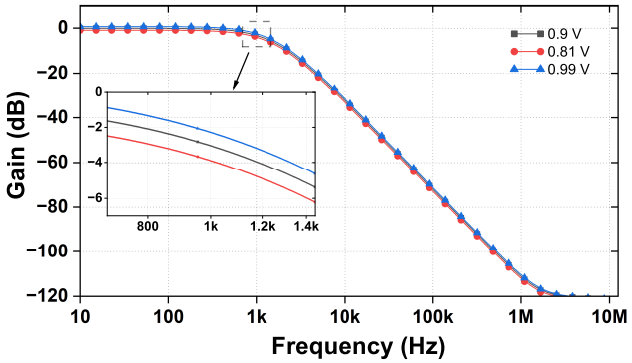


Figure 3.11: Filter response against V_{DD} variations

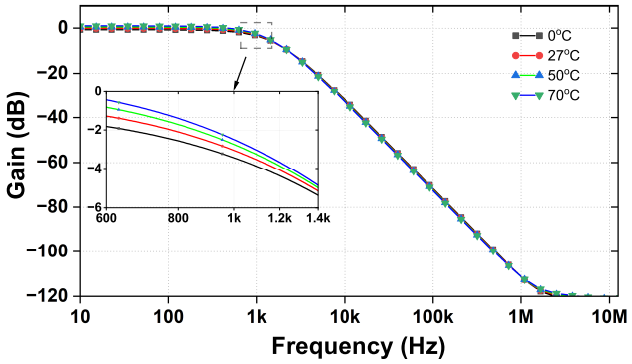


Figure 3.12: Filter response against temperature variations

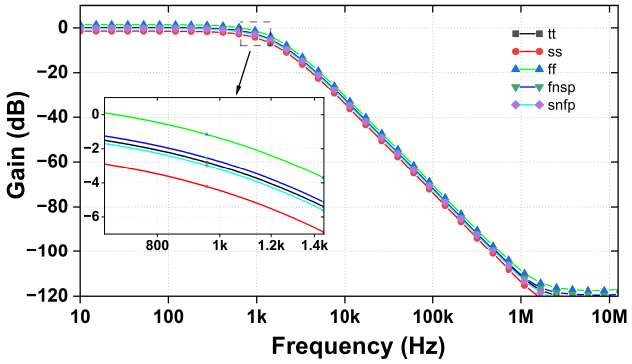


Figure 3.13: Filter response for various process corners

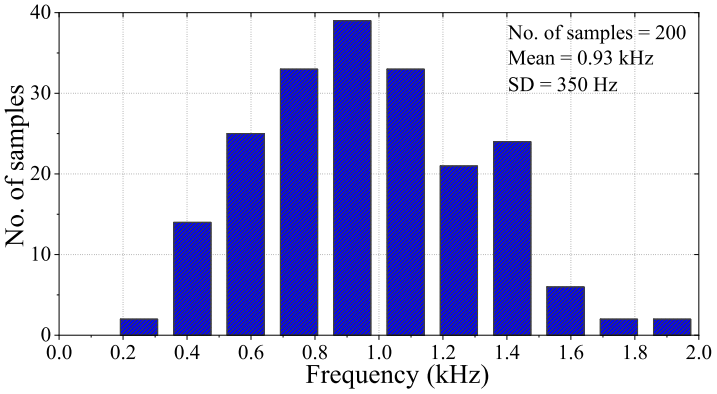


Figure 3.14: Monte Carlo analysis of f_c

3.4 Performance summary and comparison with literature

Table 3.2: Parameters of the filter

Topology	Current mode Translinear
Technology	65 nm CMOS
V_{DD}	0.9 V
f_c	1 kHz
DC gain	0 dB
Power	55 nW
I_{inpp} @ 250 Hz for 1 % THD	4.1 nA
Input referred noise†	6.5 pA_{rms}
Dynamic range	56 dB

†integrated from 1 Hz - 1 kHz

The filter parameters are summarised in Table 3.2. A performance comparison of the designed filter with other similar works found in literature is listed in Table 3.3. FoM in Table 3.3 is calculated as follows (Rekha and Laxminidhi 2013).

$$FoM = \frac{Power}{Order \times DR^2} \tag{3.28}$$

The FoM of the designed filter is found to be as low as 0.069 pJ, which indicates that the design is energy efficient when compared to other similar works. The proposed

filter offers very low power consumption and a dynamic range which is comparable or even superior to many of similar filters while operating under 0.9 V supply voltage.

Table 3.3: Performance summary and comparison with other similar works

Ref.	Technology (μm)	Supply voltage (V)	Cut-off frequency (kHz)	Order	Dynamic range (dB)	Power (nW)	FoM (10^{-12}J)
Ngarmnil and Toumazou (1995)	0.8	±2.5	2.7	2	60	1000	0.5
El-Masry and Wu (1999)	1.2	1	10	2	-	254	-
Python *et al.* (1999)	0.5	1	100	5	55	4500	2.8
Jain and Singh (2016)	0.35	±0.5	85	1	-	2620	-
Serra-Graells and Huertas (2005)	1.2	1	10	2	72	20,000	0.63
Punzenberger and Enz (1998)	1	1.2	320	3	57	23,000	15.2
This work	**0.065**	**0.9**	**1**	**2**	**56**	**0.055**	0.069

3.5 Summary

A second order current mode translinear filter is proposed in this chapter. A second order dynamic translinear loop is the core of the filter. The circuit operates at 0.9 V supply and consumes 55 nW of power. The power consumption is considerably low due to the use of MOSFETs in sub-threshold region. This proves the advantage of log-domain filters over other conventional filter configurations such as Gm-C, active-RC, OTA-C or MOSFET-C. This type of filter is internally non-linear while showing an external linear behaviour. A dynamic range of 56 dB and a FoM of 0.069 pJ imply a good overall performance of the filter. The low-power consumption of the filter makes it a good choice for biomedical data acquisition systems.

The design of RMS-DC converter, a non-linear application of dynamic translinear principle, is explained in the next chapter.

Chapter 4

TRANSLINEAR RMS-DC CONVERTER

This chapter presents a novel approach towards the design of a current-mode RMS-DC converter based on the dynamic translinear principle. The circuit is designed using a third-order translinear loop employing MOS transistors operating in the weak inverted saturation region. Hence, the designed circuit offers the benefits of low power consumption and reduced circuit complexity. The translinear nature of the circuit allows it to handle currents larger than the bias current of the circuit.

A current-mode RMS-DC converter can be described by

$$I_{out} = \sqrt{\left\langle {i_{in}}^2 \right\rangle} \tag{4.1}$$

where i_{in} and I_{out} are the input and output currents of the RMS-DC converter, and $\langle ... \rangle$ represents the time averaging operation, i.e., a low-pass filter. A mathematically equivalent equation is given by

$$I_{out} = \left\langle \frac{{i_{in}}^2}{I_{out}} \right\rangle \tag{4.2}$$

Figure 4.1 shows the equivalent block diagram of a conventional implicit RMS-DC converter (Mulder *et al.* 1997).

The implicit realization of RMS-DC converter consists of two functional blocks, a squarer-divider and a low-pass filter. The squarer-divider circuit can be realised using the static translinear principle. The low-pass filter can be realised in the log-domain using the dynamic translinear principle. Both these functions can be implemented

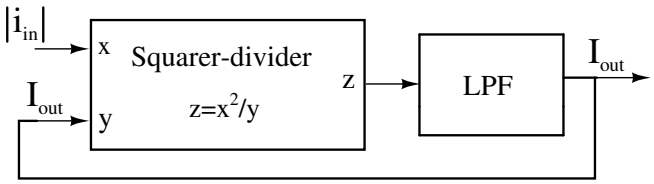


Figure 4.1: Block diagram of conventional implicit RMS-DC converter

using MOS transistors operating in the sub-threshold region.

4.1 Circuit realization

In this work, both the squarer-divider and the low-pass filter are implemented using a single translinear loop. This means that, the drawbacks of cascading those two blocks to realize an implicit RMS-DC converter can be eliminated. This was discussed in detail in chapter 1. But, in order to implement the circuit using a single translinear loop, it is essential to arrive at a differential equation representing a current-mode RMS-DC converter.

The differential equation of a current-mode first order low-pass filter having a cut-off frequency of ω_o is given by

$$\frac{dI_{of}}{dt} + \omega_o I_{of} = \omega_o I_{if} \tag{4.3}$$

where, I_{if} and I_{of} are the input and output currents of the filter, respectively. If the filter is realised in the log-domain then the cut-off frequency (ω_o) of the filter is given by

$$\omega_o = \frac{I_B}{C\,\eta\,V_T} \tag{4.4}$$

where I_B is the bias current of the filter, C is the capacitor, η is the sub-threshold slope coefficient and V_T is the thermal voltage. Note that the cut-off frequency ω_o is inversely proportional to absolute temperature.

In an RMS-DC circuit, the input current to the low-pass filter is the output current of the squarer-divider, as shown in Figure 4.1. Thus, in an RMS-DC circuit, the input current to the filter is $|i_{in}|^2/I_{out}$, and the output current of the filter is I_{out}.

$$\therefore \qquad I_{if} = \frac{|i_{in}|^2}{I_{out}}, \quad I_{of} = I_{out} \tag{4.5}$$

Substituting (4.5) in (4.3) gives the differential equation representing a current-mode RMS-DC converter.

$$I_{out}\frac{dI_{out}}{dt} + \omega_o {I_{out}}^2 = \omega_o |i_{in}|^2 \tag{4.6}$$

(4.6) is a non-linear differential equation. Thus, RMS-DC converter demonstrates the application of the dynamic translinear principle to the implementation of non-linear differential equations. In order to implement (4.6) in the translinear domain, the derivative term in the equation is eliminated by introducing a capacitor current i_c, as shown in Figure 4.2.

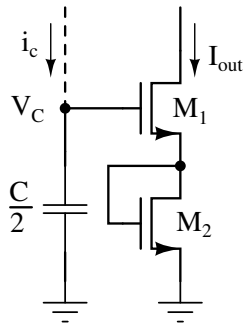


Figure 4.2: Sub-circuit of RMS-DC converter introducing i_c

Using the dynamic translinear principle, the relation between i_c and I_{out} in Figure 4.2 is given by

$$\frac{dI_{out}}{dt} = \frac{i_c \cdot I_{out}}{C\,\eta\,V_T} \tag{4.7}$$

Substituting (4.7) and (4.4) in (4.6) results in a current-mode polynomial representing an RMS-DC converter.

$$|i_{in}|^2 \,.\, I_B = (i_c + I_B) \,.\, {I_{out}}^2 \tag{4.8}$$

(4.8) can be implemented in the form of a translinear loop using six MOS transistors, as shown in Figure 4.3. Transistors $M_1 - M_6$ form the translinear loop.

The input to the RMS-DC converter is the full-wave rectified version of the input current signal. The full-wave rectified input signal is obtained using a simple absolute-value circuit proposed by Chang and Liu (2000). The absolute-value circuit is shown in Figure 4.4.

The complete circuit of the RMS-DC converter including the absolute-value circuit and the bias circuit is shown in Figure 4.5. The bias circuit mirrors the bias current (I_B) to the transistors M_{12} and M_{13}. The PMOS current mirror, using transistors

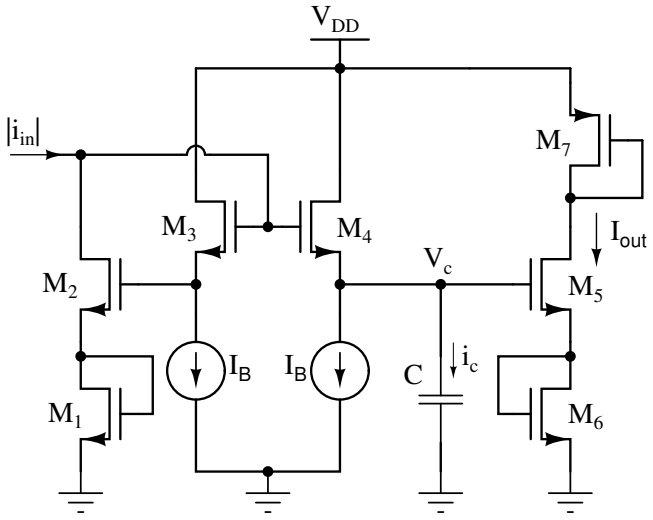


Figure 4.3: Proposed RMS-DC converter

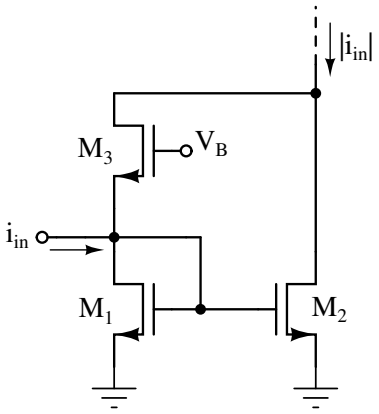


Figure 4.4: Absolute-value circuit

M_{10} and M_{11}, mirrors the full-wave rectified input current ($|i_{in}|$) to the RMS-DC converter. In Figure 4.5, the transistor M_{13} acts as a DC current source of value I_B. The transistors M_4, M_{13} and the capacitor C act as a source follower circuit. A source follower circuit resembles the characteristics of a first order low-pass filter (Rao and Rekha 2020). The cut-off frequency of this source follower low pass filter is given by

$$\omega_c = \frac{g_{m4}}{C} \tag{4.9}$$

where g_{m4} is the transconductance of the transistor M_4. Since M_4 operates in the

sub-threshold region, the transconductance of M_4 is given by

$$g_{m4} = \frac{I_B}{\eta\, V_T} \tag{4.10}$$

$$\therefore \quad \omega_c = \frac{I_B}{C\,\eta\, V_T} \implies f_c = \frac{I_B}{2\pi\, C\,\eta\, V_T} \tag{4.11}$$

The sizes of all transistors used are given in Table 4.1.

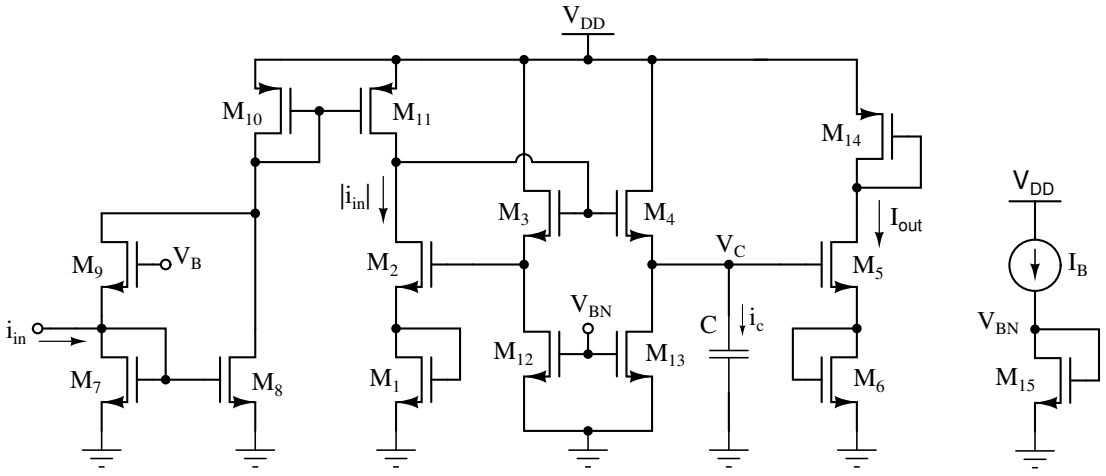


Figure 4.5: Proposed RMS-DC converter with absolute value and bias circuits

Table 4.1: Size of transistors in Figure 4.5

Transistors	W/L (μm/μm)
M_1, M_6	10/3
M_{2-5}	4/3
M_7, M_8	3.5/3
M_9	3/3
M_{10-15}	10/3

4.2 Mathematical analysis

The analysis of the proposed RMS-DC converter is done in the following section. Let the input current of the RMS-DC converter be

$$i_{in} = I_p.\sin(\omega.t) \tag{4.12}$$

The main objective of this section is to prove that the output of the proposed RMS-DC converter is the RMS value of i_{in}. i.e., to prove that

$$I_{out} = \frac{I_p}{\sqrt{2}} \tag{4.13}$$

The current-mode translinear equation representing the RMS-DC converter is given by

$$|i_{in}|^2 \cdot I_B = (I_B + i_c) \cdot {I_{out}}^2 \tag{4.14}$$

The voltage across the capacitor C shown in Figure 4.5 is

$$V_c = V_{gs5} + V_{gs6} \tag{4.15}$$

where V_{gs} is the gate-source voltage of the sub-threshold operated transistor. The gate-source voltage of the transistor is related to its drain current by

$$V_{gs} = \eta\, V_T\, ln\left(\frac{I_D}{I_S}\right) + V_{th} \tag{4.16}$$

where V_{th} is the threshold voltage of the transistor. Since transistors M_5 and M_6 carry the same current I_{out}, their gate to source voltages are equal i.e, $V_{gs5} = V_{gs6}$.

$$\therefore V_c = 2\,\eta\, V_T\, ln\left(\frac{I_{out}}{I_S}\right) + 2\, V_{th} \tag{4.17}$$

Differentiating both sides of (4.17) gives

$$\frac{dV_c}{dt} = \frac{2\,\eta\, V_T}{I_{out}} \cdot \frac{dI_{out}}{dt} \tag{4.18}$$

The voltage across the capacitor V_c and the capacitor current i_c is related by

$$i_c = C \cdot \frac{dV_c}{dt} \tag{4.19}$$

Substituting (4.18) in (4.19) gives

$$i_c = C \cdot \frac{2\,\eta\, V_T}{I_{out}} \cdot \frac{dI_{out}}{dt} \tag{4.20}$$

Therefore, (4.14) can be written as

$$|i_{in}|^2 \cdot I_B = \left(I_B + C \cdot \frac{2\,\eta\,V_T}{I_{out}} \cdot \frac{dI_{out}}{dt} \right) \cdot {I_{out}}^2 \tag{4.21}$$

To simplify the above differential equation, we make a substitution as given below

$$y = {I_{out}}^2 \tag{4.22}$$

$$\frac{dy}{dt} = 2 \cdot I_{out} \cdot \frac{dI_{out}}{dt} \tag{4.23}$$

$$\therefore \frac{1}{y} \cdot \frac{dy}{dt} = \frac{2}{I_{out}} \cdot \frac{dI_{out}}{dt} \tag{4.24}$$

Substituting (4.22) and (4.24) in (4.21) gives

$$|i_{in}|^2 \cdot I_B = \left(I_B + \frac{C\,\eta\,V_T}{y} \cdot \frac{dy}{dt} \right) \cdot y \tag{4.25}$$

$$\therefore |i_{in}|^2 \cdot I_B = y \cdot I_B + C\,\eta\,V_T \cdot \frac{dy}{dt} \tag{4.26}$$

$$\frac{dy}{dt} + \frac{I_B}{C\,\eta\,V_T} \cdot y = \frac{I_B}{C\,\eta\,V_T} \cdot |i_{in}|^2 \tag{4.27}$$

Substituting (4.11) in (4.27) gives

$$\frac{dy}{dt} + \omega_c\, y = \omega_c\ |i_{in}|^2 \tag{4.28}$$

Equation (4.28) is the general form of a first order linear differential equation and can be solved by finding out the complementary function and the integrating factor. The integrating factor (IF) is given by

$$IF = e^{\int \omega_c\, dt} = e^{\omega_c\, t} \tag{4.29}$$

Multiplying both sides of (4.28) by IF and integrating

$$\int \left(e^{\omega_c\, t} \cdot \frac{dy}{dt} + \omega_c \cdot e^{\omega_c\, t} y \right) \cdot dt = \omega_c \int e^{\omega_c\, t} \cdot |i_{in}|^2 \cdot dt \tag{4.30}$$

Substitute

$$f = e^{\omega_c\, t} \cdot y \tag{4.31}$$

Differentiating (4.31) gives

$$\frac{df}{dt} = e^{\omega_c t} \cdot \frac{dy}{dt} + \omega_c \cdot e^{\omega_c t} \cdot y \tag{4.32}$$

Integrating both sides of (4.32) gives

$$f = \int \left(e^{\omega_c \cdot t} \cdot \frac{dy}{dt} + \omega_c \cdot e^{\omega_c t} \cdot y \right) dt = e^{\omega_c t} \cdot y \tag{4.33}$$

Substituting (4.33) in (4.30) gives

$$e^{\omega_c . t} \cdot y = \omega_c \int e^{\omega_c . t} \cdot |i_{in}|^2 \cdot dt \tag{4.34}$$

For sinusoidal input current, $i_{in} = I_p \cdot \sin(\omega\, t)$, the integral on the RHS of (4.34) evaluates to

$$\begin{aligned} \int e^{\omega_c t} \cdot |i_{in}|^2 \, dt = {} & \frac{-{I_p}^2 \cdot e^{\omega_c t} \cdot 2\,\omega_c \cdot \omega \cdot \sin(2\omega t)}{2\,\omega_c\,(4\,\omega^2 + {\omega_c}^2)} + \\ & \frac{{I_p}^2 \cdot e^{\omega_c t} \cdot 4\,\omega^2}{2\,\omega_c\,(4\,\omega^2 + {\omega_c}^2)} + \frac{{I_p}^2 \cdot e^{\omega_c t} \cdot {\omega_c}^2}{2\,\omega_c\,(4\,\omega^2 + {\omega_c}^2)} - \\ & \frac{{I_p}^2 \cdot e^{\omega_c t} \cdot {\omega_c}^2 \cdot \cos(2\omega t)}{2\,\omega_c\,(4\,\omega^2 + {\omega_c}^2)} \end{aligned} \tag{4.35}$$

At room temperature, with $I_B = 5\,\text{nA}$ and $C = 10\,\text{nF}$, the cut-off frequency (f_c) of the source follower, formed by transistors M_4, M_{13} and capacitor C, is found to be 2.18 Hz. The frequency of the input signal current in this analysis is 1 kHz. Thus, it is found that $\omega >> \omega_c$. $\therefore\ (4\,\omega^2 + {\omega_c}^2) \approx 4\,\omega^2$. Thus, (4.35) can be simplified as

$$\begin{aligned} \int e^{\omega_c t} \cdot |i_{in}|^2 \, dt \ = {} & \frac{-{I_p}^2 \cdot e^{\omega_c t} \cdot \omega \cdot \sin(2\omega t)}{4\omega^2} + \\ & \frac{{I_p}^2 \cdot e^{\omega_c t}}{2\,\omega_c} + \frac{{I_p}^2 \cdot e^{\omega_c t} \cdot \omega_c}{8\,\omega^2} - \\ & \frac{{I_p}^2 \cdot e^{\omega_c t} \cdot \omega_c \cdot \cos(2\omega t)}{8\,\omega^2} \end{aligned} \tag{4.36}$$

Since the input signal frequency (ω) is large, terms containing ω^2 in denominator of (4.36) can be neglected. Therefore, (4.36) can be further simplified as

$$\int e^{\omega_c t} \cdot |i_{in}|^2 \, dt = \frac{{I_p}^2 \cdot e^{\omega_c t}}{2\,\omega_c} \tag{4.37}$$

Hence, (4.34) can be solved as

$$e^{\omega_c t} \cdot y = \omega_c \cdot \frac{{I_p}^2 \cdot e^{\omega_c t}}{2\,\omega_c} \implies y = \frac{{I_p}^2}{2} \tag{4.38}$$

Substituting $y = {I_{out}}^2$ in (4.38) gives

$${I_{out}}^2 = \frac{{I_p}^2}{2} \quad i.e., \quad I_{out} = \frac{I_p}{\sqrt{2}} \tag{4.39}$$

(4.39) shows that the output current of the RMS-DC converter (I_{out}) is equal to the RMS value of the input current (i_{in}). The analysis was done based on the approximations done due to large input frequency. This defines the bandwidth of the circuit for accepted error in the output RMS values. Bandwidth of the circuit is discussed in the following sections.

4.3 Post layout simulation results

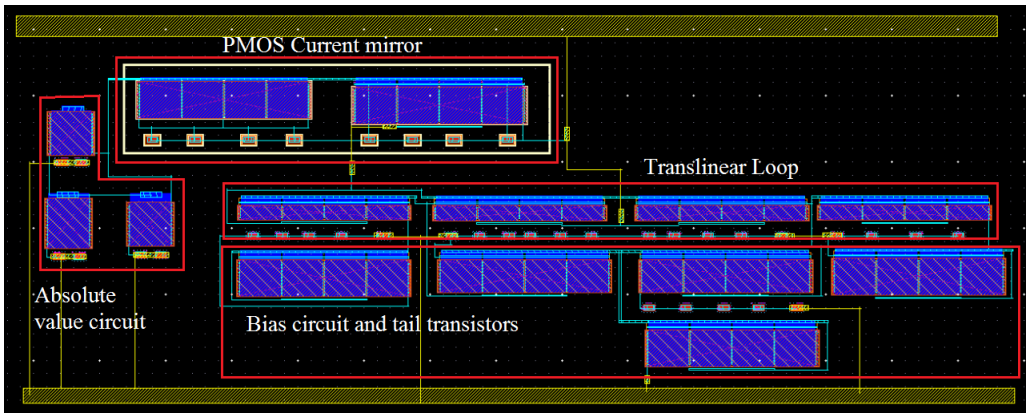


Figure 4.6: Layout of proposed RMS-DC converter

The proposed RMS-DC converter shown in Figure 4.5 is designed in UMC 65 nm CMOS technology and post layout simulations are carried out. The layout is shown

in Figure 4.6. The circuit consumes a layout area of 74 μm $\times$ 29 μm. The circuit operates at a supply voltage of 1 V and a bias current (I_B) of 5 nA. The bias voltage V_B for the absolute value circuit is fixed at 200 mV. The off-chip averaging capacitance is chosen to be 10 nF.

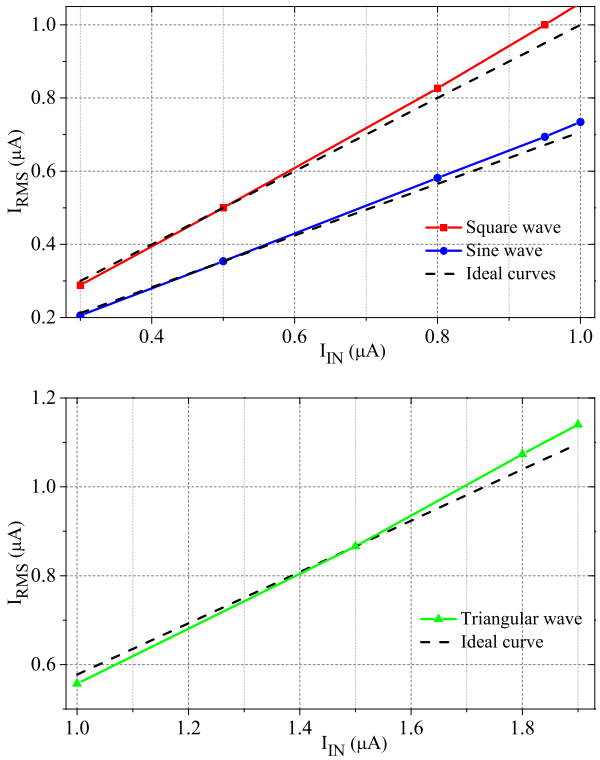


Figure 4.7: Characteristics of the proposed RMS to DC converter for sinusoidal, bipolar square and triangular waveforms

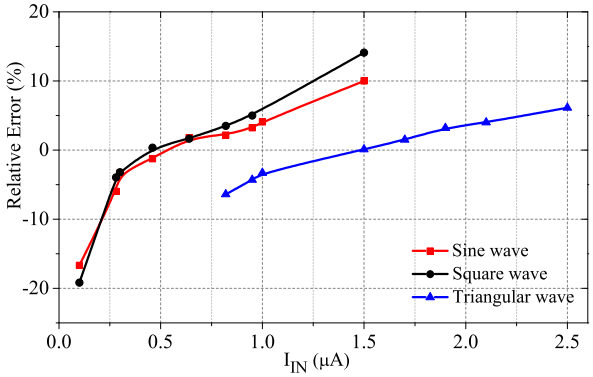


Figure 4.8: Relative error for sinusoidal, bipolar square and triangular waveforms

Figure 4.7 shows the characteristics of the proposed RMS-DC converter for sinusoidal, bipolar square and triangular waveforms. Ideal RMS curves are also plotted and from the figure, it is evident that the characteristics of the circuit follow the ideal RMS plots very closely. Since RMS value implies the AC power, RMS value is determined by the amplitude and type of the signal. The ratio of the RMS values to the peak amplitudes of bipolar square, sinusoidal, triangular and sawtooth signals are 1, $1/\sqrt{2}$, $1/\sqrt{3}$ and $1/\sqrt{3}$ respectively. The deviation of the actual characteristic curves from ideal value is expressed by relative error and is defined as follows.

$$Relative\ error = \frac{I_{rms,calculated} - I_{rms,simulated}}{I_{rms,calculated}} \times 100 \tag{4.40}$$

Figure 4.8 shows the relative error with respect to input amplitude for sinusoidal, bipolar square and triangular waveforms. The relative error is within ±3% for an input range of 300-800 nA, 300-950 nA and 1-1.9 μA for square, sinusoidal and triangular/sawtooth waveforms respectively.

Figure 4.9 shows the transient response of the converter when excited by a 500 nA, 1

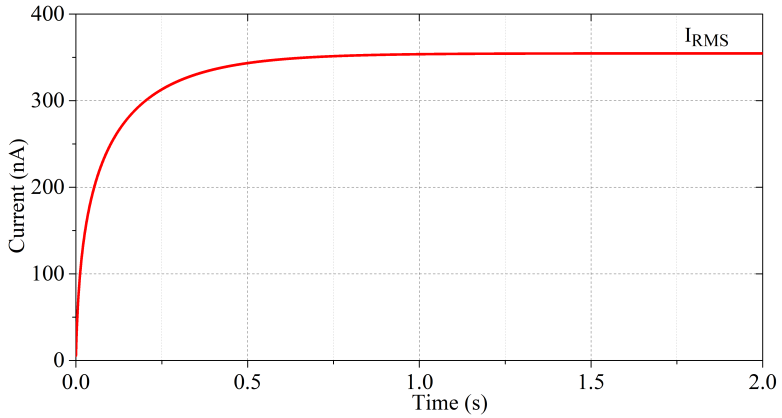


Figure 4.9: Transient response of the proposed converter

kHz sinusoidal signal. The circuit takes nearly 0.5 s to reach 90 % of the steady state value. Figure 4.10 shows the steady state time response of the proposed converter for 500 nA, 1 kHz sinusoidal and square waves, 1500 nA, 1 kHz triangular and sawtooth waves respectively. Simulations show that power consumption of the circuit for maximum accepted input (950 nA) is less than 1.6 μW and the static power dissipation (I_{IN}=0) is 20 nW which is contributed by bias current I_B. This bias current facilitates in tuning the bandwidth of the circuit. To determine the bandwidth of the circuit,

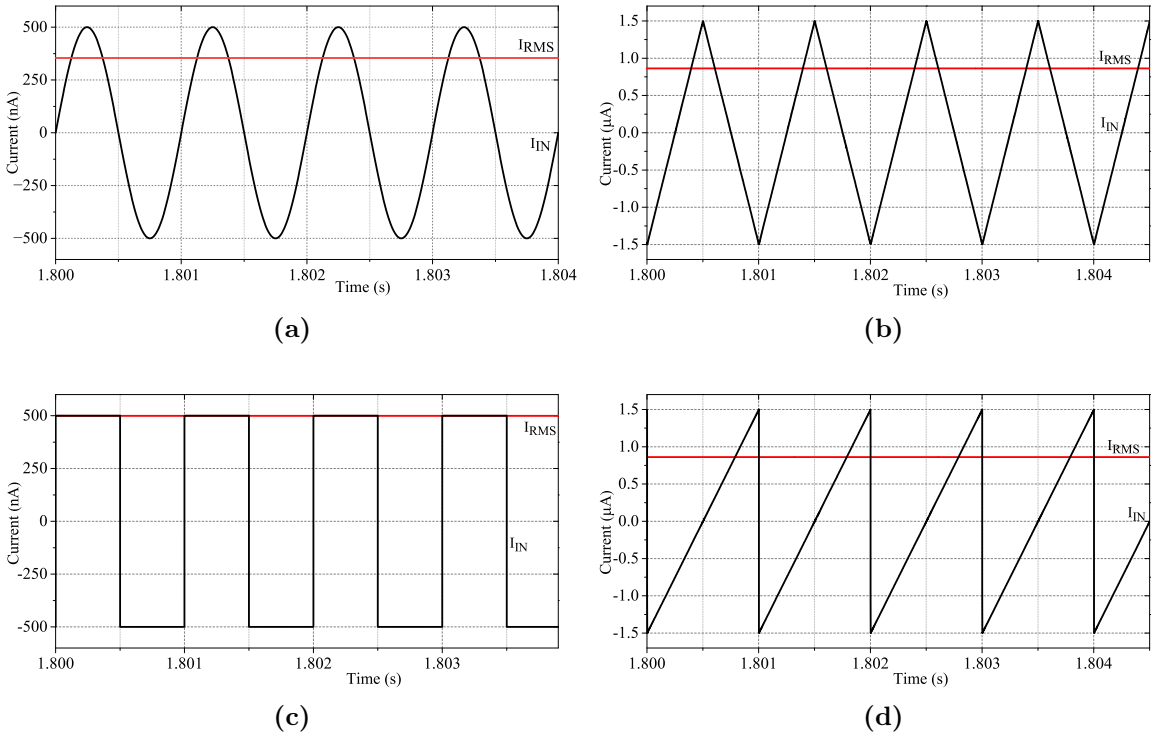


Figure 4.10: Steady state time response of the proposed RMS to DC converter for (a) Sinusoidal (b) Triangular (c) Bipolar square (d) Sawtooth waveforms

frequency of a 500 nA input sinusoidal signal is varied over a wide range. For I_B= 5 nA and C_{avg}= 10 nF, the bandwidth of the circuit is found to be 600 Hz - 650 kHz which shows a multi decade operation of the circuit. C_{avg} is selected by the following equation (Farshidi and Nejad 2012) for accepted levels of ripple in the output RMS current.

$$C_{avg} \geq \frac{5I_{rms,max}}{\eta V_T 2\pi f_{min}} \tag{4.41}$$

where $I_{rms,max}$ maximum converter output current, η is sub-threshold exponential slope factor, V_T is thermal voltage and f_{min} is the lower end of frequency range. Since the averaging capacitor and the bias current determine the lower and the higher ends of the bandwidth, respectively, the circuit offers a provision of programmability. The lower end of the frequency range can be tuned by selecting the external off-chip capacitor. This can be realized by designing an array of external capacitances and choosing a specific combination of a set of capacitors to give the desired lower frequency limit. The higher end of bandwidth can be tuned by choosing I_B, which

can be tuned by an external tuning circuit. Since I_B is also directly related to the cut-off frequency of the source follower low pass filter (ω_c), an independent tuning of I_B is not encouraged. An optimum programming algorithm for the required frequency range involves choosing C_{avg} and I_B for accepted ripple content in the output current.

4.4 PVT variations and second order effects

It is essential to verify the robustness and reliability of the proposed circuit and its stability against PVT variations. For this, the behaviour of the converter is studied by varying the supply voltage, temperature and process corners. Simulations show that the circuit is immune to power supply variations, stable over a range of temperature and gives results for various process corners with accepted level of accuracy. Figures 4.11, 4.12 and 4.13 show the variation of output RMS current for a 500 nA, 1 kHz sinusoidal signal against variations in power supply, temperature and process corners respectively. For ± 10 % change in supply voltage, the output current deviates around ± 5 % from the ideal value. The circuit shows good stability in the temperature range of 0 - 70 °C where the output RMS current fluctuates within ± 3 % of its actual value. The process corner deviations are also negligible where a maximum deviation of 5 % can be found for ff corner.

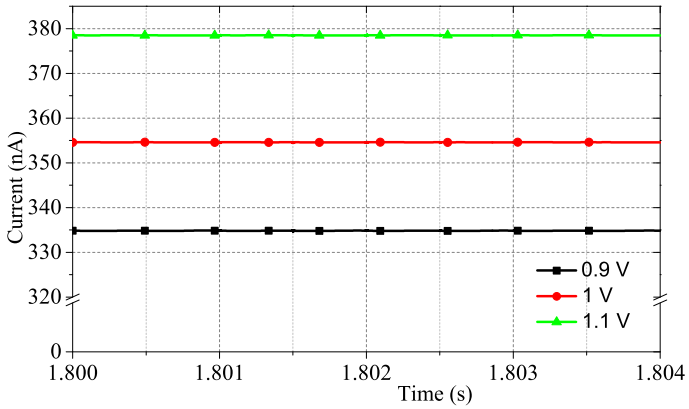


Figure 4.11: Response of converter against supply voltage variations

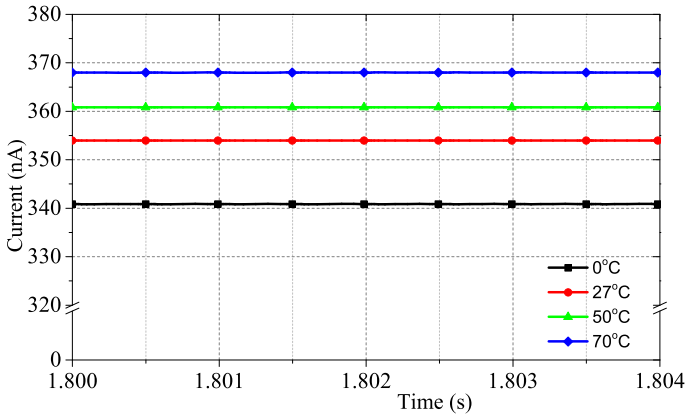


Figure 4.12: Response of converter against temperature variations

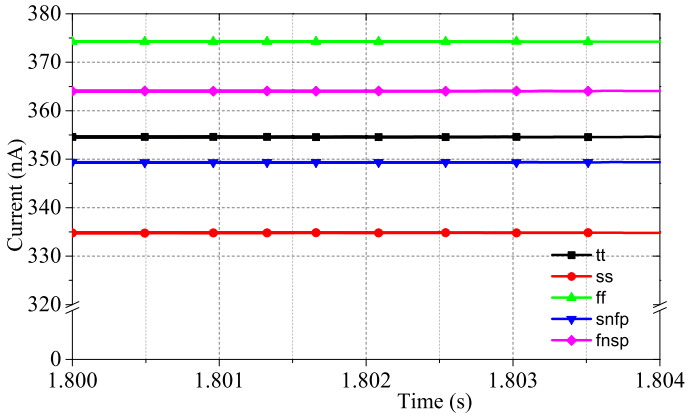


Figure 4.13: Response of converter for various process corners

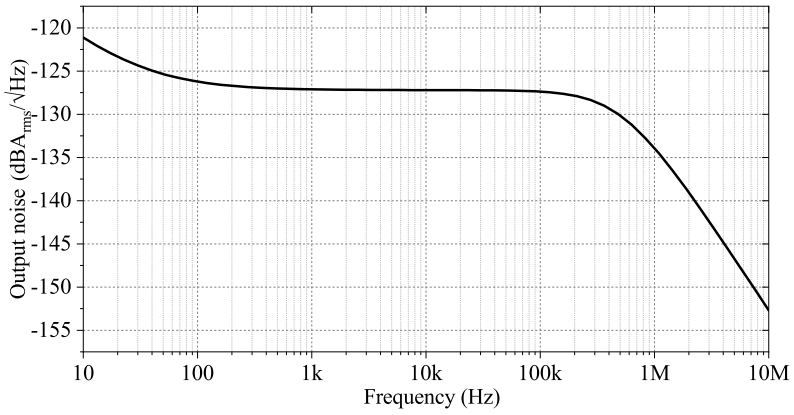


Figure 4.14: Output noise PSD

Table 4.2: Variation in bandwidth with respect to variations in V_{DD} and temp.

		Bandwidth (error within ± 5 %)
V_{DD} (V)	0.9	420 Hz - 525 kHz
	1	600 Hz - 650 kHz
	1.1	2.3 kHz - 760 kHz
		Bandwidth (error within ± 3 %)
Temp. (^oC)	0	500 Hz - 460 kHz
	27	600 Hz - 650 kHz
	50	8.2 kHz - 700 kHz
	70	10 kHz - 730 kHz

The output noise power spectral density is plotted and is shown in Figure 4.14. The output integrated noise from 10 Hz to 1 MHz is found to be 215 nA_{rms}. Table 4.2 shows the variation of bandwidth with respect to variations in supply voltage and temperature. To study the bandwidth variation with respect to supply voltage changes, the temperature is fixed at 27^oC and the bandwidth variation with respect to temperature changes, the supply voltage is fixed at 1 V.

Monte Carlo analysis is done for relative error against process variations and device mismatches and is shown in Figure 4.15. Simulation is carried out for 200 runs, and mean relative error was found to be -1.07 % with a standard deviation of 2.33. These results imply that the proposed converter is a robust, reliable and stable solution for RMS to DC conversion.

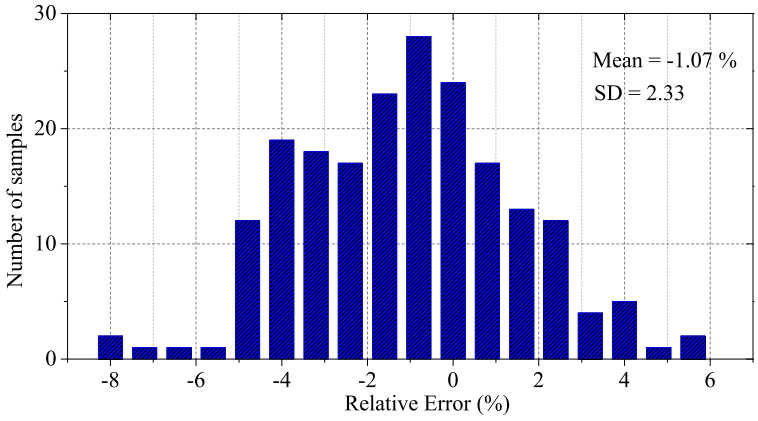


Figure 4.15: Monte Carlo analysis of relative error

4.5 Application of the proposed RMS to DC converter

To use the proposed RMS to DC converter for real world applications, the converter is tested within a biomedical system. The block diagram of the application of RMS to DC converter in a typical ECG detection environment is shown in Figure 4.16. The functional blocks of an ECG detection system are in voltage mode and a typical low power ECG detection environment is discussed by Sawigun and Thanapitak (2021) and Thanapithak and Sawigun (2018). Since the proposed converter is in current mode, it is necessary to convert the voltage signals to currents. This can be achieved by using a voltage-to-current converter at the interface between voltage mode circuits and current mode circuits. The technique used in this work to convert voltage ECG (V_{ECG}) to current ECG (I_{ECG}) is using an off-chip resistor at the input node of the converter. This current ECG signal is then injected to the translinear loop of the converter. A current mode low pass filter discussed in chapter 3 (Patil *et al.* 2019) is used for this work to filter out noise in raw ECG signals. The filter is used to limit the bandwidth of the ECG signal and to extract the PQRST complex from raw heart wave. The filter characteristics are given in Table 4.3. The proposed circuit extracts the energy content from the filtered ECG signal. This energy information is vital for doctors and medical workers in diagnosing cardiac disorders and abnormalities.

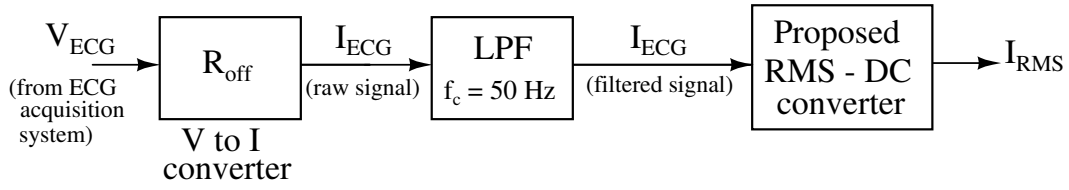


Figure 4.16: Proposed RMS to DC converter in biomedical system

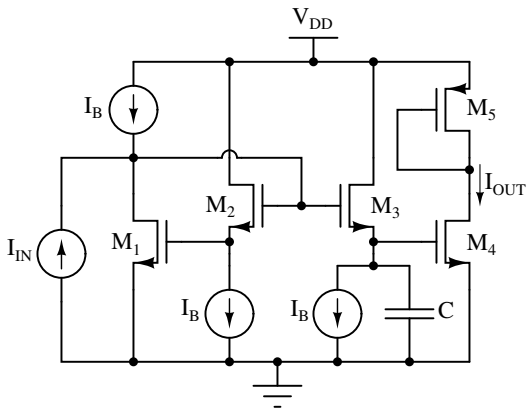


Figure 4.17: Log domain low pass filter for ECG detection

Table 4.3: Characteristics of log domain filter for ECG filtering

Topology	Cureent mode Translinear
V_{DD}	1 V
Technology	65 nm CMOS
f_c	50 Hz
DC gain	0 dB
Power	80 nW
I_{inpp} for 1 % THD	950 nA
Input referred noise	2.17 nA_{rms}
Dynamic range	57 dB

The cut-off frequency of LPF is fixed at 50 Hz. The circuit diagram of the first order log domain low pass filter is shown in Figure 4.17. Raw ECG signal is obtained from Physionet database (Goldberger *et al.* 2000), which is procured from human specimens. Filtered ECG output along with its RMS output is shown in Figure 4.18. This validates the application of the proposed circuit in low-power applications.

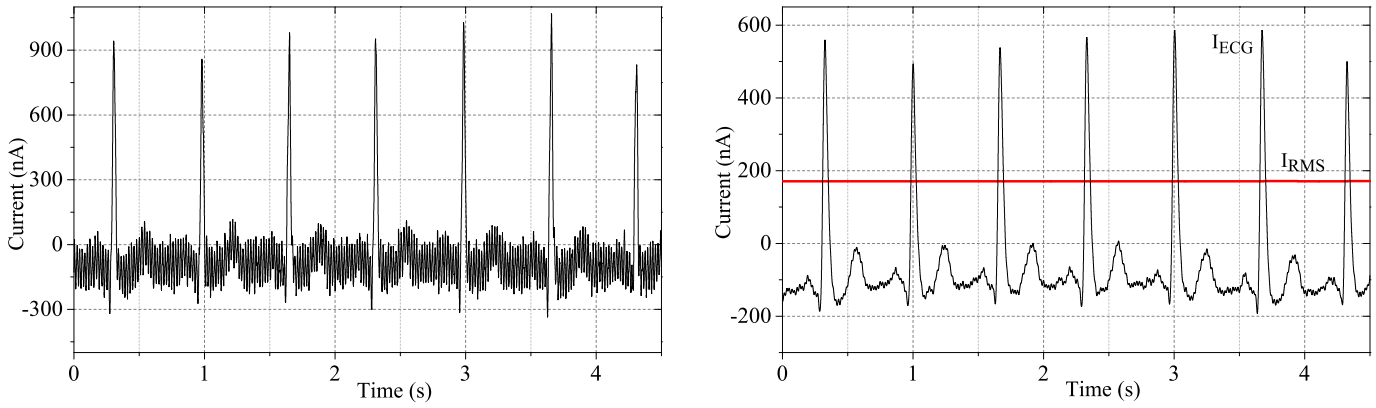


Figure 4.18: Performance of proposed RMS to DC converter in biomedical applications (a) Raw ECG signal (b) Filtered ECG signal along with corresponding RMS output

4.6 Comparison with existing literature

A fair and just comparison of the proposed converter with existing similar converters is shown in Table 4.4. The proposed circuit shows benefits of low-voltage low-power operation, wide input dynamic range, circuit compactness and sufficiently large bandwidth. The proposed circuit achieves low circuit complexity of only 14 transistors including absolute value circuit using only a single input current source and hence occupies very less silicon area on chip. For a quantitative analysis and to prove the performance superiority of the proposed circuit, a relatively more accurate figure of merit (FoM) is defined as follows.

$$FoM = \frac{P \times N_t \times N_i \times E \times \hat{C}}{DR \times f_{max}} \tag{4.42}$$

where P is the maximum dynamic power, N_t is the number of transistors used, N_i is the number of input current sources, E is the relative error expressed in %, $\hat{C}$ is the capacitance normalised to 1 nF, DR is the input dynamic range and f_{max} is the maximum frequency of operation. FoM is calculated for converters whose maximum dynamic power, input range and bandwidth/maximum operating frequency are reported. From Table 4.4, the proposed circuit exhibits the lowest FoM among other converters in the literature which implies that this work offers an energy efficient RMS

to DC conversion and can be used in low voltage, low power applications. For further ease of comparison FoM vs. V_{DD} is plotted and is shown in Figure 4.19.

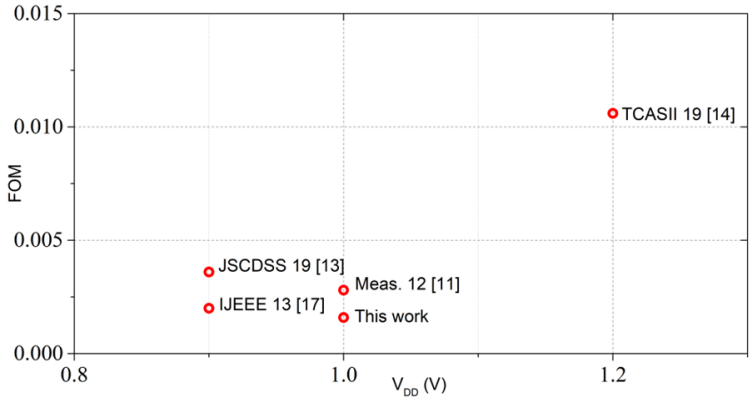


Figure 4.19: FoM vs. V_{DD}

4.7 Summary

This chapter presents a novel and energy efficient approach for the design of current-mode RMS–DC converter, which can be used in low voltage, low power applications. Both squarer–divider and low pass filter are administered within a single translinear loop which helps form a very low power consuming compact structure. The frequency range of operation can be selected externally, thus extending the use of the proposed design in a variety of applications. The post layout simulation results confirm the mathematical theory which is developed for the circuit. The stability of the circuit over PVT variations shows the robustness of the design. From FOM results, it is evident that the proposed topology offers superior performance over other existing RMS–DC converters.

The next chapter explains the design of a PTAT current source, which can be used in log-domain and G_m-C filter circuits used in bio-medical applications.

Table 4.4: Comparison of the proposed work with existing artworks

Ref.	Technology (μm)	Supply Voltage (V)	Input current range	Capacitor (nF)	Maximum dynamic power	Static power	Maximum frequency of operation	No. of input current sources	No. of transistors (Circuit complexity)	FoM
Farshidi and Sayedi (2007)	0.35	0.9	0.6-400 nA @ 2 % error	300	1.5 μW @ 400 nA	-	-	1	13	-
Farshidi and Nejad (2012)	0.18	1	50-500 nA @ 3 % error	10	3 μW @ 500 nA	-	3 MHz	1	42	0.0028
Farshidi and Sayedi (2008)	0.6	1.2	4-33 μA @ 3 % error	200	-	-	-	1	16	-
Talkhouncheh *et al.* (2019)	0.18	0.9	50-450 nA @ 6 % error	10	4 μW @ 450 nA	-	3 MHz	1	18	0.0036
Arraiza *et al.* (2019)	0.13	1.2	10-44 μA @ 10 % error	100	-	68 μW	3 MHz	1	16	0.0106
Farshidi and Asiaban (2012)	0.18	1.2	2.5-30 μA @ 3 % error	300	100 μW @ 30 μA	-	-	1	18	-
Shaterian *et al.* (2015)	0.5	5	200-390 μA @ 3 % error	1000	88 μW @ 10 μA	-	2 MHz	1	18	-
Danesh *et al.* (2013)	0.18	0.9	50-500 nA @ 3 % error	35	1 μW @ 500 nA	-	3.7 MHz	1	32	0.002
Mohammad Hadi *et al.* (2013)	0.18	0.9	1-400 nA @ 4 % error	15	0.9 μW @ 400 nA	-	-	1	15	-
Minaei and Psychalinos (2015)	0.35	1.5	70 pA -1 nA @ 3 % error	0.4	-	0.12 nW	850 Hz	1	20	-
Maryan and Azhari (2018)	0.18	1	-	20	1 μW @ 115 nA	-	-	4	19	-
Maryan *et al.* (2019)	0.18	0.8	72 pA - 1 nA @ 3 % error	100	1.4 nW @ 1 nA	82 pW	55 kHz	2	10	0.156
This work	**0.065**	**1**	**300-950 nA @ 3 % error**	**10**	**1.6 μW @ 950 nA**	**20 nW**	**650 kHz**	**1**	**14**	**0.00159**

Chapter 5

FAST SETTLING PTAT CURRENT REFERENCE

In this chapter, a fast settling PTAT current source is proposed. This chapter is an extension of work originally presented by Rao and Rekha (2019). A startup circuit added to the PTAT source improves the settling time of reference current. The proposed circuit exhibits good PTAT characteristics and better stability against power supply fluctuations. This can be used to bias low frequency filters in biomedical applications. The complete pipeline of the blocks used in such applications is shown in Figure 5.1. A low power log-domain filter is also designed in this chapter and biased using the proposed PTAT current source. Results show that the cut-off frequency of the filter remains constant irrespective of temperature variations.

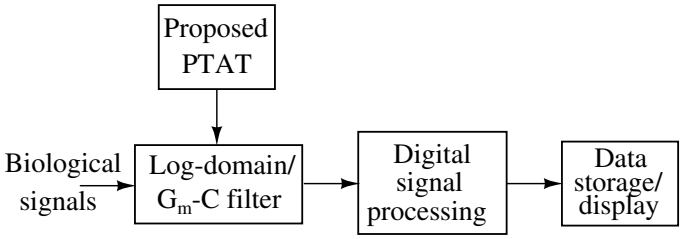


Figure 5.1: Pipeline of blocks used in biomedical applications

5.1 Proposed PTAT reference

A conventional beta-multiplier based current source circuit (Razavi 2005) is shown in Figure 5.2. Depending on the mode of operation of transistors, it can be a constant-G_m

biasing circuit or a PTAT current source. It acts as former if all the transistors work in strong-inversion saturation region ($V_{GS} > V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$) and as latter if all the transistors work in weak-inversion saturation ($V_{GS} < V_{th}$ and $V_{DS} \geq 3V_T$). When transistor operates in weak-inversion region, its drain current (Tsividis and McAndrew 2011) can be expressed as following.

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}-V_{th}}{\eta V_T}} (1 - e^{\frac{-V_{DS}}{V_T}}) \tag{5.1}$$

where $I_{D0} = \mu_n C_{ox} (\eta - 1) {V_T}^2$; μ_n and C_{ox} are electron mobility and gate oxide capacitance per unit area respectively. Other terms have their usual meanings. For $V_{DS} \geq 3V_T$ (weak-inversion saturation region), (5.1) can be approximated to (5.2).

$$I_D = \frac{W}{L} I_{D0} e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \tag{5.2}$$

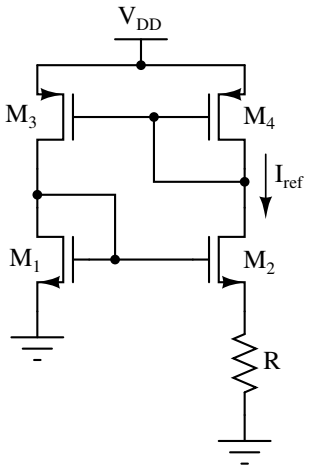


Figure 5.2: Beta-multiplier circuit

From Figure 5.2, the reference current I_{ref} which is also the drain current of M_2 (I_{D2}) can be written as (5.3).

$$I_{ref} = \frac{V_R}{R} \tag{5.3}$$

Voltage across resistor R (V_R) can be given as (5.4).

$$V_R = V_{GS1} - V_{GS2} \tag{5.4}$$

Using (5.2), gate-source voltages of M_1 and M_2 can be expressed as (5.5) and (5.6)

respectively.

$$V_{GS1} = \eta V_T ln(\frac{I_{D1}}{I_{D0}(\frac{W}{L})_1}) + V_{th1} \tag{5.5}$$

$$V_{GS2} = \eta V_T ln(\frac{I_{D2}}{I_{D0}(\frac{W}{L})_2}) + V_{th2}{}' \tag{5.6}$$

$V_{th2}{}'$ can be written as in (5.7) (Ferreira *et al.* 2008) to include the body effect of M_2.

$$V_{th2}{}' = V_{th2} + (\eta - 1)V_{SB} = V_{th2} + (\eta - 1)(V_R) \tag{5.7}$$

By substituting (5.5) and (5.6) in (5.4) and by assuming $V_{th1} = V_{th2}$, V_R can be derived as following.

$$V_R = I_{ref}.R = V_T ln(p) \tag{5.8}$$

where

$$p = \frac{(W/L)_2}{(W/L)_1}$$

Thus, I_{ref} can be expressed as in (5.9).

$$I_{ref} = \frac{V_T ln(p)}{R} \tag{5.9}$$

Assuming R is thermally stable, I_{ref} is directly proportional to temperature thereby giving PTAT characteristics. For lower values of currents (order of nAs), large values of resistors are needed. For example, to generate a reference current of 1 nA using circuit shown in Figure 5.2, a 10 MΩ resistor is required if p is chosen as 1.5. To accommodate such large resistors on chip, huge area is needed which makes the circuit more process dependent, hence reducing the accuracy of I_{ref}. In a typical SoC, where digital circuits and analog circuits co-exist together, a stable and precise clock will be available. In such systems, the resistor R in Figure 5.2 can be replaced by a switched capacitor driven by this clock which significantly enhances accuracy of I_{ref}.

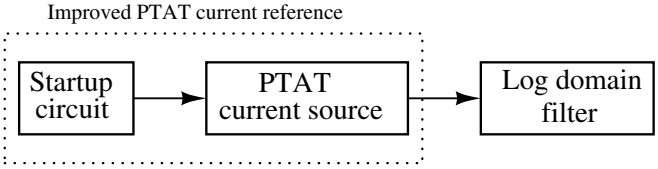


Figure 5.3: Block diagram of PTAT reference setup

The entire block diagram of the circuit setup discussed in this chapter is shown in Figure 5.3. The startup circuit is added to the PTAT current generator to reduce the settling time of I_{ref} thereby improving the transient response.

The transistor level implementation of PTAT current reference along with startup arrangement is shown in Figure 5.4. In the proposed circuit, every transistor is working in weak-inversion region. The value of p is chosen as 1.5 which means that the size of M_2 is 1.5 times the size of M_1. A switched capacitor comprising of capacitor C_1 and transmission gate switches (M_n and M_p) is used in place of resistor. M_p is selected 4 times larger than M_n in the transmission gate so that its on resistance does not depend on the voltage across it.

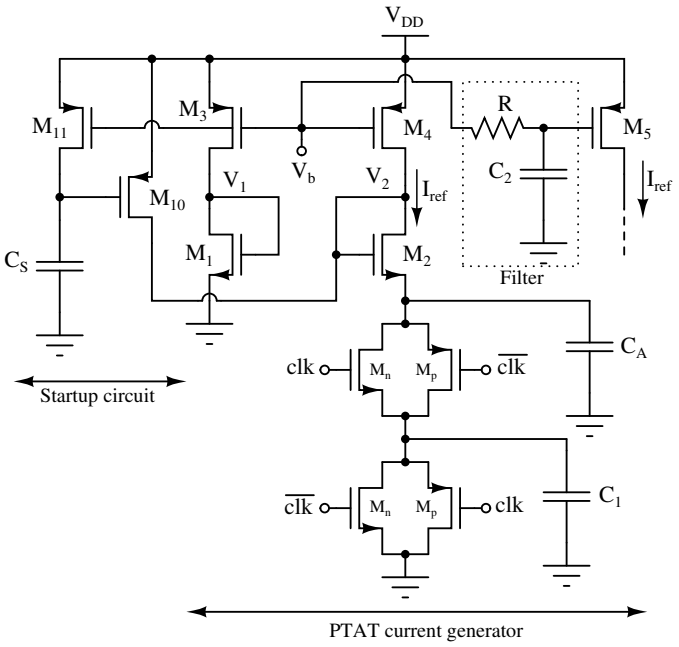


Figure 5.4: Proposed PTAT current reference

The sizes of all transistors used are given in Table 5.1.

Two clocks (clk and $\overline{clk}$) which are complementary to each other and having frequency f_{clk} are used for the switching operation. When clk becomes high ($\overline{clk}$ becomes low), capacitor C_1 charges and when clk becomes low ($\overline{clk}$ becomes high), it discharges. The average resistance (R_{eq}) of the switched capacitor is given as in (5.10) (Razavi 2005).

$$R_{eq} = \frac{1}{f_{clk} C_1} \tag{5.10}$$

Table 5.1: Size of transistors in Figure 5.4

Transistors	W/L (μm/μm)
M_1	4/3
M_2	6/3
M_{3-5}	20/3
M_6, M_7	2/3
M_8, M_9	6/3
M_{10}	1/0.5
M_{11}	2/1
M_n	1/1
M_p	4/1

By substituting R_{eq} (5.10) in place of R in (5.9), we get (5.11).

$$I_{ref} = V_T f_{clk} C_1 ln(p) \tag{5.11}$$

From (5.11) it can be seen that, I_{ref} is directly proportional to C_1. If f_{clk} and p are chosen properly, smaller capacitor values can be obtained for the currents in the order of nA.

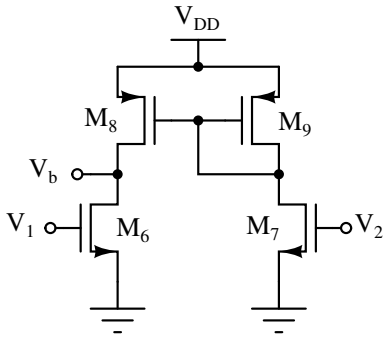


Figure 5.5: Error amplifier

The purpose of error amplifier which is shown in Figure 5.5 is to make the drain voltages of M_1 and M_2 equal thereby making currents through them equal. This kind of biasing minimises the dependency of I_{ref} on V_{DD} which improves supply voltage sensitivity.

It takes around 8 ms for the reference current to settle to the steady state value of 1 nA in the circuit presented by Rao and Rekha (2019). To reduce this delay, a startup arrangement comprising of M_{10}, M_{11} and C_S is added to the circuit. A similar

kind of startup circuit is discussed by Kumar *et al.* (2018). In Figure 5.4, when the circuit is switched on and before it reaches the steady state, initially the gates of $M_{1,2}$ and $M_{3,4}$ are at zero volt and V_{DD} respectively. Assuming zero initial voltage across the capacitor C_S, M_{10} turns on and pulls up the gates of $M_{1,2}$ to V_{DD}. $M_{1,2}$ start conducting and I_{ref} rises. Then, potential at the gates of $M_{3,4}$ drops and M_{11} turns on. C_S starts to charge towards V_{DD} and potential at the gate of M_{10} increases and once the circuit reaches steady state, M_{10} turns off. M_{10} and M_{11} do not have a static current path from V_{DD} to ground. Hence startup circuit dissipates zero static power. Value of capacitor C_S and sizes of M_{10} and M_{11} determine how fast startup circuit can initialise the main circuitry and how fast it can be disconnected once main circuitry reaches the steady state. Transistors M_{10} and M_{11} operate in linear region and the linear ON resistance of these transistors are given by (5.12).

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \tag{5.12}$$

The speed at which the startup circuit is activated is determined by the speed at which the transistor M_{10} is turned on. The ON time of M_{10} is limited by the input capacitance of M_{10} which comprises of gate to source and gate to drain capacitances. By properly choosing the size of M_{10}, the ON time can be optimised.

When it comes to disconnection of startup circuitry, assuming M_{11} as a linear resistance given by (5.12), the RC time constant (τ) of the branch consisting of M_{11} and C_S is given by (5.13).

$$\tau = \frac{C_S}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \tag{5.13}$$

When capacitor C_S charges above the voltage $(V_{DD} - V_{th})$, M_{10} turns off. $(V_{DD} - V_{th})$ is approximately 150 mV in this design and time for C_S to charge to this voltage (30 % of final value) from 0.5 V supply through M_{11} is nearly 0.4τ.

A low pass filter which comprises of R and C_2 is added to maintain the ripple content in the output reference current within the accepted level. Capacitor C_2 is chosen as 0.1 pF and resistor R is tuned to maintain the ripple content in I_{ref} less than *1 %*. To remove high frequency noise during switching operation, capacitor C_A is used at the source of M_2. A 100 kHz clock is selected for this work. The capacitors, C_1, C_A, C_S are taken as 0.8 pF, 10 pF, 1 pF respectively.

5.1.1 Simulation results

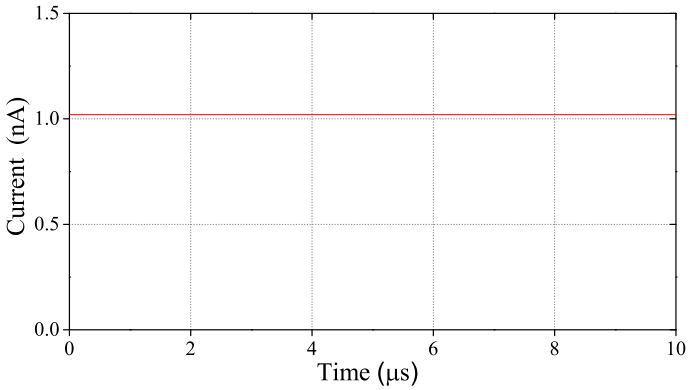


Figure 5.6: I_{ref} at V_{DD}= 0.5 V

The proposed circuit is designed using UMC 65 nm CMOS process with a supply voltage of 0.5 V. Periodic Steady State (PSS) analysis is carried out to plot the reference current. Figure 5.6 shows the output current generated (1 nA) for one clock period (10 μs) at room temperature (27°C).
Figure 5.7 shows I_{ref} variations when temperature is varied from $-10°C$ to 80°C for $V_{DD} = 0.5$ V. It can be observed that I_{ref} changes linearly with temperature and thus has a good PTAT characteristics over the range of temperature.

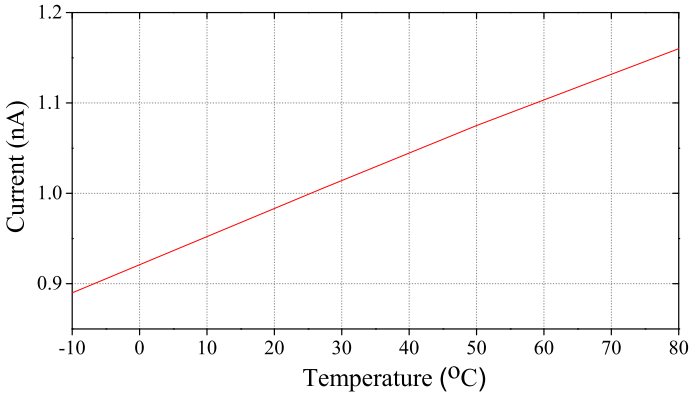


Figure 5.7: I_{ref} vs. temperature

I_{ref} is plotted for different values of V_{DD} at room temperature as shown in Figure 5.8. I_{ref} is 0.996 nA and 1.018 nA for V_{DD} of 0.4 V and 0.9 V respectively. The supply

voltage sensitivity of I_{ref} is found to be 3.23 %/V by considering these extreme values.

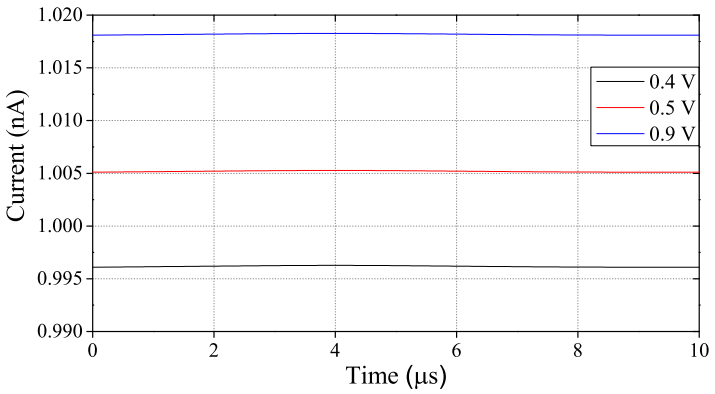


Figure 5.8: I_{ref} for different supply voltages

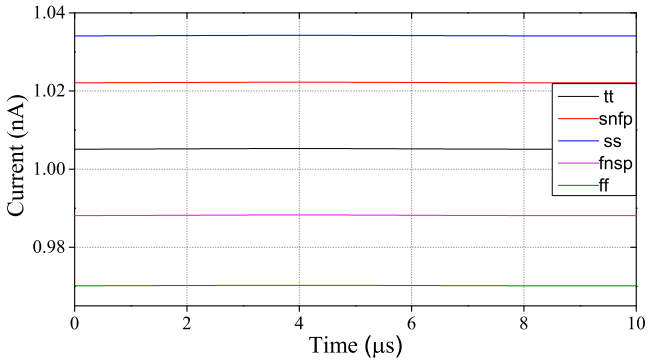


Figure 5.9: I_{ref} across process corners

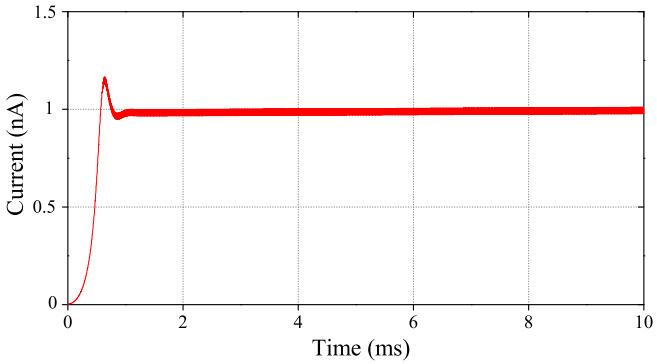


Figure 5.10: Transient response of the current flowing through M_2

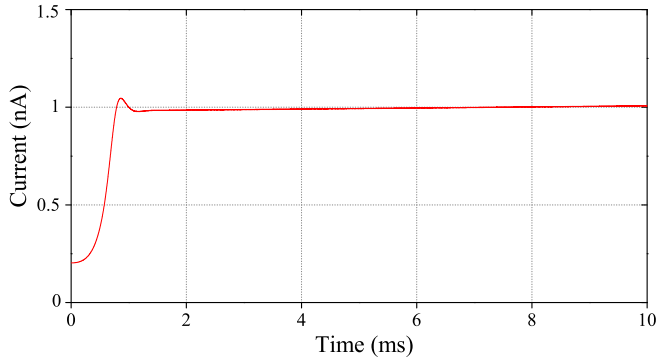


Figure 5.11: Transient response of the current flowing through M_5

Figure 5.9 plots I_{ref} for various process corners at room temperature and $V_{DD} = 0.5$ V. I_{ref} deviates maximum in ss and ff corners (1.034 nA and 0.968 nA). The maximum deviation is less than ± 3.6 %. The current flowing through the source of M_2 is shown in Figure 5.10. It has ripples having peak-to-peak magnitude of approximately 0.1 nA. The ripple free current flowing through M_5 is shown in Figure 5.11. The settling time is found to be approximately 1 ms.

Table 5.2: Comparison of the proposed work with other similar works

	Technology (μm)	Supply voltage (V)	Reference current (nA)	Settling time (ms)	Power (nW)	Supply voltage sensitivity (%/V)
Camacho-Galeano *et al.* (2005)	1.5	1.2	0.4	-	2	6
Osaki *et al.* (2013)	0.18	1.2	6	-	-	6.47
Jorge and Aita (2016)	0.04	1.2	100	-	350	2.9
Rao and Rekha (2019)	0.065	0.5	1	8	1.5	2.7
This work	**0.065**	**0.5**	**1**	**1**	**1.5**	**3.2**

The improved PTAT reference consumes a power of 1.5 nW at room temperature from a supply voltage of 0.5 V. The proposed circuit along with existing PTAT current references in the literature are listed in Table 5.2 and a fair comparison is done. The proposed PTAT circuit functions under the lowest supply voltage and has a very low supply voltage sensitivity and settles faster than Rao and Rekha (2019) (nearly 87 % improvement in settling time).

5.2 Log domain filter design

The proposed PTAT current source shows excellent PTAT characteristics. To verify this, a low frequency log-domain filter is designed and biased with the proposed switched capacitor based PTAT current reference. This log-domain filter can be used in low power biomedical applications like processing of ECG, EEG signals. The expectation is that the cut-off frequency of the filter remains the same irrespective of the variations in temperature.

The design of log domain filter is discussed in detail in chapter 3 and the schematic of the filter is shown in Figure 5.12.

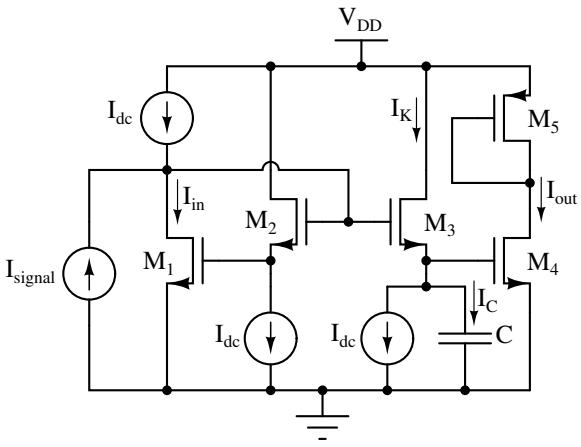


Figure 5.12: First order log-domain filter

In this circuit, the MOSFETs M_1–M_4 form the translinear loop. The cut-off frequency of the filter is given by following.

$$f_c = \frac{I_{dc}}{2\pi\eta V_T C} \tag{5.14}$$

The ideal DC current sources shown in Figure 5.12 can be replaced by current sources implemented using MOSFETs. In this work I_{dc} is taken as I_{ref} (1 nA). The cut-off frequency of 100 Hz is obtained by choosing C=37 pF. By substituting (5.11) in (5.14), f_c can be expressed as in (5.15).

$$f_o = \frac{f_{clk} C_1}{2\pi\eta C} ln(p) \tag{5.15}$$

From (5.15), it can be seen that f_c is independent of temperature.

5.2.1 Simulation results

The filter is designed to operate with a supply voltage of 0.5 V. For a comparison, I_{dc} is generated from a temperature independent current reference and ac response of the filter is plotted. Figure 5.13 shows the variation of cut-off frequency in the temperatures ranging from $-10°C$ to $80°C$. The maximum deviation is found to be 16 %. To verify the PTAT characteristics, I_{dc} is generated from the proposed PTAT source and ac response is plotted. Figure 5.14 shows that deviation of cut-off frequency is negligible and maximum deviation is found to be less than 2 %. The band transitions are enlarged in corresponding inset graphs. Table 5.3 shows the deviation of filter cut-off frequency for both temperature independent and the proposed PTAT current references.

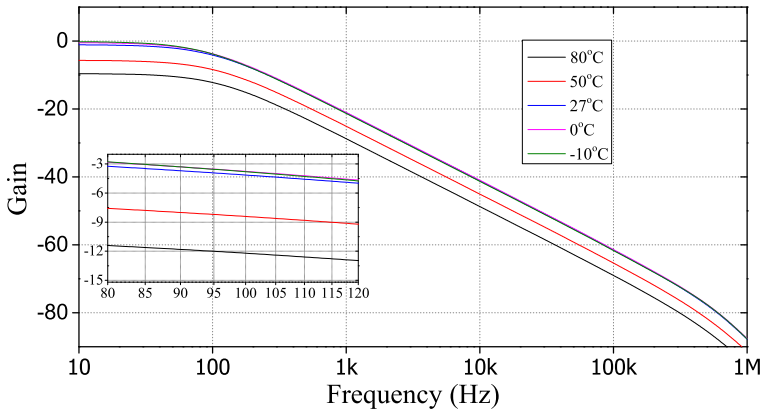


Figure 5.13: Response of the filter biased with temp. independent source

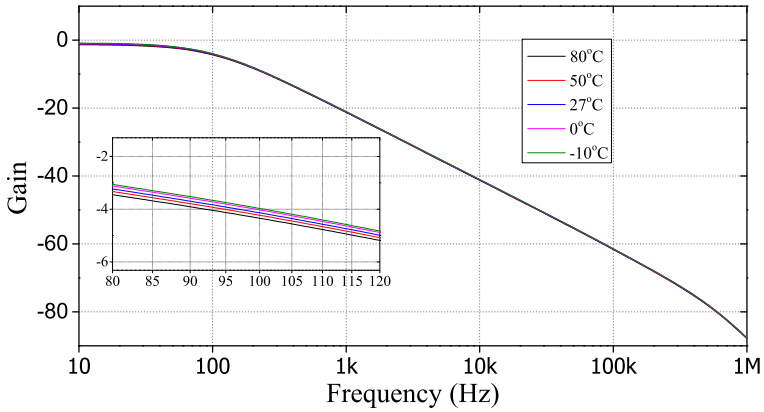


Figure 5.14: Response of the filter biased with the proposed PTAT

Table 5.3: Cut-off frequency deviation

Temp. (°C)	f_c (Hz)	
	Temp. independent	Proposed PTAT
-10	116	101.9
0	107	101.2
27	100	100
50	93	99
80	88	98.4

Table 5.4 lists the performance summary of the filter biased by the proposed PTAT current source.

Table 5.4: Performance summary of the filter

Topology	Log domain
Technology	65 nm CMOS
V_{DD}	0.5 V
f_c	100 Hz
DC gain	0.94
Power (nW)	2.5 nW
I_{in-pp} @25 Hz for 1% THD	0.82 nA
IRN†	3.26 pA$_{rms}$
DR @1 % THD	48 dB

†integrated from 1 to 100 Hz

5.3 Summary

This chapter proposes a low voltage, low power, fast settling switched capacitor PTAT current reference circuit. Settling time is reduced with the aid of a startup circuit. The PTAT circuit exhibits good PTAT characteristics in the temperatures ranging from $-10°C$ to $80°C$ while operating under a very low power. The circuit is less

susceptible to power supply fluctuations and can work at supply voltages as low as 0.4 V. To test the PTAT source, a low power log-domain low frequency filter is also designed and biased with PTAT reference. Simulation results imply that the filter cut-off frequency remains unchanged irrespective of temperature variations and this validates the theory explained in the paper.

Chapter 6

ACTIVE-RC FILTER FOR LOW FREQUENCY APPLICATIONS

As discussed in chapter 1, biological signals are very weak signals having very low bandwidth and their frequency range is listed in Table 1.1. To process these biological signals which have the above-discussed frequency range, the cut-off frequency of the filter used in the data acquisition system should be as low as the bandwidth of these signals. For example, the maximum bandwidth of the filter used in the acquisition of ECG signals must be a couple of hundreds of hertz.
Generally active-RC filters are used in the moderate frequency range (kHz-MHz). Conventional active-RC filter has limitations to operate in low frequency range. This chapter discusses the design of a low power active-RC filter for processing ECG signals. A folded cascode OTA with transistors operating in sub-threshold region designed in 180 nm CMOS technology operating at 1.2 V supply voltage is used as the building block of the filter.

6.1 Folded cascode OTA

An amplifier is one of the essential building blocks of the analog circuits and related systems. The design of the amplifier becomes more complex with new CMOS technologies, with reduced transistor length and decreased supply voltage. There are many topologies for the amplifier design such as telescopic, folded cascode and two stage designs among which folded cascode topology was chosen for this work. The folded cascode design is a prominent topology for the amplifier which gives sufficiently large

open loop gain, better output swing, convenient choice of common mode range and high output impedance (Razavi 2005). Compared to a telescopic amplifier, a folded cascode amplifier gives better output swing due to "folding" of transistors. Moreover, building a telescopic topology in lower supply voltage makes the design stringent. A folded cascode design relaxes this situation by folding the input and output branches. Apart from this, a folded cascode structure offers a convenient choice of input common mode. For example, the input common mode for a PMOS pair in a folded cascode design can be as low as zero and that for an NMOS pair can be as high as V_{DD}. The operational transconductance amplifier (OTA) used in this design is a differential input single ended output amplifier and is operating in sub threshold region.

Figure 6.1 shows the schematic of a PMOS input folded cascode operational transcon-

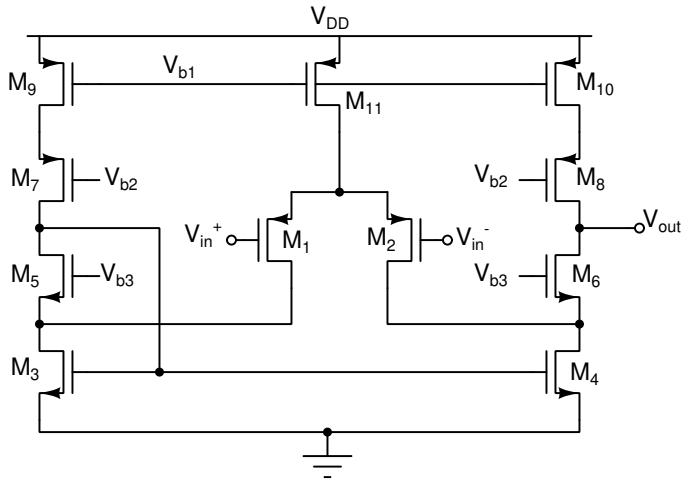


Figure 6.1: Folded cascode OTA

ductance amplifier with bias voltages V_{b1}, V_{b2} and V_{b3}. A PMOS input pair is chosen over NMOS pair in order to have low 1/f noise. Transistors M_1 and M_2 are the input devices with transconductances g_{m1} and g_{m2} respectively and M_{11} is the tail current source biased by voltage V_{b1}. The total current in the circuit is divided such that majority of current is flowing through input branch which comprises of transistors M_1, M_2 and M_{11} to have large transconductance. Thus the bias current through output branches comprising of transistors M_3-M_{10} is less so that the output resistance seen at the output node is enhanced. Transistors M_3-M_6 form a self cascode current mirror load and transistors M_7-M_{10} form the cascode current sources. The sizes of all transistors used are given in Table 6.1.

Table 6.1: Size of transistors in Figure 6.1

Transistors	W/L (μm/μm)
M_1, M_2	8/1
M_3, M_4	10/1
M_5, M_6	2/1
M_7, M_8	3/1
M_{9-11}	15/1

The unity gain bandwidth (UGB) of the amplifier is given by

$$UGB = \frac{g_{m1}}{2\pi C_L} \tag{6.1}$$

where g_{m1} is the transconductance of transistor M_1 and C_L is the load capacitance. The transconductance of the OTA in sub-threshold region is given by

$$g_m = \frac{I_D}{mV_T} \tag{6.2}$$

where I_D is the drain current flowing through input transistor M_1 (or M_2), m is a factor greater than one, which is related to the sub threshold slope and body effect and

$$V_T = \frac{kT}{q}$$

is the thermal voltage.

The drain current of a PMOS transistor working in sub-threshold region is given by

$$I_D = Aexp\left[B\left(V_{SG} - |V_{th}|\right)\right]\left[1 - exp\left(\frac{-V_{SD}}{V_T}\right)\right] \tag{6.3}$$

where,

$$A = \mu_p C_{ox}\frac{W}{L}(m-1){V_T}^2$$

$$B = \frac{1}{mV_T}$$

For $V_{SD} \geq 4V_T$, the current I_D can be assumed to be independent of V_{SD}. Then (6.3) can be simplified to

$$I_D \approx Aexp\left[B\left(V_{SG} - |V_{th}|\right)\right] \tag{6.4}$$

The output resistance of the folded cascode OTA is given by (6.5).

$$R_{out} = \frac{1}{\frac{(g_{ds4}g_{ds6})}{g_{m6}} + \frac{g_{ds8}(g_{ds2}+g_{ds10})}{g_{m8}}} \tag{6.5}$$

The DC gain of the OTA is given by (6.6).

$$A_V = \frac{V_{out}}{V_{in^+} - V_{in^-}} = \frac{g_{m1}}{\frac{(g_{ds4}g_{ds6})}{g_{m6}} + \frac{g_{ds8}(g_{ds2}+g_{ds10})}{g_{m8}}} \tag{6.6}$$

where g_{mi} is the transconductance of transistor M_i and g_{dsi} is the output conductance of transistor M_i.

Sub threshold region of operation offers better transconductance efficiency ($\frac{g_m}{I_D}$) than strong inversion region. i.e., more transconductance (g_m) can be generated with a given current (I_D) when transistor is operated in sub threshold region than in strong inversion region. Better voltage gain, low distortion, low power dissipation and simple compensation are the key merits in designing the input differential stage of CMOS amplifier below the strong inversion (Comer and Comer 2004). In this work, the input stage is designed in such a way that a total bias current of 15 nA is allowed to flow through the input transistors M_1 and M_2.

6.2 Filter realization

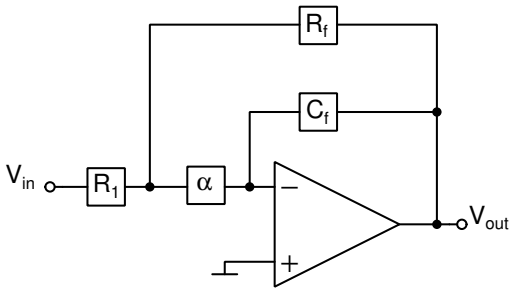


Figure 6.2: LPF with α block

A continuous time filter to process ECG signals having signal bandwidth of 50 Hz is designed. But to achieve this low bandwidth, the resistor and capacitor values used in the filter must be very high which consumes significant silicon area on the chip. To save the silicon area, the concept of current steering technique (Moon and Song

1993) is explored to enhance the time constant of the filter. Two first order low pass filters are built using the designed folded cascode OTA. The total filter is realized by cascading these two first order filters. A first order active-RC low-pass filter using current steering technique (Wong *et al.* 2005) is shown in Figure 6.2. R_1, R_f and C_f are the input resistor, feedback resistor and capacitor respectively. The current steering is done by the α-block. α-block determines the current through the capacitor C_f. In this design, α is chosen to be very much less than one. The effective capacitor transformation is shown in Figure 6.3. The effective capacitance is $\frac{C_f}{\alpha}$. Since $\alpha \ll 1$, effective capacitance is very much greater than C_f. For example, an effective capacitance of 100 pF can be realized by choosing C_f=1 pF and α=0.01.

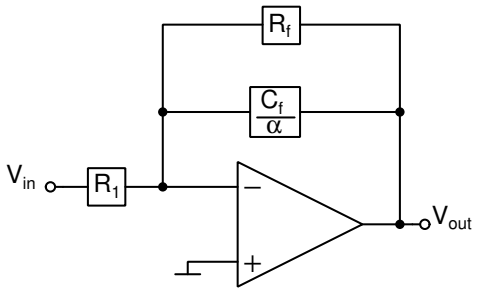


Figure 6.3: LPF with α-transformed capacitor

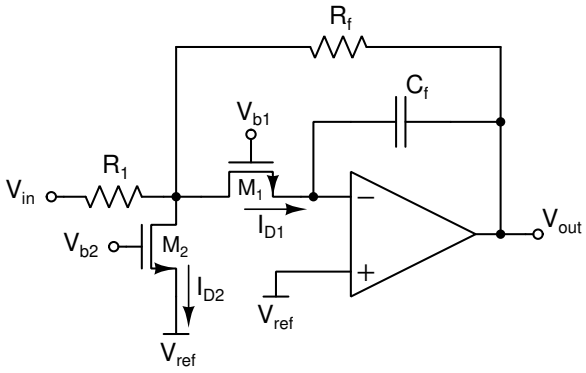


Figure 6.4: LPF with α block realized using transistors

The schematic of first order low pass filter with α-block realized using transistors is shown in Figure 6.4. Transistors M_1 and M_2 constitute the current steering block (α-block) and have W/L ratio of 8 μm/1 μm each. M_1 and M_2 are operating in deep triode region and work as voltage controlled resistors. A small fraction of input

current (I_{D1}) is flowing through M_1 to charge and discharge the capacitor C_f and most of the input current (I_{D2}) is bypassed through M_2. This process increases the effective capacitance and hence the time constant of the circuit. Thus, the cut-off frequency can be reduced without following the traditional method of employing very large capacitors and resistors and thereby saving the silicon area on chip to a great extent. The cut-off frequency of the filter can be tuned by varying V_{b1} or V_{b2}. In this design, V_{b2} is fixed at V_{DD} and V_{b1} is tuned to fix the cut-off frequency of the filter. The transfer function and the cut-off frequency of the circuit are given by (6.7) and (6.8) respectively.

$$H(s) = \frac{-\frac{R_f}{R_1}}{1 + s\frac{R_f C_f}{\alpha}} \tag{6.7}$$

$$f_c = \frac{\alpha}{2\pi R_f C_f} \tag{6.8}$$

where

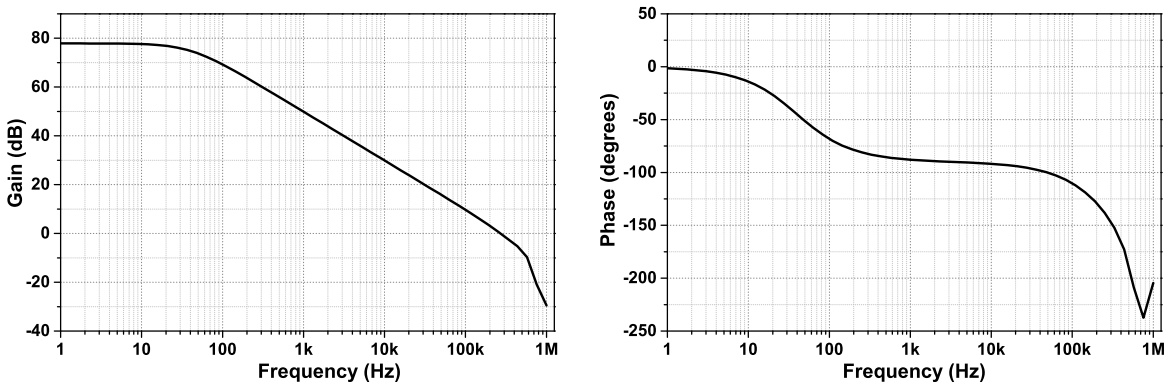
$$\alpha = \frac{I_{D1}}{I_{D1} + I_{D2}} \approx \frac{I_{D1}}{I_{D2}} \ll 1$$

The overall second order filter has two real poles at $\omega = \frac{\alpha}{R_f C_f}$. -3 dB frequency is taken as the cut-off frequency of the overall filter. To obtain 50 Hz as the overall cut-off frequency of the second order filter ($f_c{}'$) , the cut-off frequency of individual first order filter (f_c) (Sawigun and Serdijn 2016) is designed by

$$f_c{}' = f_c \cdot \sqrt{\sqrt{2} - 1} \tag{6.9}$$

6.3 Simulation results

The magnitude and phase responses of the designed OTA are shown in Figure 6.5a and Figure 6.5b, respectively. The OTA has a unity gain bandwidth (UGB) of 270 kHz and a DC gain of 77 dB. Table 6.2 lists the parameters of the folded cascode OTA.



(a) Magnitude response **(b)** Phase response

Figure 6.5: Frequency response of OTA

Table 6.2: Parameters of OTA

Technology	180 nm CMOS
V_{DD}	1.2 V
Open loop DC gain	77 dB
Power	30 nW
UGB (C_L=0.1 pF)	270 kHz
Phase margin	50^o
IRN†	54 μV_{rms}

†integrated from 20 Hz to 300 kHz

Figure 6.6 shows the frequency response of the second order filter. The cut-off frequency of the filter is found to be 50 Hz. Figure 6.7 shows a sample of unfiltered ECG (Goldberger *et al.* 2000) and corresponding filtered output. Even though it can not completely filter out noise, it can clearly illustrate P, QRS and T waves. This portrays a successful ECG detection.

Table 6.3 shows the performance summary. A fair comparison of the designed filter with existing works given in the literature is listed in Table 6.4. The Figure of Merit (FoM) in Table 6.4 is calculated as follows:

$$FoM = \frac{Power}{Order \times DR^2} \tag{6.10}$$

Lower FoM implies that the design is more energy efficient. It can be seen that the

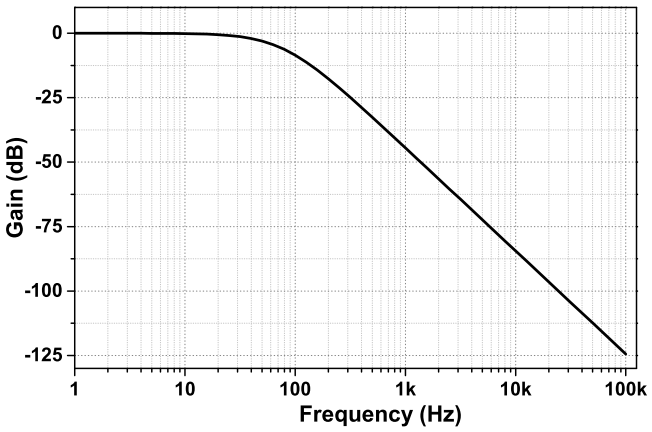
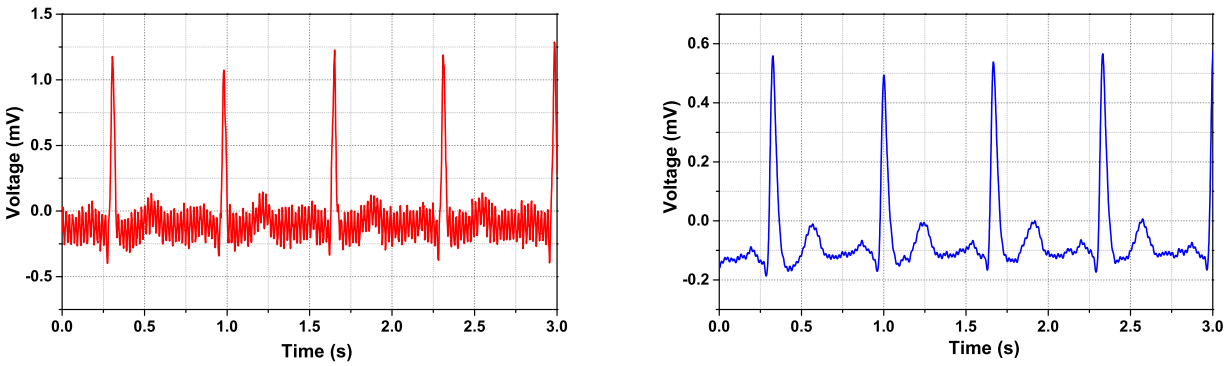


Figure 6.6: Frequency response of the filter

FoM of the designed filter is found to be as low as 0.4 pJ. This indicates that the designed filter is very energy efficient.



(a) **(b)**

Figure 6.7: (a) Sample of raw ECG (b) Filtered output

The conclusions of all the contributions proposed by this thesis and the future directions are detailed in the next chapter.

Table 6.3: Performance summary

Technology	180 nm CMOS
Topology	Active-RC
Order	2
V_{DD}	1.2 V
f_c	50 Hz
DC gain	0 dB
Power	80 nW
V_{in-pp} @16 Hz for 1% THD	96 mV
IRN†	90 μV_{rms}
DR @1 % THD	49 dB

†integrated from 1 to 50 Hz

Table 6.4: Performance comparison with other similar works

Ref.	Technology (μm)	Supply voltage (V)	f_c (Hz)	Order	DR @1 % THD (dB)	Power (nW)	FoM (pJ)
Solís-Bustos *et al.* (2000)	0.8	1.5	2.4	6	60	10,000	1.66
Veeravalli *et al.* (2002)	1.2	2.7	0.3	2	70	8,180	0.45
Qian *et al.* (2005)	0.35	1.5	37	5	57	11,000	4.3
Lee and Cheng (2009)	0.18	1	250	5	50	453	0.906
Gosselin *et al.* (2010)	0.18	1.8	3 k	9	34	360	15.9
Arya and Oliveira (2016)	0.13	0.9	48	2	43.8	800	16.6
Sun and Lee (2017)	0.18	1	50	5	49.9	350	0.7
This work	**0.18**	**1.2**	**50**	**2**	**49**	**80**	**0.4**

6.4 Summary

This chapter presents a low power second order active-RC filter designed in 180 nm CMOS process operating at 1.2 V supply voltage which is suitable for acquisition of ECG signals. A low power folded cascode OTA with transistors working in sub threshold region is used as the building block of the filter. To achieve the large time constant of the filter, current steering technique is employed unlike the conventional way of using large resistor and capacitor values and hence the design is area efficient. Having an OTA with good DC gain, the filter exhibits very good second order response. The filter was found to be consuming a power as low as 80 nW and showing a dynamic

range of 49 dB. The overall FOM of the filter was found to be 0.4 pJ which implies the power efficiency of the filter.

Chapter 7

CONCLUSIONS AND FUTURE DIRECTIONS

7.1 Conclusions

This thesis identifies the design challenges in designing low voltage, compact continuous time filters that can be integrated into portable biomedical instruments. Realizing the shortcomings of conventional filter designs, this thesis proposes feasible solutions for designing such filters under low supply voltages and with lower CMOS technologies (a few tens of nanometers). A fourth-order filter built using folded single-branch biquad is proposed, which operates under 0.6 V. The filter consists of only PMOS devices to have less 1/f noise and folding in the design gives better signal swing. The design is compact such that, with three transistors and a pair of capacitors, a biquad function can be realized and tuning filter parameters is also convenient. DR and FoM of this filter are comparable with many of similar filters and superior to some of the significant topologies reported in the literature.

This thesis also presents filter design using log-domain technique. Log domain filters are easy to design and compact compared to other conventional filter topologies. Log domain filters are developed from a mathematical model, a current domain differential equation of a low pass filter. A first-order log domain filter is proposed, which works under 0.9 V. The circuit can handle signal currents that are very close to bias currents. A second-order filter is realized by cascading such first-order cells. The filter consumes power as low as 55 nW and shows very good FoM, making it attractive for integrating into portable electronic devices.

In addition to linear circuits like filters, this thesis also addresses the challenges in designing non-linear circuits. For the same, a compact, low power RMS-DC converter is proposed. The core of the circuit is a third-order translinear loop that contains six transistors. Performance limitations that are usually concomitant with the conventional design of RMS-DC converter are precluded by the proposed design. The circuit operates under 1 V, uses only 14 transistors, has satisfactory operating range, and shows a wide bandwidth. An FoM to compare similar converters is proposed in this thesis, and the numbers show that the proposed converter has one of the best performances.

A PTAT current reference circuit that can be used to bias above discussed circuits is proposed. The current reference is switched capacitor based so that a low-value current (1 nA) can be generated without consuming a large silicon area on the chip. To reduce the settling time of the current, a startup circuit is proposed, which turns on the current reference faster.

Monte Carlo simulations and simulations across PVT variations have been performed to check the robustness of these proposed designs. It is found that all the designs are robust across these variations.

The literature is certainly benefited from the research carried out by this thesis. Various low power analog circuits are designed in the range of 0.6V to 1.2V supply voltage and presented. It is quite relevant as demand for low power and low voltage circuits is increasing with advent of electronic portable gadgets and implantable medical devices. This can also advance the field of artificial intelligence, underwater and space explorations, defence etc. where designs on ICs for such applications need to be very compact and energy efficient. However, the practical deployment of these design comes with its own set of complexities and limitations which are encountered after chip fabrication. These include manufacturing variability, sensitivity to environmental conditions, power supply noise and grounding, noise and interference, component aging and degradation, limited integration, difficulty in abstraction, testing and characterisation and limited design reuse. But most these limitations can be tackled by careful design, optimisation and good layout practices.

7.2 Future directions

This thesis mainly focused on developing linear/non-linear circuits suitable for low voltage ($\leq$ 1 V), and low power (of the order of nW) environments. While designing higher-order CT filters, the choice of Q factor of the biquads plays a major role. For the filter to have Butterworth/Chebyshev response, the location of filter poles and Q factor must be properly designed. Moreover, automatic tuning circuits can also be incorporated into the design to fix the filter parameters (cut-off frequency and quality factor) across transistor mismatches and process variations. The proposed filter design can be extended to have the above-mentioned standard filter responses along with on-chip circuits to stabilize filter parameters over device mismatches and PVT variations. SF and VF based filters are two of the prominent techniques in designing compact single-branch filters. They are energy efficient, sufficiently linear, and can be used for low power applications. Filter topologies based on SF and VF based architectures can be explored further.

Translinear principle is an excellent method to realize low power, high dynamic range circuits. This thesis proposed a CT LPF and an RMS-DC converter using this technique. But, a vast majority of linear/non-linear differential equations can be implemented using these techniques. Opamps, OTAs, BPF, notch filter, squarers, square root circuits, absolute value function, inverters etc., can also be realized in a very compact and efficient way. This thesis sheds light on the use of the translinear principle in designing all such circuits.

In the PTAT current reference, the large value resistor was replaced by a switched capacitor to generate a current of 1 nA. The circuit shows excellent supply voltage sensitivity and improved transient response. Additional circuits are added to suppress the noise generated by the switched capacitor. This work can be extended by replacing switched capacitor with impedance scaling circuits, some of which are discussed in chapter 1, that offer very large resistor values, thereby eliminating extra circuits for noise removal. Further, introducing such impedance scaling techniques to design ultra-low voltage ($<$ 0.5 V) current references will be interesting.

This thesis contributed to developing ICs that can be used in the detection/processing of ECG signals. Many research has been carried out in recent years to study wave propagation in the human heart. Owing to the complexity of experiments on real human hearts, several investigations were conducted using a prototype model, Belousov-

Zhabotinsky (BZ) reaction (Zaikin and Zhabotinsky 1970). This is a simple chemical reaction whose wave dynamics resemble that of the heart. The BZ dynamics are mathematically expressed by the two-variable Oregonator model (Field and Noyes 1974). However, these models, which are coupled partial differential equations, are difficult to solve without sophisticated numerical models, and it demands extensive computations. If the chemical parameters in the wave model could be translated into an electrical equivalent, these models can be represented by differential equations involving electrical parameters. This can be implemented using the log-domain technique which is discussed in chapters 3 and 4. Thus, human heart models can be simulated in circuit level using transistors and passive devices. This will be a significant advancement in the study of heart wave dynamics.

The circuits proposed in this thesis are designed using 65 nm CMOS technology. But the digital circuits are currently fabricated under 28 nm, 14 nm and 7 nm technology nodes. So it is necessary to develop analog circuits that can offer satisfactory performance under these technology nodes. This thesis can be used as a benchmark for such advancements in the state-of-the-art. This thesis helps designers realize filters and other non-linear circuits which can operate under a supply voltage 0.3 V or less, thus extending the research set by this thesis.

Since designing compact low-voltage analog circuits for low-power applications is quite challenging, the scope of the research is never-ending and there is a persistent trend to attain performance very close to ideal one. The capabilities of such analog architectures may constantly be expanded, and the performance boundaries can always be pushed further.

Appendix I
SUB-THRESHOLD REGION OF OPERATION

A-1 Introduction

In order to achieve higher transconductance efficiency at lower currents and to reduce the overall power consumption of the circuit, transistors are operated in sub-threshold (weak inversion) region. When $V_{GS} < V_T$, the transistor conducts in sub-threshold region. In this region, the drain current equation of a MOS transistor is given by (A.1) (Taur and Ning 2013, Tsividis and McAndrew 2011).

$$I_D = I_{D0}(\frac{W}{L})e^{\frac{V_{GS}-V_{th}}{\eta V_T}}(1 - e^{\frac{-V_{DS}}{V_T}}) \tag{A.1}$$

where $I_{D0} = \mu_n C_{ox}(\eta - 1)V_T^2$; μ_n, C_{ox}, η and V_T $(= kT/q)$ are mobility of the electron, capacitance per unit area presented by the gate oxide, sub-threshold slope factor and thermal voltage respectively. For sub-threshold saturation region $(V_{DS} \geq 4V_T)$, $1 - e^{\frac{-V_{DS}}{V_T}} \approx 1$. Hence, (A.1) is approximated to (A.2).

$$I_D = I_{D0}(\frac{W}{L})e^{\frac{V_{GS}-V_{th}}{\eta V_T}} \tag{A.2}$$

The transconductance of the transistor operating in sub-threshold saturation region is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{\eta V_T} \tag{A.3}$$

Appendix II
NON-LINEARITIES IN A SYSTEM

A-2 Harmonics

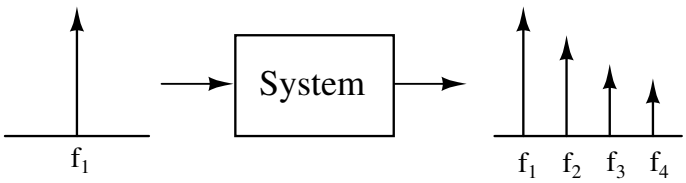


Figure A.1: Harmonics in a system

An ideal linear system can be written in the form of

$$y(t) = Kx(t) \tag{A.4}$$

where y(t) and x(t) are the output and input of the system, respectively. This means that the output is directly proportional to the input of the system. For example, if the input to the system is $x(t) = Asin(\omega t)$, then the output can be written as $y(t) = KAsin(\omega t+\phi)$. However, a practical system does not follow this direct proportionality. The output of such systems can be written as

$$y(t) = a_1x(t) + a_2x(t)^2 + a_3x(t)^3 + .. \tag{A.5}$$

where $a_1 > a_2 > a_3$...The higher order terms are called harmonics, and these are the copies of signal appearing at frequencies that are integral multiples of the fundamental

frequency. This is depicted in Figure A.1. Devices are typically linear over a certain input range, where the power of harmonics is negligible. Beyond this range, the non linear behaviour of the system becomes significant which can distort the output. This distortion leads to loss of data, which is undesirable.

A-3 Intermodulation

Intermodulation occurs when two (or more) signals mix in a non-linear device. This mixing produces new signals at the sums and differences of their frequencies. f_1 and f_2 are the fundamental tones that excite the system and output spectrum is shown in Figure A.2.

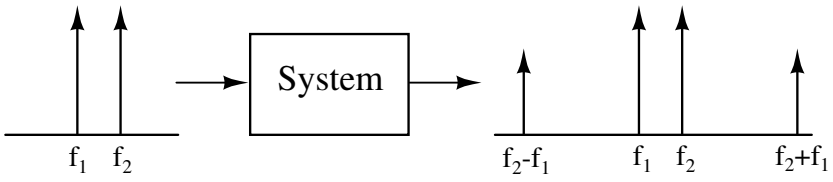


Figure A.2: Intermodulation in a system

Apart from the mixing of fundamental tones with themselves, they can mix with each other's harmonics ($2f_1$, $2f_2$) and generate products at frequencies $2f_1$+f_2, $2f_1$-f_2, $2f_2$+f_1, $2f_2$-f_1...These are called intermodulation products. The order of harmonics and intermodulation is the sum of their (unsigned) coefficients. For example:

- $2f_1$ is second order (2)
- f_1+f_2 is also second order (1+1)
- $3f_1$ is third order (3)
- $2f_2$+f_1 and $2f_2$-f_1 are both third order (2+1)

The output spectrum showing intermodulation products is plotted in Figure A.3.

A-4 Third order intermodulation

The above-discussed intermodulation products, in most cases, are undesired. This distortion is often referred to as intermodulation distortion. Some products are easy

to eliminate from the output spectrum. For example, higher-order harmonics have very low amplitudes and can usually be ignored. Higher frequency products often fall outside of the filter passband and hence get attenuated. The typical way of dealing with troublesome products is through filtering, but this becomes difficult when the products are very close in frequency to the desired (fundamental) signals. As shown in Figure A.3, among the intermodulation products, tones $2f_1$-f_2 and $2f_2$-f_1 (third order intermodulation products) pose a concern since these tones appear close with the fundamentals, which cannot be easily filtered out.

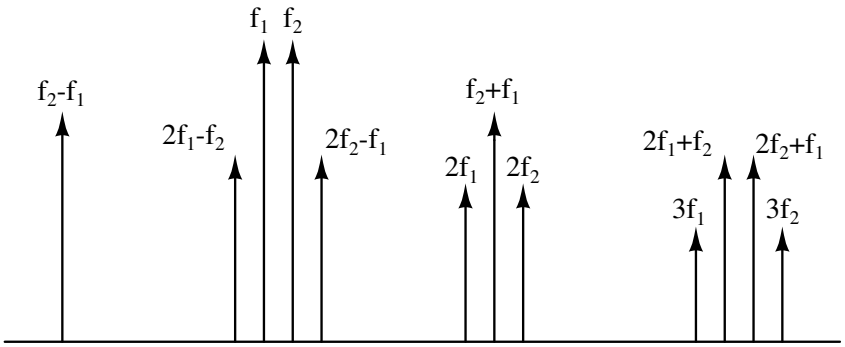


Figure A.3: Higher order intermodulation products

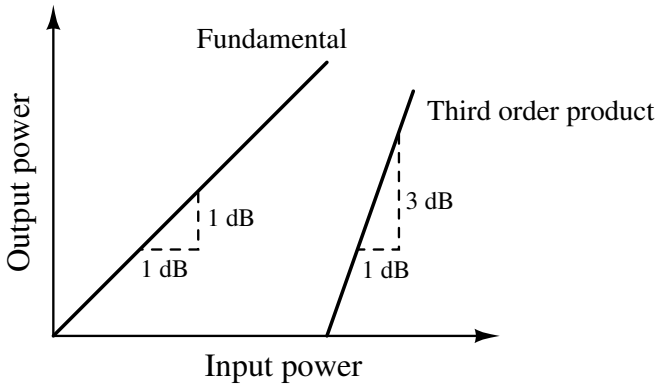


Figure A.4: Power plots

Besides the filtering issue, third-order intermodulation products present an additional complication. For every 1 dB increase in the power of the fundamental (useful) signal, the power of third-order (unwanted) intermodulation products increases by 3 dB. This is shown in Figure A.4. This means that not only do the frequencies of

third-order intermodulation products fall close to fundamentals, but also the power of the former rises more quickly than that of the latter.

A-5 Third order intercept

It would appear that the two gain lines in Figure A.4 would meet at some point. i.e., at some input power, the level of third order products would match and eventually exceeds the level of the fundamental signal. In reality, however, this does not happen. Real-world devices have a limit on how much output power they can produce regardless of the level of input power. Eventually, the maximum output power is reached when the gain lines begin to curve or flatten out. When this point is reached, the device (filter in this work) is said to be in compression. However, if we extend the two lines, we can calculate the point at which they would meet. This is the third order intercept point often referred to as TOI or Input Intercept Point (IIP_3) because this is the point where the third order power would intercept the fundamental power. This is shown in Figure A.5.

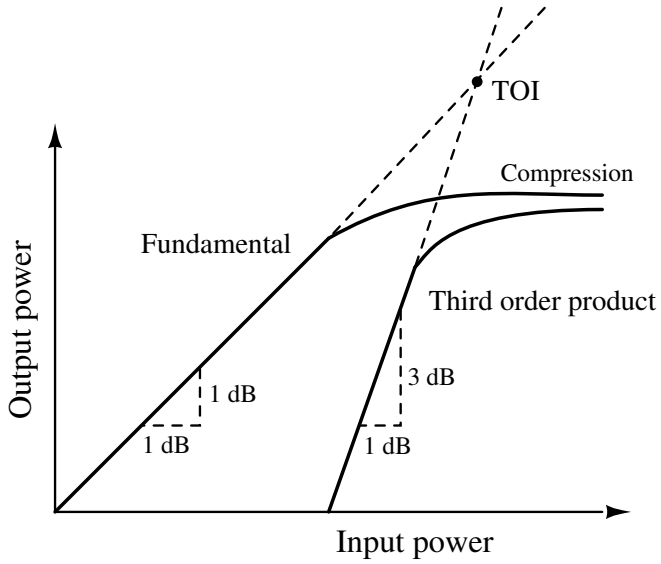


Figure A.5: Third order intercept

From the graph, it is evident that TOI is a theoretical value that we calculate based on measured values. In short, we cannot "measure" TOI directly.
TOI is the most common way to quantify the linearity of the device. The higher the TOI, the better the linearity and the lower the level of intermodulation distortion.

Appendix III
PERFORMANCE METRICS OF A FILTER

The linearity parameters of a filter are discussed in the previous section. Based on such parameters, the performance of the filter can be studied, and the metrics to quantify the performance are listed below.

A-6 Total Harmonic Distortion

Total harmonic distortion (THD) is a measure to estimate the non-linearity of a system. It is defined as the ratio of sum of the powers of all harmonic components to the power of the fundamental component. It is expressed in percentage (%) or in decibels (dB). THD is also expressed in terms of RMS voltages as given in (A.6).

$$THD\,(dB) = 20\,log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ...}}{V_f}\right) \tag{A.6}$$

where V_i ($i = 2,\ 3,\ 4....$) is the RMS voltage of i^{th} harmonic component. V_f is the RMS voltage of the fundamental component.

Lower THD indicates less distortion in the filter output. A THD of 1 % (-40 dB) is considered as an acceptable level of distortion in all the characterization of circuits discussed in this thesis. This means that the power of sum of all the harmonics is less than or equal to 1 % of the power of fundamental.

A-7 Input Referred Noise

Input-referred noise (IRN) is the noise voltage or current that, when applied to the input of the noiseless circuit, generates the same output noise as the actual circuit does. This is a theoretical concept and cannot be "measured". IRN can be calculated by measuring other noise parameters of the circuit. The equivalent representation of IRN in a circuit is shown in Figure A.6.

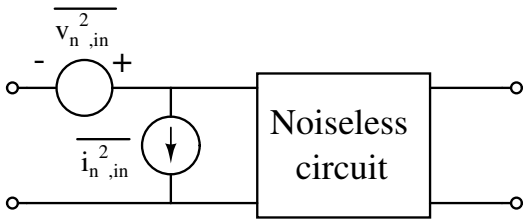


Figure A.6: Input referred noise

A-8 Dynamic Range

Dynamic range is defined as the ratio of maximum input signal level to the minimum input signal level that a circuit can handle. Maximum input signal is limited by the distortion and minimum input is limited by the IRN. For CT filters, dynamic range is defined as

$$\text{DR} = \frac{\text{RMS value of the input signal for a specified THD at the output}}{\text{Input referred noise}} \tag{A.7}$$

A-9 1 dB Gain Compression Point

The 1 dB gain compression point describes the device saturation. A device maintains a constant gain for low-level input signals. However, at higher input levels, the device saturates, and its gain decreases. The 1 dB gain compression point indicates the power level that causes the gain to drop by 1 dB from its small signal value.

A-10 Figure of Merit

Figure of merit (FoM) is used to evaluate the power efficiency of filter circuits. Generally, FoM is defined as,

$$FoM = \frac{Cost}{Performance} \tag{A.8}$$

The cost of circuit operation is the power it draws from the supply/battery. The performance is measured in terms of the linear range and bandwidth of the circuit. The performance also accommodates a metric that shows how ideal the filter response is (order of the filter). In this work, we have used two expressions for the figure of merit defined in (A.9) (Zhang *et al.* 2013) and (A.10) (Rekha and Laxminidhi 2013).

$$FoM_1 = \frac{P}{N \times f_c \times DR} \tag{A.9}$$

$$FoM_2 = \frac{P}{N \times DR^2} \tag{A.10}$$

where P is the total power consumption, N is the filter order and f_c is the cutoff frequency. A lower value of FoM indicates better energy efficiency of the filter.

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Publications based on the Thesis

Journals

Published

1. **Muhammed Mansoor C. B.**, Anuradha P. and Rekha S. ‟1 V, 20 nW true RMS to DC Converter based on third order dynamic translinear loop,″ IETE Journal of Research (Taylor & Francis), pp. 1-12, 2022.
   DOI: 10.1080/03772063.2022.2077244.
2. **Muhammed Mansoor C. B.**, Hanumantha Rao G. and Rekha S. ‟Low power fast settling switched capacitor PTAT current reference circuit for low frequency applications,″ Advances in Science, Technology and Engineering Systems Journal, Vol. 5, No. 6, pp. 865-870, 2020.
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Communicated

- **Muhammed Mansoor C. B.**, and Rekha S. ‟0.6 V, 61 dB DR fourth order low pass filter using folded single branch biquads,″ Circuits, Systems, and Signal Processing, Springer.

Conferences

1. **Muhammed Mansoor C. B.** and Rekha S. ‟Low power active-RC filter for ECG detection,″ IEEE sponsored Global Conference for advancement in Technology (GCAT 2019), Bangalore, 18-20 Oct. 2019, pp. 1-5.
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