ADAPTIVE DISTANCE RELAY FOR STATCOM CONNECTED TRANSMISSION LINES - DEVELOPMENT OF DSP BASED RELAY HARDWARE, RELAYING SCHEMES AND HIL TESTING PROCEDURES

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby ***declare*** that the Research Thesis entitled **ADAPTIVE DISTANCE RELAY FOR STATCOM CONNECTED TRANSMISSION LINES - DEVELOPMENT OF DSP BASED RELAY HARDWARE, RELAYING SCHEMES AND HIL TESTING PROCEDURES** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirements for the award of the Degree of ***Doctor of Philosophy*** is a ***bona fide report of the research work carried out by me***. The material contained in this thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to *certify* that the Research Thesis entitled **Adaptive Distance Relay for STATCOM Connected Transmission Lines - Development of DSP Based Relay Hardware, Relaying Schemes and HIL Testing Procedures**, submitted by **Sham M.V.** (Register Number: EE09F02) as the record of the research work carried out by him, is *accepted* as the *Research Thesis submission* in partial fulfillment of the requirements for the award of degree of ***Doctor of Philosophy***.

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ABSTRACT

KEYWORDS: DSP;FACTS;HIL;STATCOM .

Flexible AC Transmission System (FACTS) devices are used to enhance the transient stability limit and power transfer capacity of the existing transmission lines. Static Synchronous Compensator (STATCOM) a shunt type FACTS device is used to maintain the voltage at the point of common coupling on the transmission lines. A STATCOM has fast response of about 1-2 fundamental cycles, which matches with the typical response time of the protection subsystem. Hence, its functional characteristics and associated control system introduce dynamic changes during fault conditions in a transmission line. It is important that distance relays perform correctly irrespective of such dynamic changes introduced during faults, as it defeats the purpose of STATCOM installation.

The work presented in this thesis is aimed at detailed study on the influence of STATCOM on the performance of distance relay under normal and abnormal operating conditions of the power systems. The work also put forth adaptive distance relaying schemes to mitigate the adverse of impact of STATCOM on distance relay. Its performance is compared with the conventional standalone mho type distance relay, through simulations on a realistic study power system using EMTDC/PSCAD package.

A relay hardware to implement, the adaptive relaying scheme has been developed using TMS320F28335 digital signal processor and a simultaneous sampling ADS8556 analog to digital converter. The real time hardware in the loop test bench has been developed, using Doble F6150 power system simulator, to test the performance of the newly developed relaying schemes and relay hardware. The simulation results obtained from EMTDC/PSCAD are used as test signals for this purpose. The evaluation results

have clearly demonstrated, the efficacy of the adaptive relaying schemes in mitigating the adverse impact of STATCOM on the distance relay performance.

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ABBREVIATIONS

ac	alternating current
ADC	Analog to Digital Converter
ANN	Artificial Neutral Network
COMTRADE	COMmon format for TRAnsient Data Exchange for power systems
DAS	Data Acquisition System
dc	direct current
DSC	Digital Signal Controller
DSP	Digital Signal Processor
EMTDC	Electromagnetic Transient and DC
FACTS	Flexible AC Transmission System
FCWF	Full Cycle Window Fourier
FFS	Fundamental Frequency Switching
FFT	Fast Fourier Transform
GTO	Gate Turn Off thyristor
HIL	Hardware-In-the-Loop
HMI	Human Machine Interface
ISR	Interrupt Service Routine
LPF	Low Pass Filter
MLI	Multi-Level Inverter
MPI	Multi-Pulse Inverter
ms	milliseconds
NPC	Neutral Point Clamped
PC	Personal Computer
PCC	Point of Common Coupling

PI	proportional-integral
PLC	Programmable Logic Controllers
PLL	Phase Locked Loop
PSCAD	Power Systems Computer Aided Design
PST	Phase Shifting Transformer
PWM	Pulse Width Modulated
RFCWF	Recursive Full Cycle Window Fourier
S/H	Sample and Hold
SSC	Signal Conditioning Circuit
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
THDv	voltage Total Harmonic Distortion
VAR	Reactive Volt Ampere
VSC	Voltage Source Converter
VSI	Voltage Source Inverter

NOTATION

α	Phase angle between the STATCOM voltage and the ac power system voltage (degree)
δ	Load angle (degree)
θ	Phase Locked Loop synchronizing angle (degree)
σ	Conduction angle over a half cycle period (degree)
γ	Dead angle over a quarter cycle period (degree)
E_r	Receiving end source voltage (kV)
E_s	Sending end source voltage (kV)
I_q	Actual quadrature current (p.u.)
I_{qref}	Reference quadrature current
I_{sc}	Short circuit current (kA)
I_{st}	STATCOM current (kA)
P	Transmission line active power (MW)
P_{st}	STATCOM active power (MW)
Q	Transmission line reactive power (MVAR)
Q_{st}	STATCOM reactive power (MVAR)
R_f	Fault resistance (Ω)
V	Source voltage (kV)
V_r	Receiving end voltage (kV)
V_{ref}	Reference voltage (p.u.)
V_s	Sending end voltage (kV)
V_{sc}	Short circuit voltage (kV)
V_{st}	STATCOM terminal voltage (kV)
v_t	PCC terminal voltage (p.u.)
X_f	Fault reatance (Ω)
X_t	Coupling transformer reactance (Ω)
Z_f	Fault impedance (Ω)
Z_{Relay}	Apparent impedance seen by the relay (Ω)

CHAPTER 1

Introduction

There is an everlasting demand for electric power. The generated power is transferred through transmission lines to the load centres. As power transfers grow, the power system becomes increasingly more complex to operate and the system can become less secure for riding through the major outages. It may lead to large power flows with inadequate control, excessive reactive power in various parts of the system, large dynamic swings between different parts of the system and subsequently result in voltage instability and collapse. Thus ac transmission network requires dynamic reactive power control to maintain satisfactory voltage profile under varying load conditions and transient disturbances (K. R. Padiyar and Kulkarni, 1997). This can be achieved by incorporating Flexible AC Transmission System (FACTS) devices into existing power grids. A brief overview of FACTS devices is presented in the following section.

1.1 Flexible AC Transmission System (FACTS) Devices

The use of FACTS controllers in power system has been of worldwide interest in recent years. The integration of FACTS devices enhance the controllability, stability, power transfer capability and power quality. They control the interrelated parameters that govern the operation of transmission systems including impedance, current, voltage and phase angle. By providing added flexibility, FACTS controllers can enable a line to carry power closer to its thermal rating (Hingorani and Gyugyi, 1999; Paserba, 2003).

1.1.1 Applications of FACTS Devices

An electric power system suffers from several operating problems such as system instability, high transmission losses, voltage limit violations, under utilization of transmis-

sion line capacity and cascade tripping. The cause for these abnormalities is attributed to uncontrolled active and reactive power flows in the system. Traditionally this problem has been solved by building new power plants and transmission lines. But, this solution is costly due to the spurt in prices of land and construction materials, apart from long gestation period involved in the process. Whereas, FACTS devices provide a better adaptation to varying operational conditions and improve the usage of existing resources. The basic applications of FACTS devices are (Acha *et al.*, 2002; Zhang *et al.*, 2012):

- Power flow control
- Increase of transmission capability
- Voltage control
- Reactive power compensation
- Stability improvement
- Power quality improvement
- Interconnection of renewable and distributed generation.

There are varieties of FACTS devices developed in the recent years. In general, they are classified based on the way in which they are interfaced with the power system as, series controllers, shunt controllers and combined series-shunt controllers. But the scope of this research work is confined to shunt type of FACTS device known as Static Synchronous Compensator (STATCOM). The following paragraph gives a brief account of various aspects of STATCOM.

1.2 Static Synchronous Compensator (STATCOM)

The progress in the field of power electronics, particularly Gate Turn-Off (GTO) based devices, have introduced a new family of shunt FACTS controllers viz. STATCOM . A STATCOM injects /absorbs required reactive current into/from the transmission system so as to maintain the voltage at the point of common coupling (PCC) to a set reference value. This feature is exploited to control the specific parameters of an electric power system to enhance transmittable power, which is the ultimate objective of providing

reactive shunt compensation in a transmission system.

The STATCOM can be realized based on a voltage sourced or current sourced converter topologies. But, from an overall cost point of view, the voltage-sourced converters (VSC) seem to be preferred (Hingorani and Gyugyi, 1999; Jain *et al.*, 2009). There are numerous toplogies available for implementing VSC. In comparison to other VSC topologies, the multi-pulse converter has a superior total harmonic distortion (THD) for a given number of semiconductor switches (Soto and Green, 2002). Most industrial practices are to deploy 48 pulse configuration (Lee *et al.*, 2003; Schauder *et al.*, 1998; Wenhua *et al.*, 2000; Uzunovic *et al.*, 2001; Zhou *et al.*, 2005; El-Moursi and Sharaf, 2005). The THD of output voltage is in compliance with the IEEE 519 standard. The STATCOM built with this type of inverter topology can be directly connected to the transmission system without any filtering requirement. Therefore a three level, 48 pulse inverter based STATCOM has been modelled in EMTDC / PSCAD and its dynamic performance is analysed in this thesis.

The STATCOM's main function is to regulate voltage magnitude at the PCC. This functionality is achieved by implementing a real time closed loop digital controller. The controller is responsible for generating gating commands for the switching devices in such a way that, the STATCOM maintains the correct level of reactive output current to regulate the PCC voltage to a set reference value. A controller based on decoupled current control strategy (El-Moursi and Sharaf, 2005) has been modelled in EMTDC/PSCAD and tuned to support the functionality of STATCOM. The methodology followed in modeling is narrated.

Another important issue is the selection of proper location for the placement of STATCOM. The placement of STATCOM controller depends on the application for which it has been installed. The midpoint placement is the best location for shunt connected STATCOM, specifically to meet the purpose of increasing the power transfer capability of long transmission lines. This is because, each side of the FACTS device address only half the transmission line impedance. Whereas, a STATCOM placed at the transmission line end has to deal with the full line impedance. Also mid point placement

of STATCOM controller, is more effective for dynamic voltage control, enhances transient stability and dampens power oscillations (Hingorani and Gyugyi, 1999; Kowsalya *et al.*, 2009; Ooi *et al.*, 1997). For this reason the STATCOM connected at the midpoint of transmission line is considered in this work.

The installation of STATCOM helps to load transmission lines up to thermal limit and enhance grid reliability, but on the other hand it poses challenges for protection engineers. This is because, inclusion of STATCOM changes dynamic behaviour of the power system and many sub-systems are affected, including the protective systems (Padiyar, 2007; Miller, 1982). Therefore, it is essential to study effects of FACTS devices on the protective systems. Especially the distance relay, which is the main protective device at EHV and HV level transmission systems deserves special attention. This has become important research interest and several researchers have reported their investigations. Section that follows present literature survey on this topic.

1.3 Influence of STATCOM on Distance Protection

This section presents the literature review on the influence of STATCOM on the performance of the distance relay. Finally, the outcome of literature survey is summarized at the end of this section. Many researchers have reported impacts of shunt compensation including FACTS controllers on the performance of distance relays. In (El-Arroudi *et al.*, 2002) influence of 300 MVAR STATCOM was analysed, verified through simulation and showed that distance relay under reached at first zone. A 160 MVA STATCOM has been integrated with the 138 kV transmission system to study the influence of STATCOM on the distance relay operation in (Zhou *et al.*, 2005). This study revealed relationship between operating mode and the nature of reach problem exhibited by the relay. Relay under-reached when the STATCOM supplies the reactive power (capacitive mode), and over-reached when the STATCOM consumes the reactive power (inductive mode). In (Albasri *et al.*, 2007; Sidhu *et al.*, 2005; Albasri *et al.*, 2006) the performance of various distance protection schemes including both stand alone and the advanced

channel aided schemes on transmission lines has been presented. Study revealed that the relay with the channel-aided schemes perform better as compared to the stand-alone scheme. However, authors have also reported that channel-aided schemes fail to provide reliable operation for all types of faults in midpoint shunt-FACTS compensated transmission system.

The literature survey point out that the STATCOM connected transmission lines are vulnerable to apparent impedance measurement errors, and none of the papers have suggested remedy to mitigate the influence of STATCOM on the performance of distance relays. Literature survey also divulge that the traditional protection schemes are not proficient in such applications. However such undesired operations can be corrected through the deployment of futuristic concept, popularly known as; "adaptive relaying schemes".

The research work reported here proposes new adaptive relaying scheme for the protection of STATCOM connected transmission lines. Following section enumerates the research objectives of this thesis,

1.4 Objectives of the Research Work

- Identifying a suitable model power system configuration to study the impact of midpoint STATCOM on the performance of the distance relay.
- To develop transient behavioral model of selected model power system using EMTDC / PSCAD, which can depict true power system transients. Study the interaction between STATCOM controller and the power system during normal and abnormal conditions, using both analytical and simulation methods.
- Development of adaptive distance relaying schemes, to achieve reliable relay operation and verification of the proposed scheme through simulations.
- To develop numerical adaptive distance relay hardware using modern digital signal controller(DSC).
- Real time performance evaluation of newly developed adaptive distance relay using hardware in the loop (HIL) method of testing.

1.5 Thesis Organisation

The research work carried out to meet the above objectives has been presented systematically in the thesis. A brief skeletal structure of the thesis along with summary of content in each chapter is presented in paragraphs that follow:

Chapter 1 gives the insight about the research area and aimed at familiarisation of the issues associated with the topic. The chapter provides an overview of topics such as current power system scenario, role of FACTS controllers in power system, voltage source converter topologies with particular emphasis on high power applications and adaptive relaying applied to transmission line protection. Literature review, encompassing the mid point shunt compensation and its effect on the performance of the distance protection is included, followed with narration on scope and objectives of research work. Following this, essence of the work and the contents of different chapters that follow, are summarised.

Transient behavioural modelling of a 48 pulse $\pm$100MVA STATCOM, based on three level neutral point clamped (NPC) voltage source inverter (VSI) is detailed in the chapter 2. Complete mathematical analysis of inverter has been carried out, equations describing the output voltage of the individual stages has been presented with their respective waveforms. A decoupled current controller is implemented to operate the STATCOM in both voltage control and reactive power control modes for a wide range of varying system conditions by considering a realistic study system. Further, results of EMTDC/PSCAD simulations, conducted to assess the transient performance of STATCOM controller, are furnished in this chapter.

Chapter 3 investigates the influence of STATCOM on the the distance relay operation. This work is carried out in two phases. In the first phase, a numerical distance relay model is developed for the protection of transmission line using EMTDC/PSCAD simulation package. In the second phase, the STATCOM is integrated to the power system at the midpoint of the transmission line in order to study its influence on the distance protection. The mathematical equations describing the apparent impedance er-

ror due to the presence of STATCOM are derived. Also, extensive simulation results of tests conducted on the EMTDC/PSCAD study model are included in the same chapter.

In chapter 4, development of a new adaptive distance relaying schemes, to mitigate the effect of midpoint STATCOM is described. Adaptive equations have been developed to correct the measured apparent impedance error in the presence of STATCOM. The performance of adaptive schemes are evaluated for different faults at various locations through simulations. Further, results pertaining to a comparative analysis of the adaptive relay with the conventional distance relay are also included.

Chapter 5 describes the development of a fully functional, adaptive distance relay hardware, using state of the art 32 bit, digital signal controller TMS320F28335 and ADS8556 a simultaneous sampling type analog to digital converter. A test bench comprising of Doble F6150 power system simulator has been setup to assess the performance of the adaptive distance relay in real time. This constitutes Hardware In Loop setup. The HIL test results show that, newly developed adaptive relay provides reasonable protection for the STATCOM connected transmission lines by mitigating reach problems. All the above aspects are detailed in this chapter.

Finally, in Chapter 6, the conclusions and the contributions of this research work are highlighted and future scope for research is summarised.

CHAPTER 2

Transient Behavioural Modelling of STATCOM

2.1 Introduction

In recent years, power systems have been operating at the higher end of their stability limit, in-order to meet the ever-increasing power demand. Such operating condition results in some major disorders in the power system, like poor voltage regulation, uncontrolled power flow, transient instability, etc. On the contrary, in-spite of such operating conditions, the power system has to honor the grid code specifications.

Integration of FACTS devices into power systems, helps to confront these operational ailments quickly in an elegant manner. Among the FACTS family, STATCOM is a shunt connected device, which has been widely adopted to regulate voltage at the PCC. A VSC is the basic building block of many FACTS devices including STATCOM. At present, VSC can be realized using gate turn-off thyristor (GTO) devices which have self turn off and bidirectional conduction capability. The VSC provides maneuverability to control the magnitude, the phase angle and the frequency of the output voltage, which is most desirable feature from FACTS controller view point.

Many types of VSC configurations have been reported in the literature such as multipulse, multilevel and a combination of multipulse and multilevel converters (Rodriguez *et al.*, 2002; Geethalakshmi and Dananjayan, 2010). A brief overview of all the aforementioned configurations are discussed in this chapter. A forty eight pulse VSC based on both multipulse and multilevel inverter configurations has been developed. It is observed that, this type of inverter configuration produces nearly sinusoidal output voltage with THD of 3.81%. The VSC so configured in EMTDC / PSCAD is integrated to function with 100MVA STATCOM transient behavioural model. This forms first phase of research work.

Regulation of voltage at PCC is the prime responsibility of the STATCOM controller. Its dynamic performance depends on the control technique employed in the controller. It is desired that the controller respond quickly to all the operating conditions of the power system while maintaining the stability. A complete closed loop decoupled reactive current control technique is used to implement the STATCOM controller (El-Moursi and Sharaf, 2005).

In-order to assess the benefits derived from STATCOM installation, evaluation tests are conducted. For this purpose, a realistic study model has been developed in EMTDC/ PSCAD simulation environment. Various system conditions are simulated using proper load excursion model. The simulation results indicate that, STATCOM plays a vital role in regulation of voltage at PCC to a set reference value. Thereby it enhances the power transfer capacity of the transmission system.

This chapter presents the development of transient behavioural model of $\pm$ 100 MVA STATCOM, and the results of evaluation tests conducted to study its performance under varying system conditions. Overview of the various converter topologies are discussed in the following sections.

2.2 Multipulse Converters

The term "multipulse" is not defined very precisely in the literature (Paice and Society, 1996). A basic three phase converters switching at fundamental frequency are known as six pulse inverters. However, by popular usage in the power electronic industry, converters operating in a three-phase system providing more than six levels of dc per cycle are known as multipulse converters. Multipulse methods involve multiple converters with a common dc supply. Phase shifting transformers (PST) are indispensable part of these converters and provides means for cancellation of specific harmonic current pairs, for example, the 5^{th} and 7^{th} harmonics, or 11^{th} and 13^{th} and so on. In this way, multipulse converters give a simple and effective technique for reducing converter harmonics. Usually fundamental frequency switching (FFS) is employed in such con-

figuration. In this type of switching technique, each semiconductor device is limited to one turn-on and one turn-off per power cycle. Even though, this switching technique is complex, it offers other advantages like, high semiconductor switch utilization and low switching losses. It is current practice to use several six-pulse VSCs, arranged to form a multipulse structure, to achieve better waveform quality and higher power ratings. Hence they have been widely used in high power applications in the FACTS and HVDC systems (Hingorani and Gyugyi, 1999; Acha *et al.*, 2002).

2.2.1 Multilevel Converters

The traditional two level VSI produces a square wave output as it switches the dc voltage source on and off. In recent years, industry has begun to demand higher power equipment, which now reaches the Megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. It is difficult to connect a single power semiconductor switch directly to medium voltage range including 2.3, 3.3, 4.16, or 6.9 KV. For these reasons, a new family of multilevel inverters have emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors switches and capacitor voltage sources. They produce the output voltages with stepped waveforms. The commutation of the switches permits addition of the capacitor voltages, which reach high voltage at the output, while the switches have to withstand only reduced voltages. By increasing the number of levels in the inverter, the output voltages have more steps resulting in a staircase waveform, which has reduced THD. However, increasing number of levels increases the control complexity and introduces voltage imbalance problems. In-spite of these limitations following are the attractive features which makes them still popular: (Rodriguez *et al.*, 2002).

- They can generate output voltages with extremely low distortion and lower $\frac{dv}{dt}$.
- They draw input current with very low distortion.
- They can operate with a lower switching frequency.

2.2.2 Combined Multipulse and Multilevel Converter Topology

The major problem, with the multipulse inverter, is the requirement of magnetic interfaces, constituted by complex zig-zag phase shifting transformers (Wu, 2006), which increases the cost, but instead has a merit of less control complexity and low THD. On the other hand, Multi level inverter is cheaper but has high control complexity and high THD. Hence, in-order to obtain an optimal inverter topology, a trade off between the cost and the complexity in control is necessary. Therefore, a hybrid topology, involving both multipulse and multilevel inverter configurations, extracting the advantages of both will be most attractive solution. The section that follow presents the development of transient behavioural model of 48 pulse VSC based on combined multipulse and multilevel inverter configurations.

2.3 Development of Transient Behavioural Model of 48 Pulse VSC

In the present work, a 100 MVA, 48 pulse inverter operation is achieved, by connecting four identical three phase, three level inverter bridges to transformers whose outputs are phase-displaced with respect to one another. Even though this inverter topology has been in use for quite some time now, detailed mathematical analysis has not been reported. Work reported here involves building functional equations and modeling of 48 pulse inverter from basics. The following section discusses the operation of three level inverter, which is the primitive building block in the process of realizing the 48 pulse inverter architecture.

2.4 Three Level Neutral Point Clamped (NPC) Inverter

Three-level inverters are preferred in high power application as they offer several advantages over the traditional two-level inverter topology. This topology is popularly known

as NPC inverter. The three-phase three-level NPC inverter configuration is shown in figure 2.1.

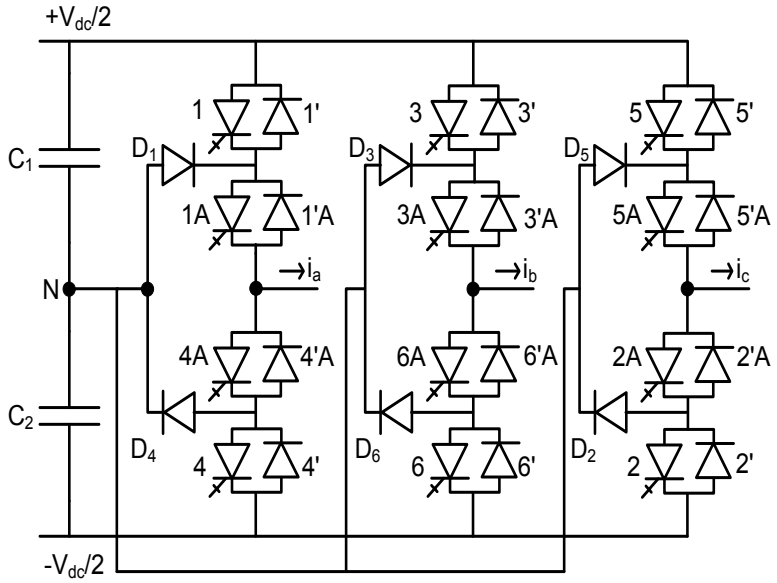


Figure 2.1: Three level NPC inverter (Paice and Society, 1996)

All three legs of the inverter are connected across the same dc bus bars and the clamping diodes connected to the same midpoint N of the dc capacitor. It is seen that each half of the phase leg is split into two series connected valves 1-1′ and 1A-1′A. The midpoint of the split valves is connected by diodes D_1 and D_4 to the midpoint N as shown. Doubling the number of valves from two to four per phase leg with the same voltage rating would double the dc voltage and hence the power capacity of the converter. Thus only the addition of the clamping diodes adds to the inverter cost (Hingorani and Gyugyi, 1999). Also this topology enables to use low voltage GTO modules comfortably, as the switches are only subjected to half of the dc bus voltage.

2.4.1 Working of Three Level NPC Inverter

The NPC inverter can produce three voltage levels at the output, determined by the switching states of the switching devices in each phase legs. The switching states and the corresponding output of a single three level leg are listed in the table 2.1. From

Table 2.1: Switching states of a three level inverter

Switching device	Output voltages $\frac{+V_{dc}}{2}$	zero	$\frac{-V_{dc}}{2}$
1	On	Off	Off
1A	On	On	Off
4A	Off	On	On
4	Off	Off	On

the switching states, it can be seen that when 1 and 1A are turned on, the output is connected to positive dc bus, when 1A and 4A are on, the output is zero; and when 4A and 4 are on, the output is connected to negative dc bus . When a pair of switches is turned on the other pair of switches must be turned off to avoid the short circuit of the bridge. To clamp the voltage, two extra clamping diodes D_1 and D_4 as shown in figure 2.1, are required to connect the dc bus mid-point to the load applying zero volts. They also allow the current to flow in either direction, when the converter operates in the freewheeling mode. The three-level inverter topology, shown in the figure 2.1 is implemented using GTO based switch model, readily available in the EMTDC/PSCAD package. Switching signals for the GTOs are derived using the fundamental frequency switching(FFS) technique. Details of the FFS scheme is furnished in following section.

2.4.2 Gate Pulse Logic for the Three Level NPC Inverter

All power electronic converters, require appropriate switching scheme for their desired operation. In this work FFS method is implemented for the purpose of switching pulse generation. Figure 2.2 shows the block diagram of three-level NPC inverter along with firing pulse generator block.

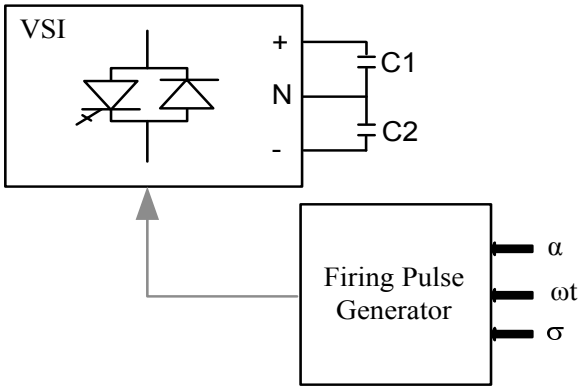


Figure 2.2: Firing pulse generator for NPC inverter

There are three inputs for the firing pulse generator namely, STATCOM controller output (α), Phase locked loop synchronizing angle (ωt) and the fixed conduction angle over half cycle (σ). Typical firing pulse timing sequence generated for a single limb is as shown in the figure 2.3. Where 1, 1A, 4A and 4 are the switches of the first limb as shown in the figure 2.1. A dotted line below the switch indicate the 'ON' state of the respective switch. It can be observed from the same figure that, at any given point of time two switches are in the 'ON' state. The output voltage produced by a pair of conducting switches is indicated in the table 2.1. The duration of the +Vdc or -Vdc level, can be adjusted between 0 and 180 degrees by varying the conduction angle (σ). The firing pulses for the other two limbs of the inverter are phase shifted by -120^0 and -240^0 respectively from the first leg. This inverter works as a two level inverter by choosing σ equal to 180 degrees as shown in the figure 2.4. For all other conduction angles, inverter produces three level output. Figure 2.5 shows the inverter output voltages for $\sigma = 172.5^0$.

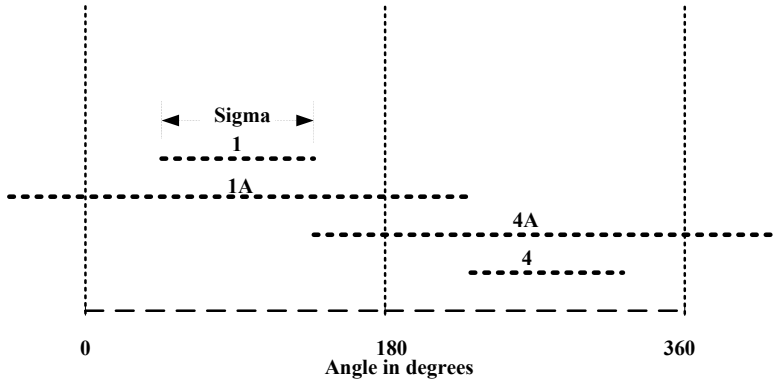


Figure 2.3: Firing pulse timing diagram

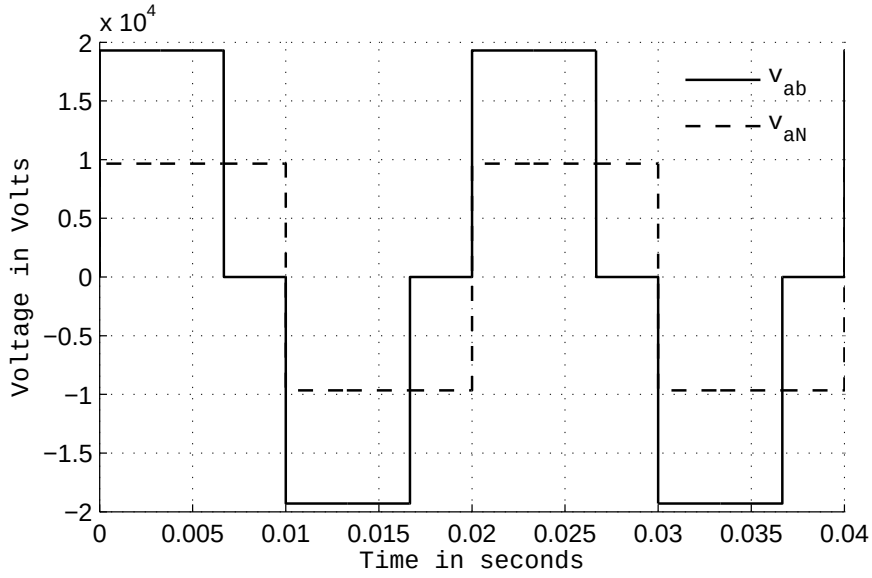


Figure 2.4: NPC inverter voltages for $\sigma = 180^0$

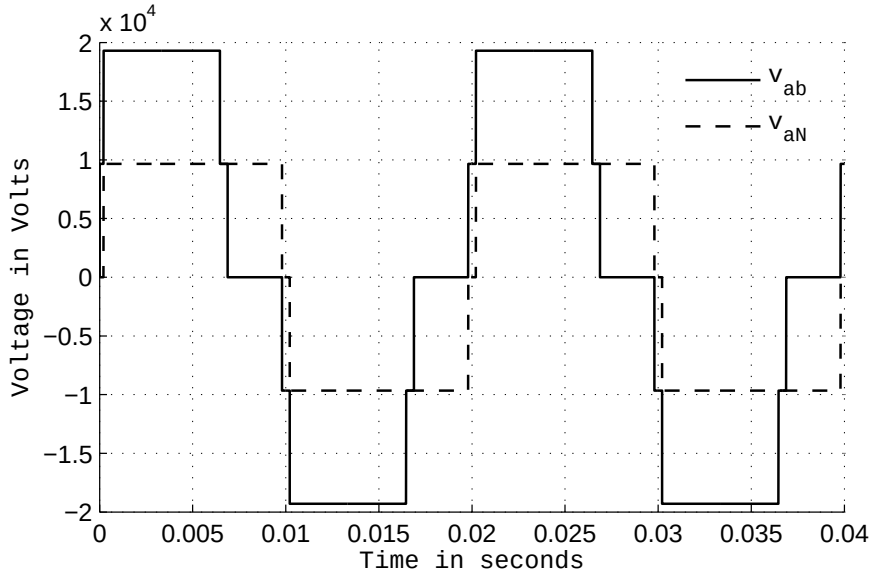


Figure 2.5: NPC inverter voltages for σ= 172.5^0

The line-to-line voltages, v_{ab}(t) shown in the figure 2.4 can be mathematically expressed as ,

$$v_{ab}(t) = \sum_{n=1}^{\infty} v_{ab_n} \sin\left(n\omega t + \frac{n\pi}{6}\right) \tag{2.1}$$

Where,

$$v_{ab_n} = \frac{4v_{dc}}{n\pi} \cos\left(\frac{n\pi}{6}\right) \tag{2.2}$$

$$\forall n = 6r \pm 1, r = 0, 1, 2, ... \tag{2.3}$$

Expanding the equation 2.1 by Fourier series yields,

$$\begin{aligned} v_{ab}(t) = & \frac{2v_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 30^0) - \frac{1}{5}\sin(5\omega t + 150^0) - \frac{1}{7}\sin(7\omega t + 210^0)\right. \\ & + \frac{1}{11}\sin(11\omega t + 330^0) + \frac{1}{13}\sin(13\omega t + 30^0) - \frac{1}{17}\sin(17\omega t + 150^0) \\ & \left. - \frac{1}{19}\sin(19\omega t + 210^0) + \ldots\right) \end{aligned} \tag{2.4}$$

The line to neutral voltage, shown in the figure 2.4 , can be mathematically expressed

as,

$$v_{an}(t) = \sum_{n=1}^{\infty} v_{an_n} \sin(n\omega t) \tag{2.5}$$

where,

$$v_{an_n} = \frac{4v_{dc}}{3n\pi}\left(\sin\left(\frac{n\pi}{3}+1\right)\right) \tag{2.6}$$

It can also be expressed in the other form as,

$$v_{an_n} = \frac{v_{ab_n}}{(-1^r)\sqrt{3}} \tag{2.7}$$

equation 2.7 $\implies$

$$v_{ab_n} = (-1)^r\sqrt{3}v_{an_n} \tag{2.8}$$

by substituting equation 2.7 in equation 2.5 we can write,

$$v_{an}(t) = \frac{1}{\sqrt{3}}\sum_{n=1}^{\infty}\frac{v_{ab_n}}{(-1)^r}\sin(n\omega t) \tag{2.9}$$

Expanding equation 2.5 by Fourier series yields expression for line to neutral voltage $v_{an}(t)$ i.e., :

$$\begin{aligned} v_{an}(t) = &\frac{2v_{dc}}{\pi}\left(\sin(\omega t)+\frac{1}{5}\sin(5\omega t)+\frac{1}{7}\sin(7\omega t)+\frac{1}{11}\sin(11\omega t)+\frac{1}{13}\sin(13\omega t)\right. \\ &\left.+\frac{1}{17}\sin(17\omega t)+\frac{1}{19}\sin(19\omega t)+\frac{1}{23}\sin(23\omega t)+\ldots\right) \end{aligned} \tag{2.10}$$

The harmonic spectrum of line to line voltage is shown in the figure 2.6. It can be seen that, the harmonic magnitude of the individual component is inversely proportional to their respective harmonic orders.

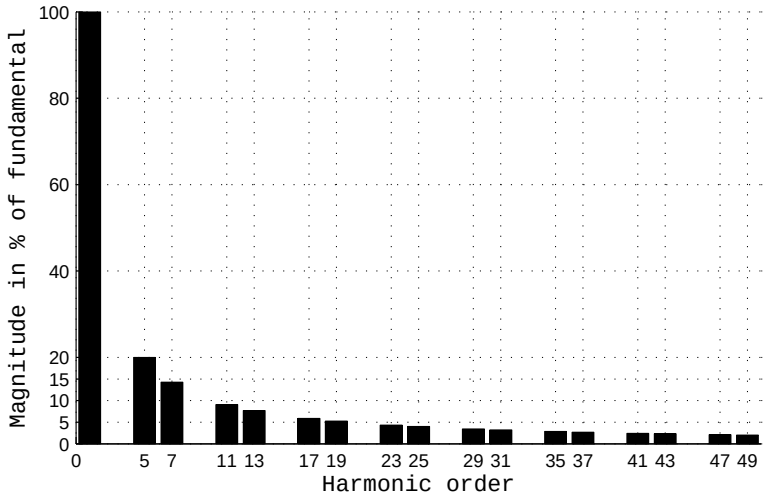


Figure 2.6: Harmonic spectrum of the line to line voltage

In-spite of simplest architecture, the six-pulse VSC cannot be used in high power applications by virtue of its high harmonic content. But, it is possible to improve the harmonic performance of the converter by means of multipulse inverter topology. In this method two or more three-phase, six-pulse converters are combined to produce superior waveform with lesser THD. In the next section twelve-pulse configuration obtained by combining two six-pulse VSCs is discussed in detail.

2.4.3 Twelve Pulse Operation

Twelve pulse VSC operation is very useful from the power system application point of view. Because, this is the basic configuration required for implementing FACTS devices like STATCOM. The FACTS controllers based on such a topology can be interfaced to the power system with minimal filtering requirements, due to better harmonic performance. In this section, the development of twelve pulse inverter is narrated with help of the mathematical equations pertaining to the output voltage waveforms.

It has been shown in the previous section, that the phase-phase voltage and phase-neutral voltages described by the equations 2.4 and 2.10 respectively, are 30° out of phase with each other. If this phase shift is corrected, all harmonics, other than $\forall n =$

$12r \pm 1$, where r=0,1,2,..., (i.e., 5^{th}, 7^{th}, 17^{th}, 19^{th}....) contained in the six pulse VSC output can be canceled. This feature is exploited, in multipulse converter to reduce the harmonics (Sen, 1999).

The circuit arrangement to achieve twelve pulse operation is shown in the figure 2.7 (Marín, 2001). In this configuration, phase-phase voltages of two three-phase, identical six pulse inverters are connected to secondaries of Y-Y and Y-Δ transformers. The basic idea is to utilize the inherent phase shift of 30° between the Y-Y and Y-Δ transformers to cancel the harmonics, not included in the set, $\forall n = 12r \pm 1$. Both the inverters are fed from the same dc bus.

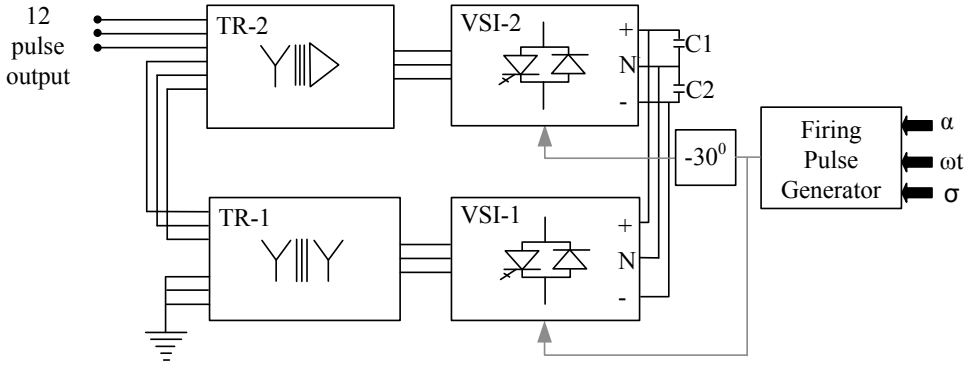


Figure 2.7: Circuit arrangement to produce 12 pulse output voltage

The phase-phase voltage waveform across the primary of transformer TR-1 $v_{ab_{t1}}$,can be expressed by the equation 2.11.

$$\begin{aligned} v_{ab_{t1}} = & \frac{2kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 30^0) - \frac{1}{5}\sin(5\omega t + 150^0) - \frac{1}{7}\sin(7\omega t + 210^0)\right. \\ & + \frac{1}{11}\sin(11\omega t + 330^0) + \frac{1}{13}\sin(13\omega t + 30^0) - \frac{1}{17}\sin(17\omega t + 150^0) \\ & \left. - \frac{1}{19}\sin(19\omega t + 210^0) + \ldots\right) \end{aligned} \tag{2.11}$$

Where k is the transformation ratio of transformer.

The firing pulse for the second converter, is delayed by 30° with respect to the first inverter. This will cause the fundamental components of both inverters, to be added up in phase on the primary side. The phase-phase voltages of second converter can be represented by its Fourier series as

$$v_{ab_{conv2}}(t) = \sum_{n=1}^{\infty} v_{ab_n} \sin(n\omega t) \tag{2.12}$$

Expanding the Fourier series yields equation 2.13

$$\begin{aligned} v_{ab_{conv2}}(t) = \quad & \frac{2v_{dc}\sqrt{3}}{\pi}\Bigg(\sin(\omega t) - \frac{1}{5}\sin(5\omega t) - \frac{1}{7}\sin(7\omega t) + \frac{1}{11}\sin(11\omega t) \\ & + \frac{1}{13}\sin(13\omega t) - \frac{1}{17}\sin(17\omega t) - \frac{1}{19}\sin(19\omega t) + \frac{1}{23}\sin(23\omega t) \\ & + \dots \Bigg) \end{aligned} \tag{2.13}$$

The phase-phase voltages of the second converter, are applied to the secondary of Y-Δ transformer. The phase-neutral ($v_{an_{t2}}$) and phase-phase voltages ($v_{ab_{t2}}$) at the primary of the second transformer TR-2, can be expressed by the equations, 2.14 and 2.15 respectively,

$$v_{an_{t2}}(t) = \frac{k}{\sqrt{3}} \sum_{n=1}^{\infty} v_{an_n} \sin(n\omega t) \tag{2.14}$$

$$v_{ab_{t2}}(t) = \frac{k}{\sqrt{3}} \sum_{n=1}^{\infty} \frac{v_{ab_n}}{(-1)^r} \sin\left(n\omega t + \frac{n\pi}{6}\right) \tag{2.15}$$

$$\forall n = 6r \pm 1, r = 0, 1, 2, \dots$$

equation 2.15 can also be written as,

$$v_{ab_{t2}}(t) = \sqrt{3}k \sum_{n=1}^{\infty} v_{an_n} \sin\left(n\omega t + \frac{n\pi}{6}\right) \tag{2.16}$$

equation 2.16 can be expanded as,

$$v_{ab_{t2}}(t) = \frac{2kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 30^0) + \frac{1}{5}\sin(5\omega t + 150^0) + \frac{1}{7}\sin(7\omega t + 210^0) + \frac{1}{11}\sin(11\omega t + 330^0) + \frac{1}{13}\sin(13\omega t + 30^0) + \frac{1}{17}\sin(17\omega t + 150^0) + \frac{1}{19}\sin(19\omega t + 210^0) + \frac{1}{23}\sin(23\omega t + 330^0) + \ldots\right) \tag{2.17}$$

By virtue of series connected primaries, the voltages of both the transformers will add up to produce the twelve pulse waveform.The equation 2.18 represents the resultant twelve pulse phase-phase output voltage waveform obtained by adding equations 2.11 and 2.17. Figure 2.8 shows the process of twelve pulse waveform generation graphically.

$$v_{ab_{12}}(t) = \frac{4kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 30^0) + \frac{1}{11}\sin(11\omega t + 330^0) + \frac{1}{13}\sin(13\omega t + 30^0) + \frac{1}{23}\sin(23\omega t + 330^0) + \ldots\right) \tag{2.18}$$

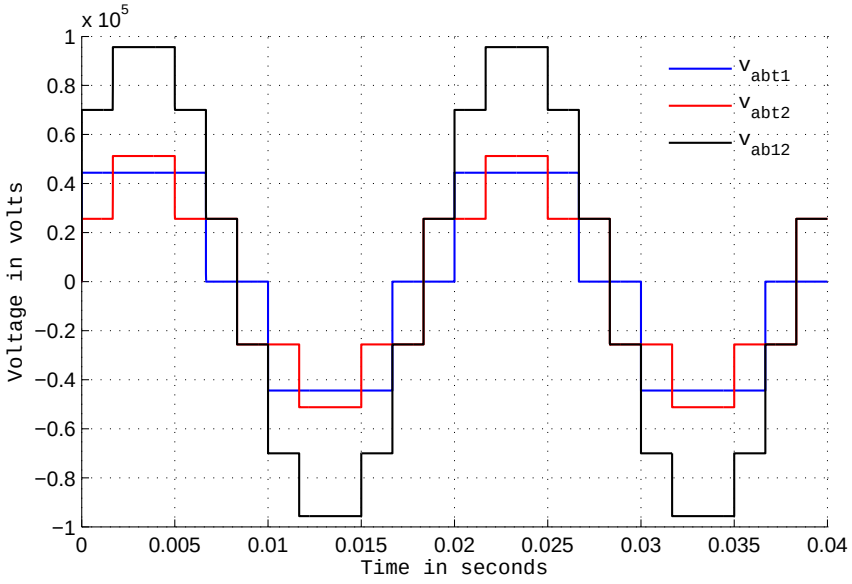


Figure 2.8: Twelve pulse output voltage waveform

The harmonic spectrum of this waveform is shown in the figure 2.9. It can be seen that, all 5+12n and 7+12n harmonic components are eliminated, from the line-line output voltage waveform, due to 30 degree phase shift between the two converters output.

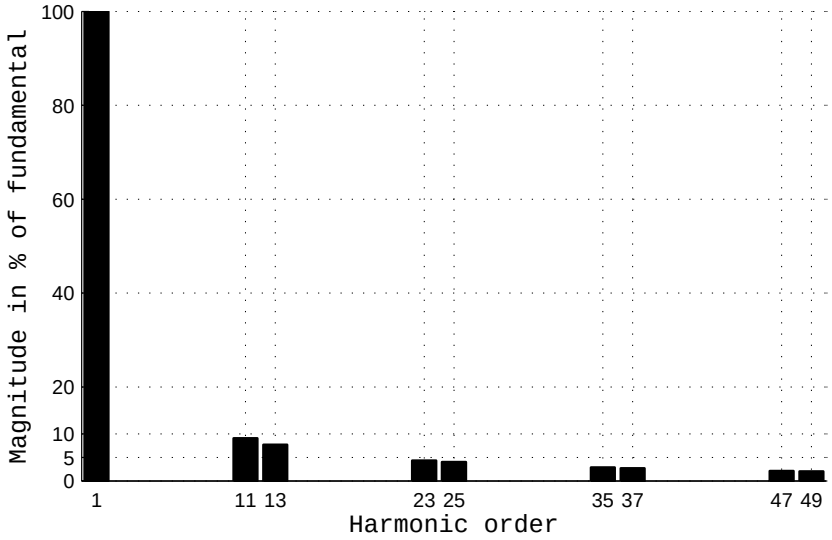


Figure 2.9: Harmonic spectrum of the 12 pulse line to line voltage waveform

Even though the harmonic performance of the twelve pulse inverter is better than six pulse inverter, it can not be interfaced to the power system directly. Hence, more six pulse inverters are combined to achieve higher pulse operation. Now a days, forty eight pulse operation is preferred which has a harmonic content in the order of n = 48r $\pm$1 (where r=0,1,2,...). Therefore, to cope with the present day operating practices, forty eight pulse inverter has been implemented in this work. The details of such configuration is presented in the following section.

2.4.4 Forty Eight Pulse operation

Conventionally, eight six pulse inverters are combined with their respective phase-shifting transformers to produce forty eight pulse output voltage waveform. This topology is costly and quite complex owing to the transformer interconnections. In this

research work forty eight pulse operation is obtained through the twenty four pulse configuration. This is possible by the use of three-level NPC inverter. This topology enjoys the benefits of both configurations and referred as the combined multipulse-multilevel inverter topology. The harmonic performance of this topology is evaluated through EMTDC/PSCAD simulations. The results show that this topology offers almost same voltage THD as that of forty eight pulse configuration.

The circuit arrangement of a twenty four pulse, $\pm$ 100 MVA, 138 kV RMS inverter is shown in the figure 2.10 (Xi and Bhattacharya, 2008; Geethalakshmi and Dananjayan, 2010).

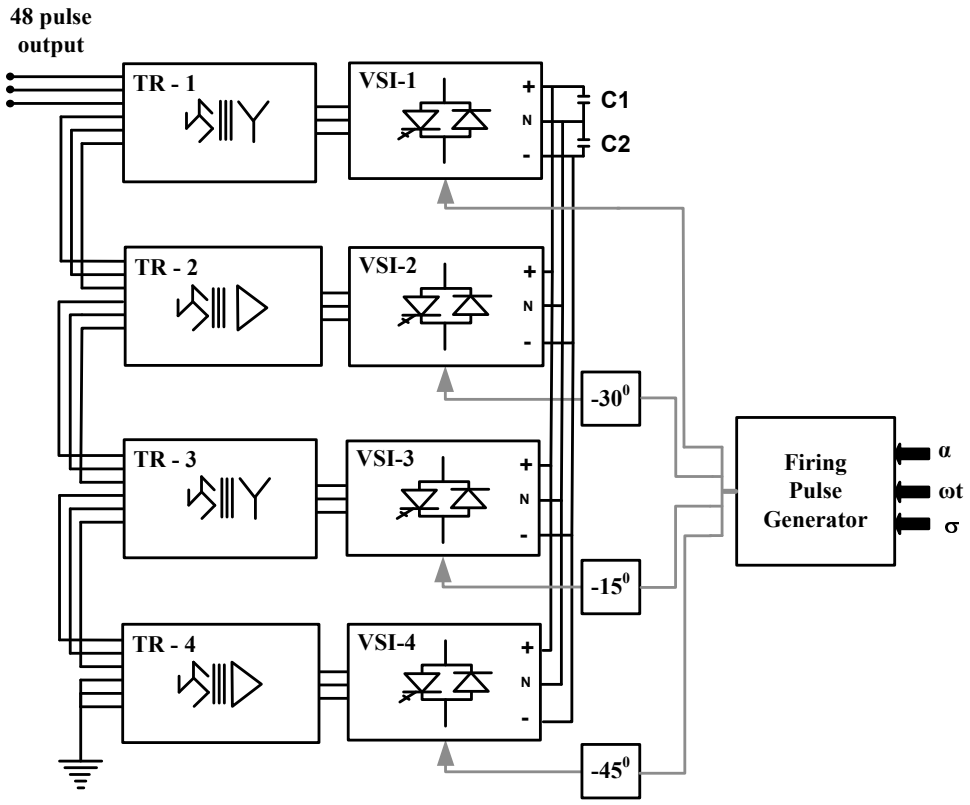


Figure 2.10: Circuit arrangement to Produce 24 pulse output voltage (Geethalakshmi and Dananjayan, 2010)

It consists of four three-level inverters, whose outputs are connected to respective phase shifting transformers. The capacity of each transformer is 25 MVA. The voltage ratio of Y-Y and Y-Δ transformers are 34.5kV:15kV and $\frac{34.5kV}{\sqrt{3}}$:15kV respectively.

The first and second converters, with their respective phase shifting transformers, will produce first twelve pulse output. Similarly, third and fourth converters, with their respective phase shifting transformers, generates second twelve pulse output. These two twelve pulse output waveforms, are phase shifted by 15^0 from each other, to obtain 24-pulse output voltage. In order to match the harmonic performance of forty eight pulse inverter, appropriate conduction angle (σ) which selectively eliminates 23^{rd} and 25^{th} harmonic components has been selected. The generation of forty eight pulse output is narrated analytically in the the subsequent paragraphs.

As discussed above, a phase shift of 15° has to be applied between the two twelve pulse waveforms to produce twenty four pulse voltage waveform. This is met by applying symmetrical phase shifts, of +7.5° and -7.5°, to the two pairs of converters. The firing pulse pattern, is properly phase shifted as shown in the table 2.2, so that, the fundamental components of all the inverters are added up on the primary side.

Table 2.2: Phase shift required to produce 48 pulse output voltage

Phase shifting transformer	Phase shift produced by the PST (degrees)	Shift in gate pulse train (degrees)
1	+7.5	0
2	+7.5	-30
3	-7.5	-15
4	-7.5	-45

A phase shift of $+\frac{\pi}{24}$ is applied to the output of the first and second converter, through the respective phase shifting transformers. The line-line voltage, across the primary side of the first transformer, can be mathematically represented by equation 2.19.

$$v_{ab_{t1}}(t) = k\sum_{n=1}^{\infty} v_{ab_n} \sin\left(n\omega t + \frac{n\pi}{6} - \frac{\pi i}{24}\right) \tag{2.19}$$

Where,

$$v_{ab_n} = \frac{4v_{dc}}{n\pi}\cos\left(\frac{n\pi}{6}\right)$$

i=1 for positive sequence harmonics.

i=-1 for negative sequence harmonics.

$\forall n = 6r \pm 1, r = 0, 1, 2, ...$

Expanding the equation 2.19 by using Fourier series yields,

$$\begin{aligned} v_{ab_{t1}}(t) = &\frac{2kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0) - \frac{1}{5}\sin(5\omega t + 157.5^0) - \frac{1}{7}\sin(7\omega t + 202.5^0) + \right. \\ &\frac{1}{11}\sin(11\omega t + 337.5^0) + \frac{1}{13}\sin(13\omega t + 22.5^0) - \frac{1}{17}\sin(17\omega t + 157.5^0) \\ &\left. -\frac{1}{19}\sin(19\omega t + 202.5^0) + \frac{1}{23}\sin(23\omega t + 337.5^0) + \ldots\right) \end{aligned} \tag{2.20}$$

Similarly, the line-line output voltage across the second transformer can be mathematically represented as,

$$v_{ab_{t2}}(t) = k\sqrt{3}\sum_{n=1}^{\infty} v_{an_n}\sin\left(n\omega t + \frac{n\pi}{6} - \frac{\pi}{24}i\right) \tag{2.21}$$

its Fourier expansion results in equation 2.22

$$\begin{aligned} v_{abt2}(t) = &\frac{2kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0) + \frac{1}{5}\sin(5\omega t + 157.5^0) + \frac{1}{7}\sin(7\omega t + 202.5^0) + \right. \\ &\frac{1}{11}\sin(11\omega t + 337.5^0) + \frac{1}{13}\sin(13\omega t + 22.5^0) + \frac{1}{17}\sin(17\omega t + 157.5^0) \\ &\left. +\frac{1}{19}\sin(19\omega t + 202.5^0) + \frac{1}{23}\sin(23\omega t + 337.5^0) + \ldots\right) \end{aligned} \tag{2.22}$$

The first twelve pulse waveform is obtained by adding equations 2.20 and 2.22 i.e., $v_{ab_{12f}} = v_{ab_{t1}}(t) + v_{ab_{t2}}(t)$

$$v_{ab_{12f}}(t) = \frac{4kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0) + \frac{1}{11}\sin(11\omega t + 337.5^0) + \frac{1}{13}\sin(13\omega t + 22.5^0) + \frac{1}{23}\sin(23\omega t + 337.5^0) + \ldots\right) \tag{2.23}$$

It can be written in compact form as given in the equation 2.24

$$v_{ab_{12f}}(t) = k\sum_{n=1}^{\infty} v_{ab_{12n}}\sin\left(n\omega t + \frac{n\pi}{6} - \frac{\pi i}{24}\right) \tag{2.24}$$

$$v_{ab_{12n}} = \frac{4v_{dc}\sqrt{3}}{n\pi} \tag{2.25}$$

$$\forall n = 12r \pm 1, r = 0, 1, 2, \ldots$$

The pattern of first twelve pulse waveform is as shown graphically in the figure 2.11.

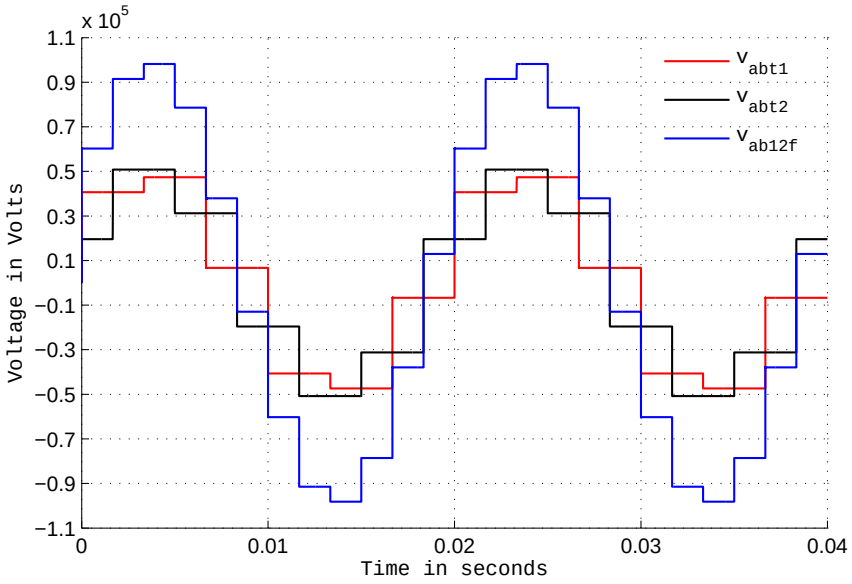


Figure 2.11: Generation of first twelve pulse waveform

Similarly phase shift of $-\frac{\pi}{24}$ is applied to the output of the third and fourth converter through the respective phase shifting transformers. The line-line voltage across the

primary side of the third transformer can be mathematically represented as

$$v_{ab_{t3}}(t) = k\sum_{n=1}^{\infty} v_{ab_n}\sin\left(n\omega t + \frac{n\pi}{12} + \frac{\pi}{24}i\right) \tag{2.26}$$

Where, i=1 for positive sequence harmonics.

i=-1 for negative sequence harmonics.

$\forall n = 6r \pm 1, r = 0, 1, 2, \ldots$

Expansion of the equation 2.26 yields,

$$\begin{aligned} v_{ab_{t3}}(t) = &\frac{2kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0) - \frac{1}{5}\sin(5\omega t + 67.5^0) - \frac{1}{7}\sin(7\omega t + 112.5^0) + \right. \\ &\frac{1}{11}\sin(11\omega t + 157.5^0) + \frac{1}{13}\sin(13\omega t + 202.5^0) - \frac{1}{17}\sin(17\omega t + 247.5^0) \\ &\left. -\frac{1}{19}\sin(19\omega t + 292.5^0) + \frac{1}{23}\sin(23\omega t + 337.5^0) + \ldots\right) \end{aligned} \tag{2.27}$$

Similarly the line-line output voltage across the fourth transformer can be mathematically expressed as,

$$v_{ab_{t4}}(t) = k\sqrt{3}\sum_{n=1}^{\infty} v_{an_n}\sin\left(n\omega t + \frac{n\pi}{12} + \frac{\pi}{24}i\right) \tag{2.28}$$

Expansion of this equation results in,

$$\begin{aligned} v_{ab_{t4}}(t) = &\frac{2kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0) + \frac{1}{5}\sin(5\omega t + 67.5^0) + \frac{1}{7}\sin(7\omega t + 112.5^0)\right. \\ &+ \frac{1}{11}\sin(11\omega t + 157.5^0) + \frac{1}{13}\sin(13\omega t + 202.5^0) \\ &+ \frac{1}{17}\sin(17\omega t + 247.5^0) + \frac{1}{19}\sin(19\omega t + 292.5^0) \\ &\left. +\frac{1}{23}\sin(23\omega t + 337.5^0) + \ldots\right) \end{aligned} \tag{2.29}$$

The second twelve pulse waveform $v_{ab_{12s}}(t)$ is obtained by adding equations 2.27 and

2.29 i.e., $v_{ab_{12s}}(t) = v_{ab_{t3}}(t) + v_{ab_{t4}}(t)$

$$v_{ab_{12s}}(t) = \frac{4kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0) + \frac{1}{11}\sin(11\omega t + 157.5^0) + \frac{1}{13}\sin(13\omega t + 202.5^0) + \frac{1}{23}\sin(23\omega t + 337.5^0) + \ldots\right) \tag{2.30}$$

Which can be expressed in the compact form as

$$v_{ab_{12s}}(t) = k\sum_{n=1}^{\infty} v_{ab_{12n}}\sin\left(n\omega t + \frac{n\pi}{12} + \frac{\pi}{24}i\right) \tag{2.31}$$

$\forall n = 12r \pm 1, r = 0, 1, 2, \ldots$

Mathematical expression for the twenty four pulse voltage waveform can be obtained by adding equations 2.23 and 2.30. i.e.,

$$v_{ab_{24}}(t) = v_{ab_{12f}}(t) + v_{ab_{12s}}(t)$$

It can be seen that the harmonics not contained in the set $24r \pm 1, r = 0, 1, 2$, are in phase opposition and hence they will cancel out resulting in twenty four pulse voltage waveform .

$$v_{ab_{24}}(t) = \frac{8kv_{dc}\sqrt{3}}{\pi}\left(\sin(\omega t + 22.5^0)) + \frac{1}{23}\sin(23\omega t + 337.5^0) + \frac{1}{25}\sin(25\omega t + 22.5^0) + \ldots)\right. \tag{2.32}$$

equation 2.32 can also be written as,

$$v_{ab_{24}}(t) = 4k\sum_{n=1}^{\infty} v_{ab_n}\sin\left(n\omega t + \frac{n\pi}{12} + \frac{\pi}{24}i\right) \tag{2.33}$$

$$\forall n = 24r \pm 1, r = 0, 1, 2, \ldots$$

The formation of twenty four pulse waveform is shown in the figure 2.12 and its harmonic spectrum is shown in the figure 2.13. It has 24r$\pm$ 1 order harmonic components i.e., 23^{rd}, 25^{th}, 47^{th} , 49^{th} and so on, with the magnitude equal to reciprocal, of their order of the fundamental component, of the output voltage waveform.

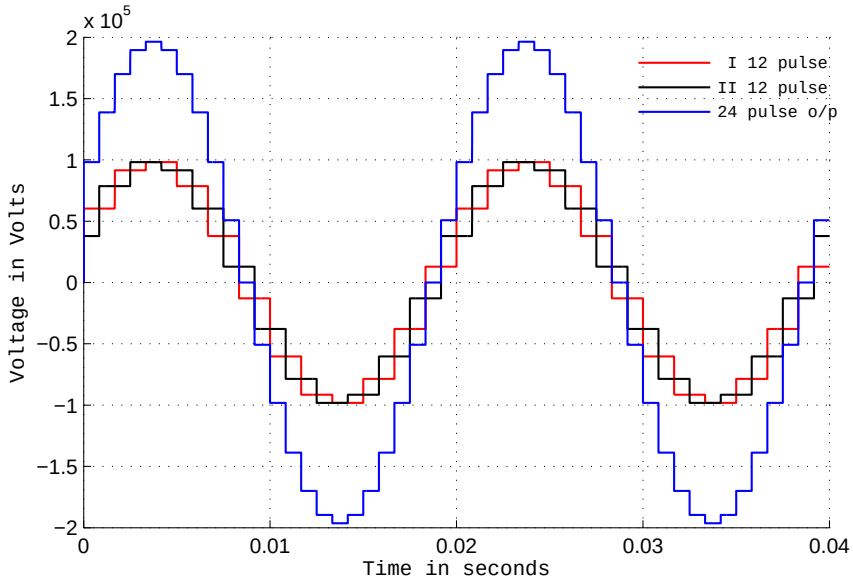


Figure 2.12: Formation of twenty four pulse waveform

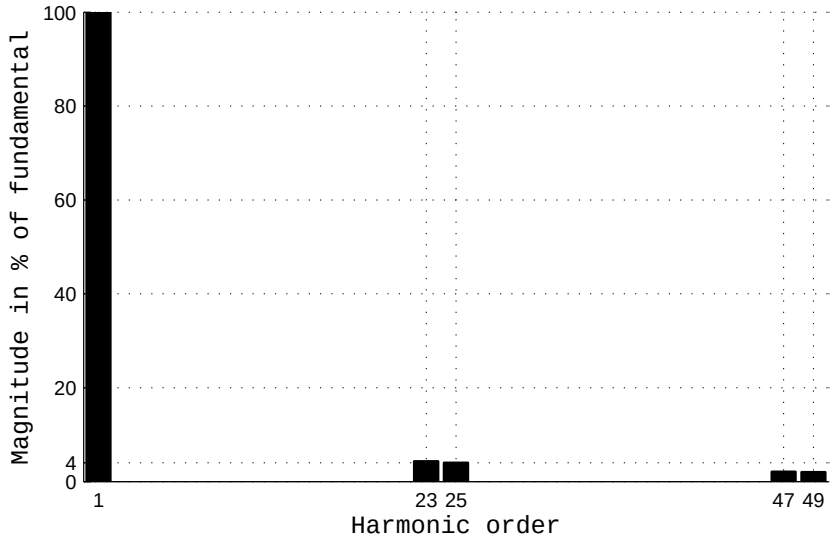


Figure 2.13: Harmonic spectrum of twentyfour pulse waveform

2.4.4.1 Choice of conduction angle (σ)

It is evident from the results presented above that, 23^{rd} and 25^{th} harmonic components are the most dominant harmonics present in the twenty four pulse output voltage waveform. This subsection explains the selection of proper σ, required to minimize the 23^{rd} and 25^{th} harmonic magnitudes. This in-turn results in almost equal THD levels in both twenty four pulse and forty eight pulse inverter output voltages.

The output voltage of VSC exhibits a fundamental component and odd harmonics each of which has amplitude given by (Sen and Stacey, 1998; Albasri *et al.*, 2006),

$$v_{ab_{24}}(t) = \frac{2v_{dc}}{n\pi}\cos\left(\frac{n\pi}{p}\right)\cos(n\gamma) \tag{2.34}$$

Where γ is the dead period during which the ac valve operates in each quarter cycle and the pole output voltage is zero. The variable 'p' represents the number of pulse of the VSC per cycle, $n = p*k\pm 1(k = 1,2,3...)$ represents the odd harmonic components. The amplitude of the odd harmonic component (n) normalized to the fundamental component is:

$$\frac{v_n}{v_1} = \frac{\cos\left(\frac{n\pi}{p}\right)\cos(n\gamma)}{n\cos\left(\frac{\pi}{p}\right)\cos(\gamma)} \tag{2.35}$$

The THD of the voltage is given by equation 2.36 where, v_1 is the fundamental component obtained from equation 2.34 by setting n = 1.

$$THD = \frac{\sqrt{\Sigma v_n^2}}{v_1} \tag{2.36}$$

Figure 2.14 shows the variation of the fundamental and THD for the output voltage (THDv) of VSC normalized with respect to the fundamental component for different dead period (γ). It can be noted that, the THD of a 24-pulse VSC is almost equal to that of a 48 pulse VSC, when γ is 3.75°. Therefore, γ is set at 3.75°, in-order to obtain an output that is comparable to the 48 pulse VSC. It can also be verified from the figure that, the fundamental component, does not decrease significantly at γ=3.75^0. Therefore,

in the present work σ is chosen to be 172.5^0.

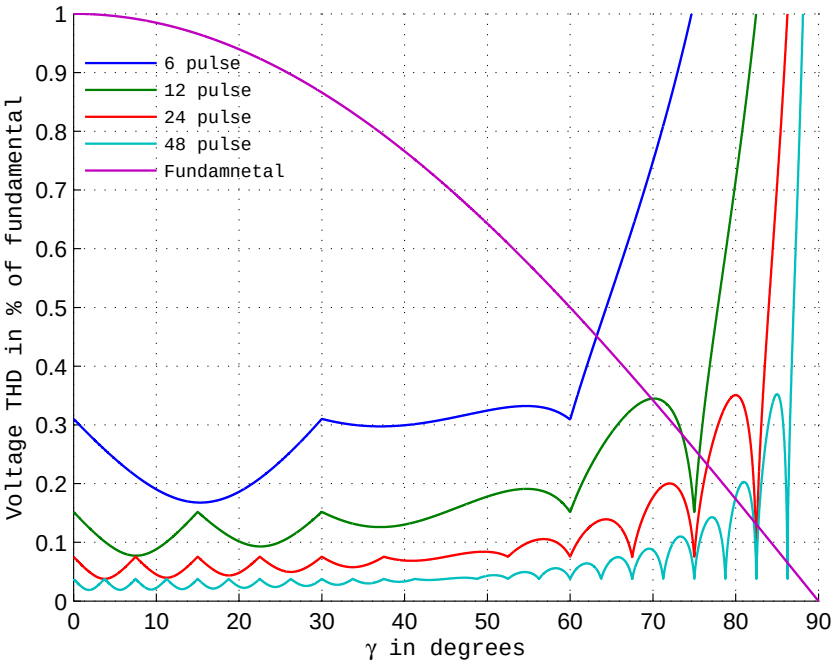


Figure 2.14: The normalized output voltage amplitude and THDv of the VSC

The forty eight pulse output voltage waveform, thus obtained is as shown in figure 2.15. The other two line−line voltage waveforms, will be displaced by -120^0 and -240^0 respectively, from first one.

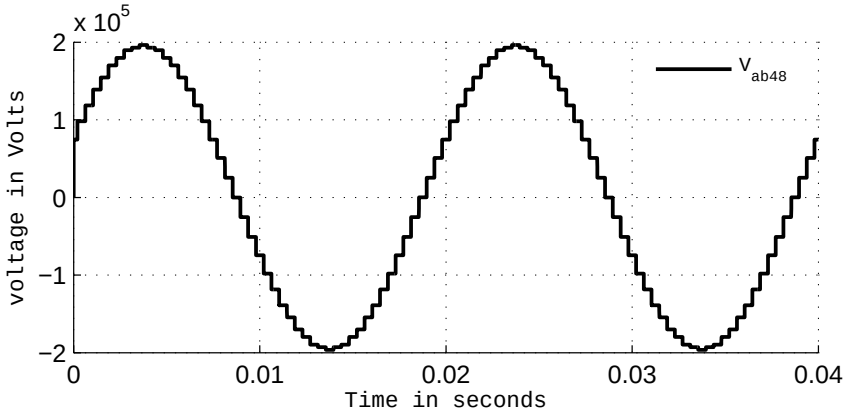


Figure 2.15: 48 pulse output voltage

Figure2.16 shows the harmonic spectrum, of the forty eight pulse voltage wave-

form obtained through EMTDC/PSCAD simulation. It can be seen that, by setting σ = 172.5^0, the magnitude of the 23^{rd} and 25^{th} harmonics can be reduced significantly. The voltage waveform is comprised of 47^{th} and 49^{th}, harmonics as the most dominant harmonics with THD of 3.81%. This THD is in compliance with the IEEE 519 standard. Hence, FACTS devices derived from such an inverter configuration can be interfaced directly with the power system without filtering requirement.

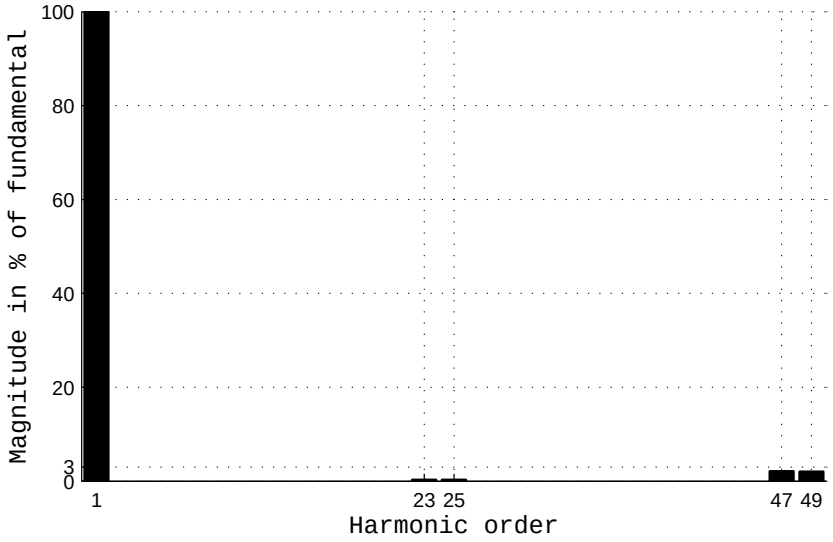


Figure 2.16: Harmonic spectrum of forty eight pulse waveform

The above facts indicate that, multipulse-multilevel inverter configuration provides favorable platform for the development of high performance FACTS devices. In this work a STATCOM model has been developed based on this configuration. Details of STATCOM implementation, its working principle and V-I characteristic is presented in the next section.

2.5 VSC Based STATCOM

The model of the STATCOM based on voltage source converter is shown in the figure 2.17 (Acha *et al.*, 2002). This model consists of a step-down transformer with leakage reactance X_t, a three-phase GTO based VSI and dc side capacitor. The dc capacitor

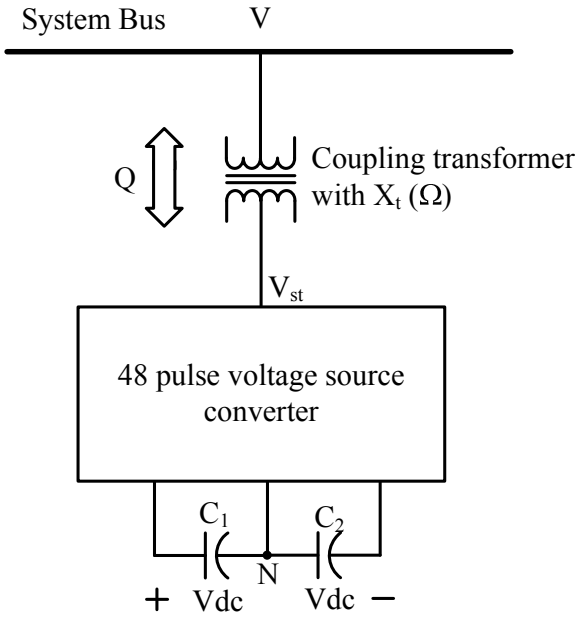


Figure 2.17: General representation of STATCOM interfaced with an ac power system (Acha *et al.*, 2002)

serves as voltage source for the converter. The ac voltage difference across, the coupling transformer leakage reactance, facilitates reactive power exchange between the STATCOM and the power system at the point of common coupling. Essentially, the primary duty of the STATCOM is to regulate the voltage, thereby improving the voltage profile of the interconnected power system.

2.6 Working Principle of STATCOM

The operating principle of the STATCOM can be explained with the help of figure 2.18 (Acha *et al.*, 2002). It is the single phase equivalent circuit of the power system shown in 2.17. In this circuit, the STATCOM is modelled as an ac voltage source V_{st}. A STATCOM has four distinct operating modes. These operating modes can be explained with the help of figure 2.19. This figure shows the steady state vector representation of different operating modes at the fundamental frequency. Each of these modes are discussed briefly in the following paragraphs.

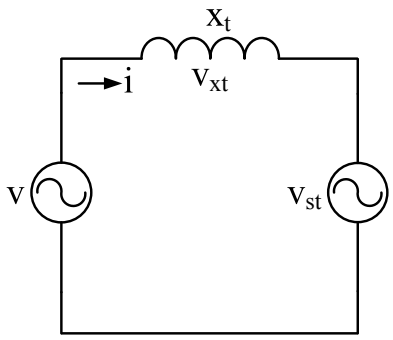


Figure 2.18: Single phase equivalent of a basic VSI based STATCOM interfaced with power system

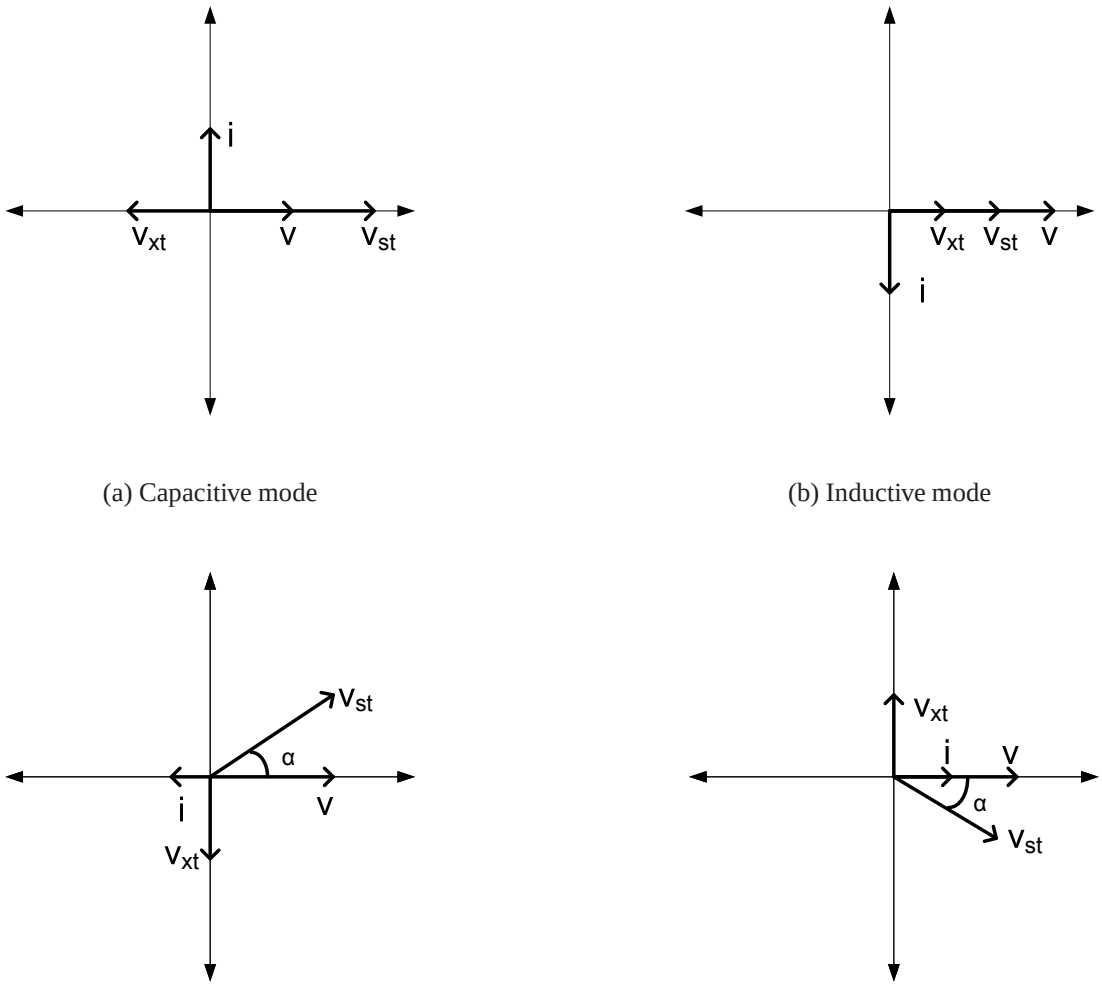
Capacitive mode: This mode prevails, when STATCOM voltage V_{st} is higher than system voltage V. In this mode of operation the STATCOM emulates a capacitor, injecting reactive power to the ac power system. Vectorial representation of this mode is shown in figure 2.19(a).

Inductive mode: This mode starts, when V_{st} is lower than system voltage V. In this mode of operation the STATCOM acts like an inductance, absorbing reactive power from the ac power system. Vectorial representation of this mode is shown in figure 2.19(b).

Active power generation mode: A STATCOM can exchange active power with the ac system provided, a suitable phase angle α exists, between the STATCOM output and the ac power system voltages. This active power exchange can be used to replenish the internal losses of the VSC. It is inevitable as a practical STATCOM suffers from losses in the coupling transformer windings and in the converter switches. These losses consume active power from the ac terminals. Therefore a small phase difference, which is just sufficient to supply the internal losses, always exists between the VSC voltage and the ac system voltage. This mode commences, whenever V_{st} leads V by an angle α. In this mode of operation STATCOM injects active power to the ac power system. Also, capacitor discharges during this mode resulting in drop in capacitor voltage. Figure 2.19(c) shows the vectorial representation of this operating mode.

Active power absorption mode: This mode commences, whenever V leads V_{st} by an angle α. During this mode, STATCOM absorbs active power from the ac power

system. This causes the voltage across the capacitor to rise. Figure 2.19(d) shows the vectorial representation of this operating mode.



(a) Capacitive mode

(b) Inductive mode

(c) Active power generation

(d) Active power absorption

Figure 2.19: Vector representation of STATCOM operation modes

With reference to figure 2.18 and figure 2.19 the active power and reactive power may be expressed by the following equations (Miller, 1982).

$$P = \frac{V_{st} V \sin(\alpha)}{X_t} \tag{2.37}$$

$$Q = \frac{V_{st}\,(V - \cos(\alpha))}{X_t} \tag{2.38}$$

It can be inferred from the above analysis that, the STATCOM can be controlled essentially by a single parameter, α. Further, if the converter is restricted to reactive power exchange, then the ac output voltage is governed by only controlling the magnitude of the dc link voltage. This is possible due to the fact that, the magnitude of the ac output voltage is directly proportional to the dc capacitor voltage. After being acquainted with the operation, it is also important to study the V-I characteristic of the STATCOM, as it decides the behaviour of the compensator under varying system conditions. This will be explained in the following section.

2.7 STATCOM Characteristics

A typical terminal voltage versus output current characteristic of a static compensator is shown in Figure 2.20 (Hingorani and Gyugyi, 1999). Two slopes of regulation settings and three load lines are superimposed on the V-I characteristics. Among the two slopes of regulation settings, first one has some specific slope and the second one has a zero slope shown by the lines SS^1 and ZZ^1 respectively. Load line L1 intersects the compensator V-I characteristic at the nominal (reference) voltage, thus the output current of the compensator is zero. Load line L2 is below load line L1 due to a decrease in the power system voltage (e.g., generator outage). This load line intersects slope regulation settings SS^1 and ZZ^1 at the points $SV_2$and ZV_2 respectively. This calls for capacitive compensation currents I_{c1} and I_{c2} respectively from the STATCOM. Load line L3 is above load line L1, due to an increase in the power system voltage (e.g., load rejection). This load line intersects slope regulation settings SS^1 and ZZ^1 at the points $SV_1$and ZV_1 respectively. This calls for inductive compensation currents I_{L1} and I_{L2}respectively from the STATCOM. The intersection points V_1^1 and V_2^1 on the voltage axis show the terminal voltage variation without any compensation for load lines L2 and L3. Similarly, points V_1 and V_2 shows the terminal voltage variation when a STAT-

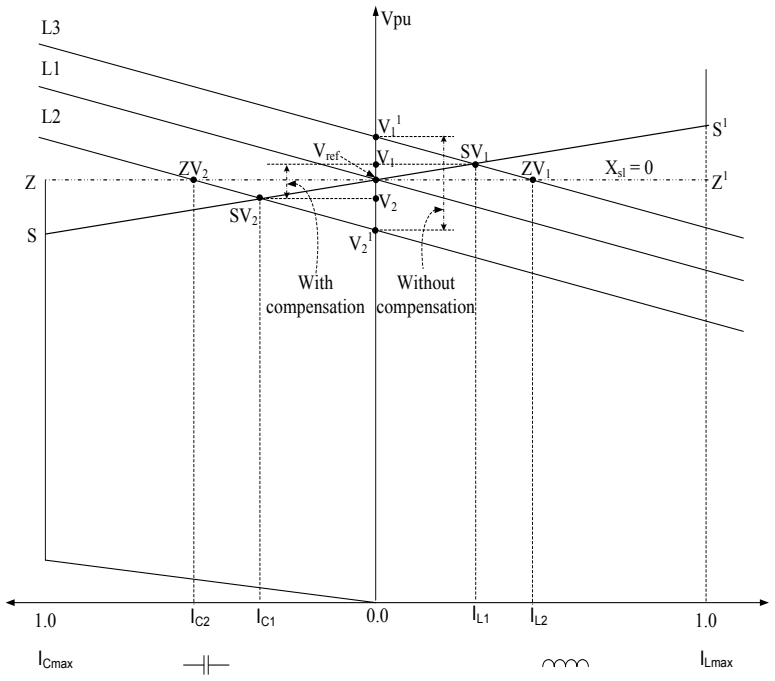


Figure 2.20: STATCOM characteristic

COM with regulation slope SS^1 has been installed. It can be observed that, voltage variation is less in a STATCOM connected system, when compared with system without STATCOM. This indicates that, installation of STATCOM helps to improve voltage regulation at the PCC.

It can also be inferred from the same figure that, the regulation slope plays deterministic role in the the compensator behaviour. A compensator with the zero regulation slope will inject/absorb more reactive current, when compared with compensator having higher regulation slope. This is because compensator with the zero regulation slope is compelled to maintain terminal voltage exactly at the set reference value (perfect terminal voltage regulator). Following paragraph provides more insight into the issue.

2.7.1 The Regulation Slope

In many applications, the static compensator is not used as a perfect terminal voltage regulator, but rather the terminal voltage is allowed to vary in proportion with the compensating current. The reasons for this are enumerated below (Hingorani and Gyugyi,

1999):

- The linear operating range of a compensator with given maximum capacitive and inductive ratings can be extended if a regulation "droop" is allowed. Regulation "droop" means that the terminal voltage is allowed to be smaller than the nominal no load value at full capacitive compensation and, conversely, it is allowed to be higher than the nominal value at full inductive compensation.
- Perfect regulation (zero droop or slope) could result in poorly defined operating point, and a tendency of oscillation, if the system impedance exhibited a "flat" region (low impedance) in the operating frequency range of interest.
- A regulation "droop" or slope tends to enforce automatic load sharing between STATCOM as well as other voltage regulating devices employed to control transmission voltage.

Because of these reasons a regulation droop of 3% has been implemented in this work. All operational aspects of the STATCOM has been evaluated using a suitable model power system. The model power system selected for carrying out the simulation studies is briefed in following section.

2.8 Model System Selected for Study

As mentioned, the research objectives include, study of interaction between STATCOM controller and the power system during both normal and abnormal conditions. To accomplish this task, a model power system has been selected. The single line diagram of the model system is shown in the figure 2.21.

The model power system consist of two 230 KV Thevinin equivalent sources E_s and E_r at the sending and receiving ends respectively. Two sources are connected by, a 200 kilometre length transmission line, with a $\pm$ 100MVA STATCOM inserted at the midpoint. The distance relay is deployed at sending end for the protection of the transmission line. This study system provides greater flexibility, to vary the load level and to change power flow direction, to suit the simulation requirement by varying the source load angle δ. The full system parameters are given in the appendix-A.

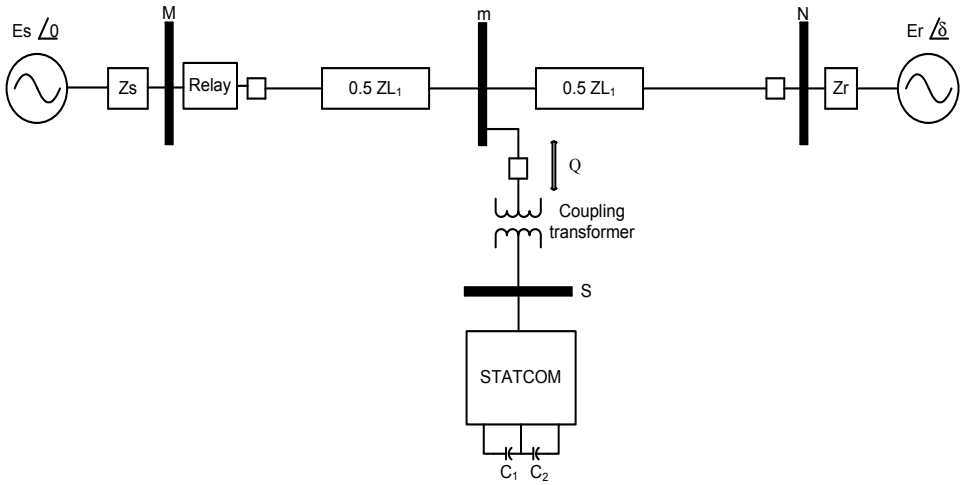


Figure 2.21: Sample model power system selected for study purpose

In order to obtain accurate transient response, the power system components of study system are modelled using the electromagnetic transient software EMTDC/PSCAD. A small time step of 25 micro seconds is used throughout the entire period of simulation to capture the fast switching transients during faults on the system.

The main objective of the midpoint connected STATCOM in the figure 2.21 is to regulate the PCC voltage to a set reference value. This in-turn enhances the power transfer capacity of the line. In-order to meet this objective a well designed closed loop controller is inevitable. Design and development of the STATCOM controller is presented in the next section.

2.9 Development of STATCOM Controller

Figure 2.22 shows the block diagram of the STATCOM controller. This controller is designed based on the decoupled reactive current control technique (El-Moursi and Sharaf, 2005). The operation of the STATCOM controller can be described as follows. The positive sequence voltage at midpoint is calculated using equation 2.39. It is compared with the reference input and the resultant error is passed through the voltage controller. This PI-controller is tuned to produce the required quadrature current reference I_{qref}. The actual quadrature current I_q injected by STATCOM at midpoint is calculated using

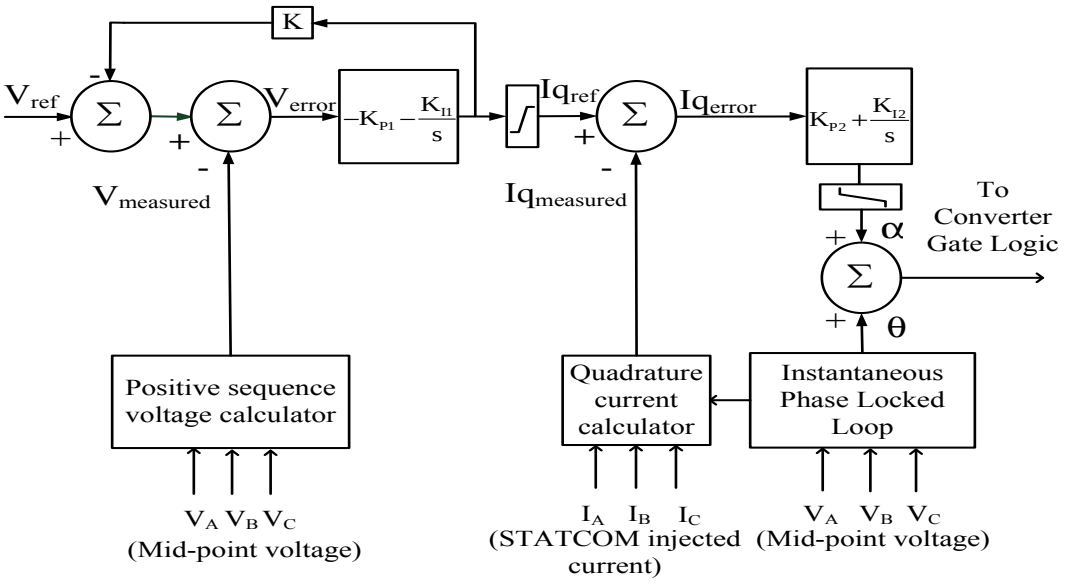


Figure 2.22: Block diagram of a decoupled reactive current controller

equation 2.40, in per unit with the 100MVA and 230kV as base MVA and base voltage respectively. The synchronizing angle θ is obtained from phase locked loop. The calculated quadrature current I_q, is compared with the reference quadrature current I_{qref} and the resultant error is passed through current controller in the inner loop. This PI-controller produces the control angle α necessary to vary the dc capacitor voltage. This in-turn controls the reactive power flow, between STATCOM and ac system, to regulate the PCC voltage. A slope factor 'K' is set to 0.03 to avail the maximum benefit from the STATCOM installation. Normally the STATCOM is designed for transient reactive current rating of about $\pm$ 2.p.u. for time less than one second (Hingorani *et al.*, 2000). Therefore outputs of both voltage and the current controllers are passed through the limiters to limit the over current during power system disturbances. The limiting values of -2p.u.$<I_{qref}>$ 2p.u and -$5^0 < \alpha < 5^0$ for the voltage and current controllers are used to achieve this task. All the faults on model power system are applied for less than one second duration, so that the transient reactive current rating of the STATCOM is not violated.

The efficacy of the controller depends upon the design of PI-controllers. A well designed controller should offer expected results under varying power system conditions. The design parameters of PI-controller is explained in the following section.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \tag{2.39}$$

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{2.40}$$

2.9.1 Design of PI-Controller

A proportional-integral (PI) controller is used as a voltage regulator for voltage control application. The parameters of the PI-controller are selected based on the step response performance of the controller for a step change in the reference voltage. The time response, and the stability of the control, is dependent on the system impedance. For this reason, the control is normally optimized for the weak system. This will result in the long response time of the strong system. With practical STATCOM, the worst case response time is typically is in the range of 30 to 70 ms (2 to 4 cycles at the power system frequency)(Hingorani and Gyugyi, 1999).

A step response of $\pm$10% change in the controller voltage reference V_{ref} is used to tune PI-controller based on the following design criteria,

- overshoot of less than 5%,
- rise time of less than 1.5 cycle
- settling time of 2 to 3 cycles.
- perform reasonably, under both weak and strong system conditions.

All of the above mentioned design criteria are confirmed through simulations. For this purpose model system shown in the figure 2.21 has been used. The system strength can be varied by varying the short circuit capacities of the sources. Model system with 6500MVA and 10000MVA source capacities have been treated as the weak and strong system respectively.

Figures 2.23 and 2.24 shows the performance of the voltage PI-regulator, for $+$10%

and -10% change in the set reference respectively. It can be seen that for both weak and strong systems, the maximum overshoot is less than $\pm 2\%$ and the settling time is around 3.5 cycles. These results are in accordance with the design criteria. The current controller was also tuned in accordance with voltage controller with similar design parameters. The values of gain used in both PI-controllers are given in Appendix-A.

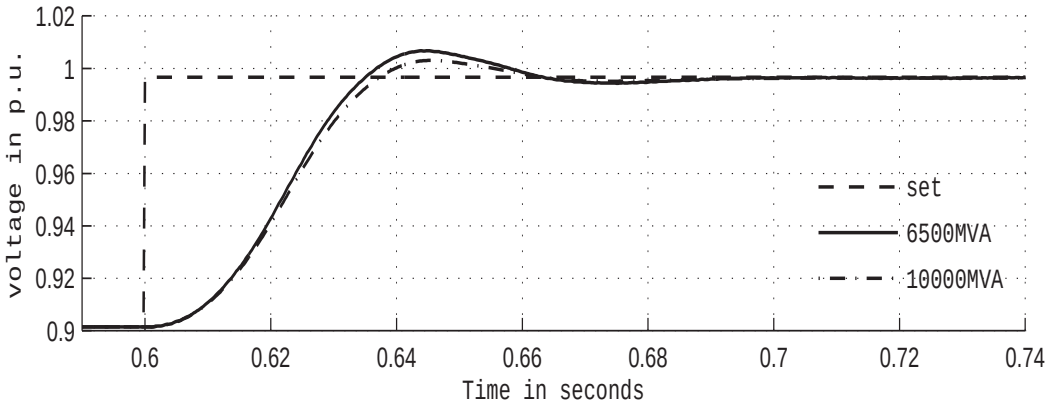


Figure 2.23: Step response of the system for +10% change in the v_{ref}

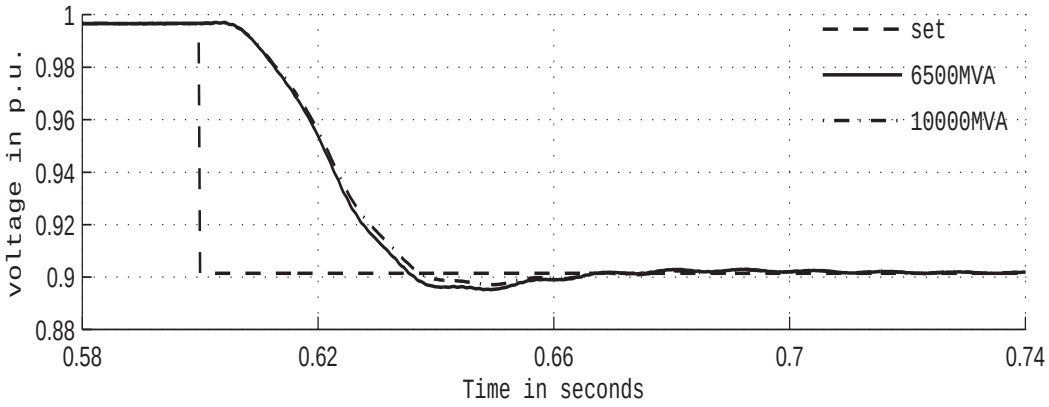


Figure 2.24: Step response of the system for -10% change in the v_{ref}

The performance evaluation of the STATCOM controller under various operating conditions is narrated with the help of simulations, in the following section.

2.9.2 Performance Evaluation of STATCOM Controller

The STATCOM controller can be operated in two modes namely,

- Voltage control mode
- VAR control mode

Operation of this controller in both operating modes has been evaluated using proper load excursion. The details are as follows:

2.9.2.1 Voltage control Mode

In voltage control mode, the main objective of the STATCOM controller is to regulate the PCC voltage to the set value. Hence in this mode the reactive power supplied by STATCOM changes depending on the set reference voltage and system conditions. For performance evaluation the following excursion has been planned with respect to voltage reference signal v_{ref} :

- 1.00 p.u. from 0.1 - 0.3 seconds,
- 1.05 p.u. from 0.3 - 0.5 seconds,
- 0.95 p.u. from 0.5 - 0.8 seconds,
- 1.00 p.u. from 0.8 - 1.0 seconds.

The desired v_{ref} command is shown in the figure 2.25. It can be seen from the same figure that, prior to STATCOM connection at 0.1s, the PCC actual terminal voltage v_t is little less than 1.0 p.u.

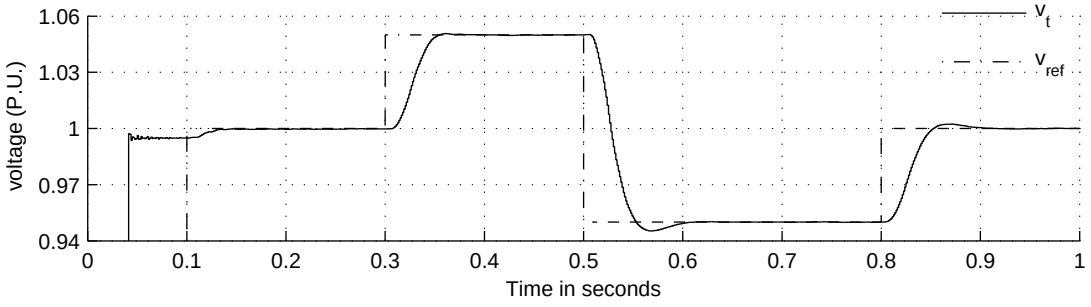


Figure 2.25: Set voltage reference and actual terminal voltage

At t=0.1s the STATCOM is pressed into service. The STATCOM controller swings

into action immediately. By virtue of this, voltage controller generates quadrature current reference signal i_{qref} as shown in figure 2.26.

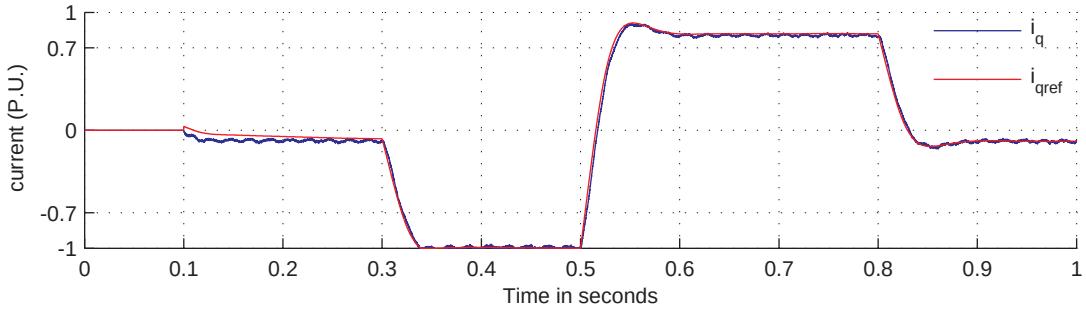


Figure 2.26: Set quadrature current reference and actual quadrature current

This corrective action charges the capacitor voltage to about 1.00 p.u as shown in the figure 2.27. Now the STATCOM is working in the capacitive mode and injects about 10 MVAR capacitive reactive power, to maintain v_t at the set reference value. At t=0.3s capacitor voltage increases further to 1.23 p.u and STATCOM injects its full rated capacity of -100 MVAR, as shown in figure 2.28 in-order to meet higher v_{ref} command. This control action took about 2.5 cycles, which satisfies the controller design criteria.

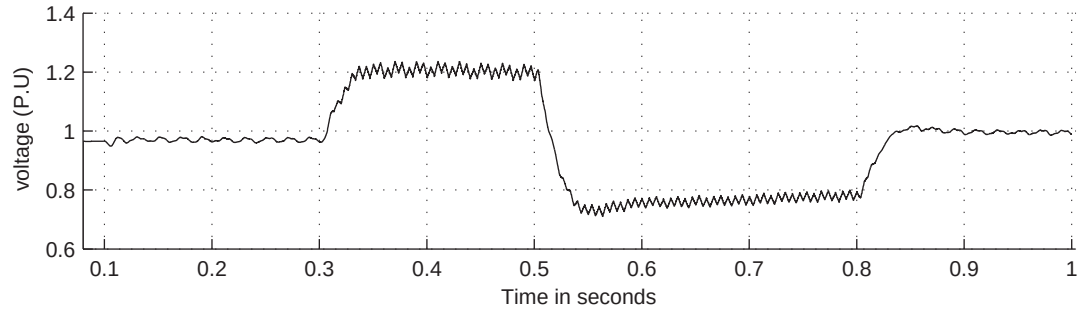


Figure 2.27: Capacitor dc voltage

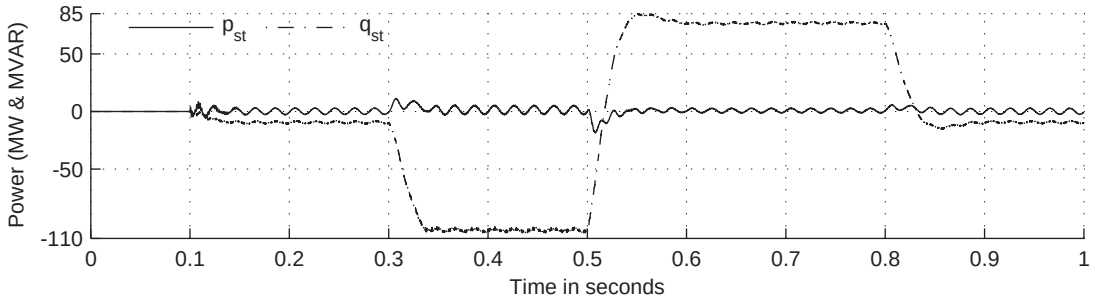


Figure 2.28: STATCOM active and reactive power

The voltage regulation leads to an increase in the transmitted real power to 162 MW from 152 MW. Due to the reactive power compensation, the transmitted reactive power decreases to -30 MVAR from +15 MVAR on the transmission line as shown in the figure 2.29. At t=0.5s, the capacitor voltage drops to 0.78 p.u. (fig. 2.27). During this period, STATCOM is working in the inductive mode. It absorbs 78 MVAR reactive power from the power system (fig. 2.28), to maintain v_t at the set value of 0.95 p.u. This poor voltage regulation, decreases the transmitted active power to 146 MW, while increasing the reactive power to 60 MW on the transmission system as shown in the figure 2.29.

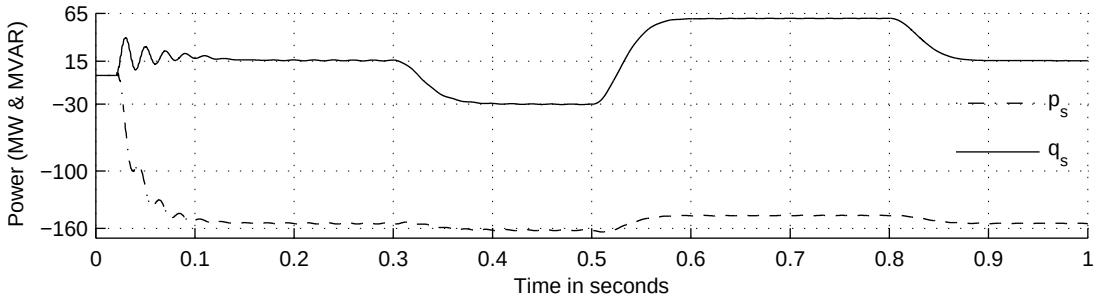


Figure 2.29: Transmission line active and reactive power

The STATCOM voltage and current waveforms are shown in the figure2.30 for the entire period of simulation. The time axis is zoomed from 0.48s to 0.56s for the purpose of close observation as shown in the figure 2.31. It can be seen that, the STATCOM current leads the voltage by 90^0 during capacitive mode (upto 0.5s) and lags the voltage by 90^0 during inductive mode (t >0.5s).

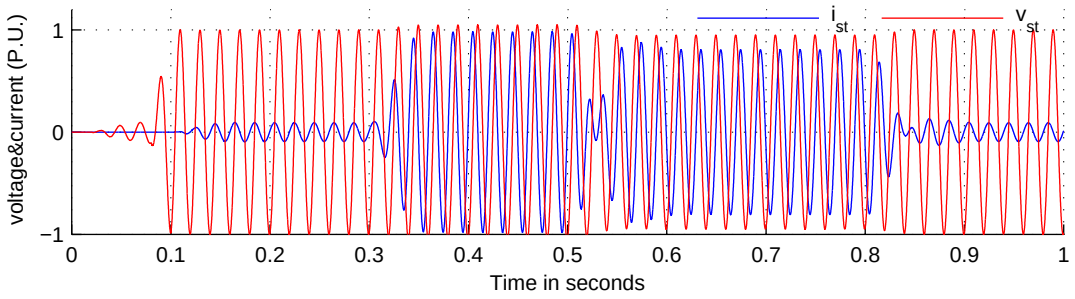


Figure 2.30: STATCOM voltage and current

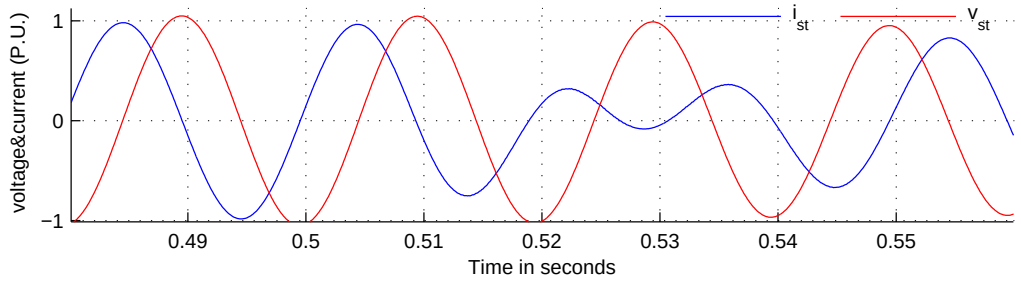


Figure 2.31: Enlarged view of STATCOM voltage and current

At t=0.8 s v_{ref} was brought back to 1.0 p.u. and STATCOM injects about 10 MVAR capacitive reactive power, to maintain v_t at the set reference value. During the entire period of simulation, the load angle δ was kept constant at 20^0, and the slope of the STATCOM was set at 0%.

The simulation has been repeated with a slope of 3%, on the same model system. It can be seen from figure 2.32 that, the terminal voltage is smaller than the reference voltage, in capacitive compensation mode and, higher than the set voltage in inductive compensation mode due to regulation slope characteristics. The quadrature current reference signal i_{qref} and the STATCOM injected/absorbed active and reactive power are presented in figure2.33 and figure2.34 respectively.

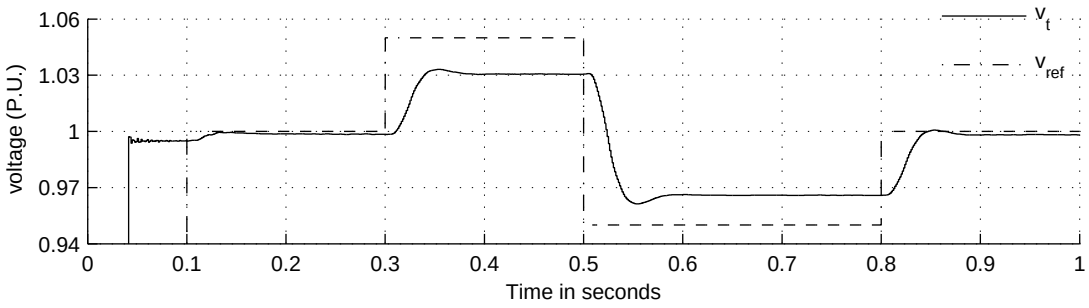


Figure 2.32: Set voltage reference and actual terminal voltage for 3% slope

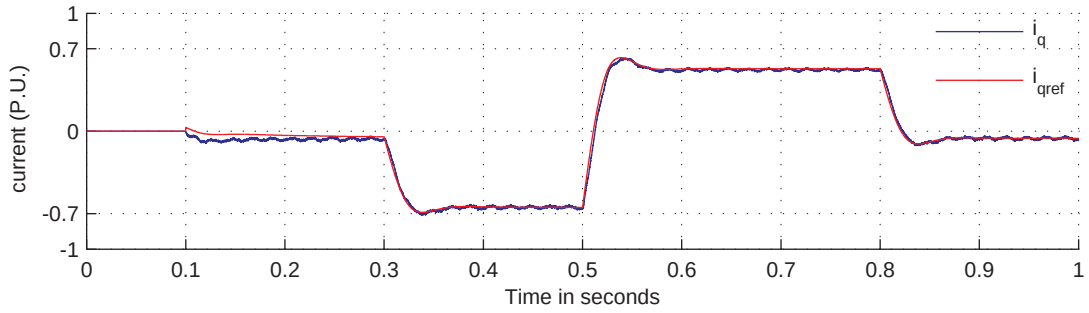


Figure 2.33: capacitor voltage for for 3% slope

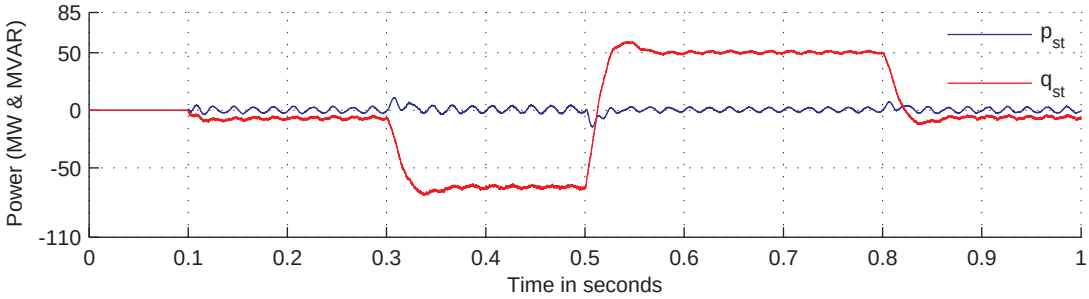


Figure 2.34: STATCOM active and reactive power for 3% slope

2.9.2.2 VAR Control Mode

The objective of the test is to measure the response of the instantaneous reactive current controller. In this mode of operation, the outer voltage control loop of the figure 2.22 is bypassed. A test signal is directly injected into i_{qref}. STATCOM controller will deliver

or absorb the reactive power as per the reference command, irrespective of the PCC voltage. For the purpose of evaluation the following excursion has been planned with respect to quadrature reference signal i_{qref} :

- 0.50 p.u. from 0.1 - 0.3 seconds,
- 1.00 p.u. from 0.3 - 0.5 seconds,
- -1.00 p.u. from 0.5 - 0.7 seconds,
- 1.00 p.u. from 0.7 - 1.0 seconds.

The desired i_{qref} command is shown in the figure 2.35. The STATCOM is switched into operation t=0.1 s, which initiates control action.

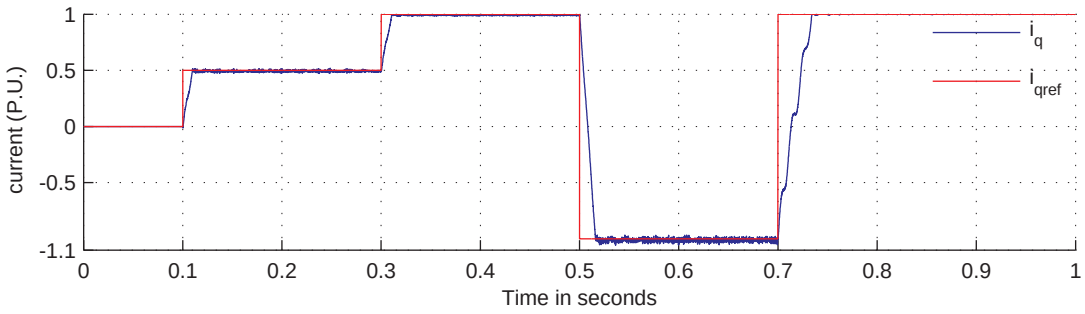


Figure 2.35: Set quadrature current reference and actual quadrature current

At t=0.1s, command to absorb 0.5 p.u. inductive reactive current from the power system has been issued to the controller. This causes drop in capacitor voltage to 0.83 p.u. as shown in the figure 2.36. STATCOM absorbs 50 MVAR reactive power from the power system as shown in the figure2.37. This leads to reduced terminal voltage at 0.96 p.u. as shown in figure 2.38.

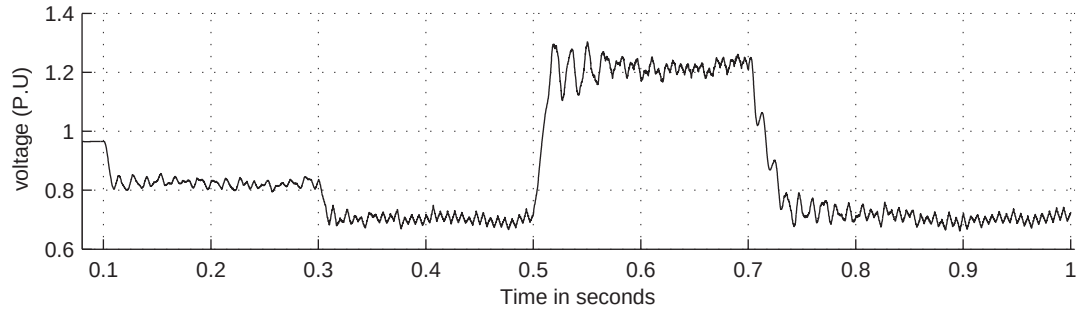


Figure 2.36: Capacitor dc voltage

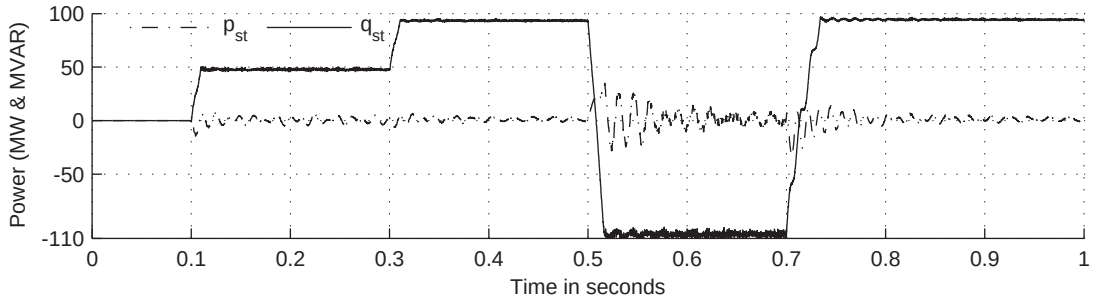


Figure 2.37: STATCOM active and reactive power

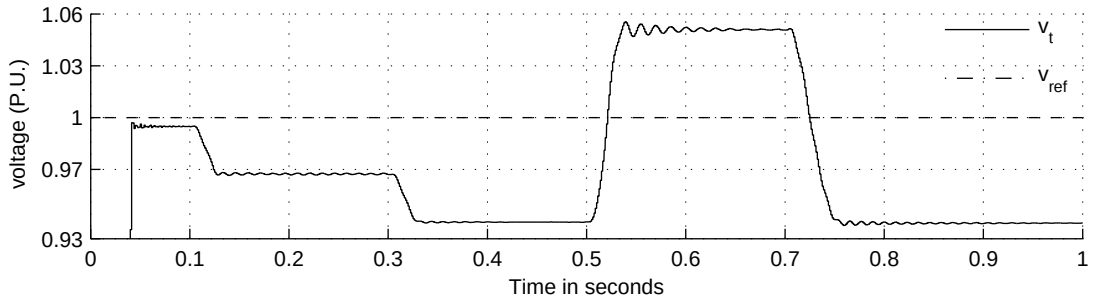


Figure 2.38: Set voltage reference and actual terminal voltage

At t=0.3s, STATCOM is set to operate at its full inductive rated capacity. Hence, capacitor voltage, drops further to 0.7 p.u. and the terminal voltage drops to 0.94 p.u.

This poor voltage regulation results in reduced active power transmission at 144 MW. Lack of reactive compensation increases the reactive power on the transmission line to 69 MVAR as shown in the figure 2.39.

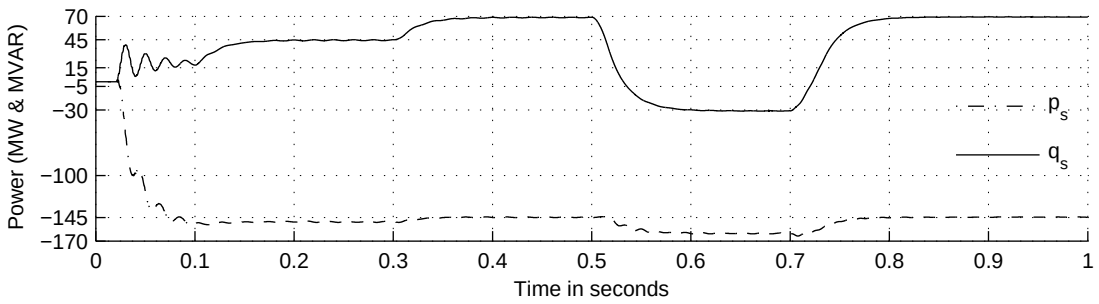


Figure 2.39: Transmission line active and reactive power

At t=0.5s reactive controller was set to operate in capacitive mode at its full rated capacity. This increases the capacitor voltage to about 1.23 p.u. resulting in an increased PCC terminal voltage. Due to excessive supply of reactive power compensation, transmission line reactive power drops to about -30 MVAR and the active power increases to 161 MW. At t=0.7s, controller was set to operate at its full inductive capacity and the controller performs as desired.

In this chapter the performance of the mid point connected STATCOM controller has been evaluated. Various system conditions are simulated by considering a typical model power system. It is shown that, the controller tuning essentially ensures good dynamic performance of STATCOM. Elaborate simulation studies proved that STATCOM interaction with transmission system meets the purpose for which it is deployed. In the chapter that follows implications of STATCOM presence on distance relay are assessed.

CHAPTER 3

Simulation Studies to Evaluate the Influence of STATCOM on Distance Relay Performance

3.1 Introduction

The protective equipments of high quality and reliable performance are required to protect the expensive power system components from damage. They accomplish this task by the prompt removal of faulty section of the power system from service, while continuing operation in the rest of the system. In addition to this, the protective relaying also provides information about the fault type and its location. Such information is highly useful in expediting the restoration process. Now a days, various protective schemes are available to cater for diverse power system protection requirements. A suitable protective scheme has to be deployed depending on the specific protection requirement.

A physical device on which the functionality of relaying scheme has been realized is known as a protective relay. The power system has witnessed many generation of protection relays, which have their own pros and cons. The present generation of relays are known as the numerical relays. The numerical relays offer following features and functionalities:

- Multi-function like protection, control and monitoring.
- Multiple characteristics.
- Communication capability integrated into these devices facilitates remote control, monitoring and data transfer.
- Adaptable characteristics, which dynamically change the protection characteristic to match the prevailing system conditions by monitoring the specific relaying signals.

These distinct features of numerical relays have drawn the attention of the utilities dealing with power system protection. As a result, the use of electro-mechanical

and solid state relays, has greatly reduced, and many existing installations have been replaced with new numerical relays (Duncan and Bailey, 2003).

The scope of research work is limited to distance relays which are widely used for transmission line protection. This type of relay measures the impedance between the relay installation point and the fault location. The measured impedance is compared against the set impedance to detect the fault. The relay issues trip signal whenever the measured impedance is less than the set impedance. The accuracy, speed and reliability of the trip decision issued by numerical relay depend on the signal processing algorithm, assuming acquired data is accurate. A widely used, Full Cycle Window Fourier (FCWF) algorithm is used to estimate the fundamental components of voltage and current signals in this work.

In the previous chapter, transient behavioural model of a forty eight pulse STATCOM has been developed and successfully interfaced with the power system. It was shown with the help of simulation results that, STATCOM installation is beneficial in PCC voltage regulation. But the excerpts from the literature review reveal that, installation of STATCOM causes adverse impact on the performance of the distance relay.

In this chapter, a numerical distance relay model has been developed to assess the STATCOM's influence. The mathematical equations describing the distance relay reach error due to the presence of STATCOM are derived. The relay model has been subjected to several fault transient conditions using a model power system. The results of performance evaluation confirm the literature review outcome. In the sections that follow, the development and testing of a numerical distance relay model for transmission line protection in EMTDC/PSCAD is explained.

3.2 Modelling of the Numerical Distance Relay

Figure 3.1 shows the block diagram of a numerical distance relay model implemented in EMTDC / PSCAD. As mentioned earlier, distance relay measures the impedance

between the relay installation point and the fault location. Relay requires fundamental component of voltage and current signals at its relay location to calculate the apparent fault impedance. The fast Fourier transform (FFT), block available in the EMTDC / PSCAD with an inbuilt anti-alias filter is used to extract the fundamental phasors of the relaying signals (voltage and current). The relaying signals are sampled at a rate of 32 samples per cycle of a fundamental 50Hz signal. The zero sequence component of the current signals is extracted using sequence component extractor block.

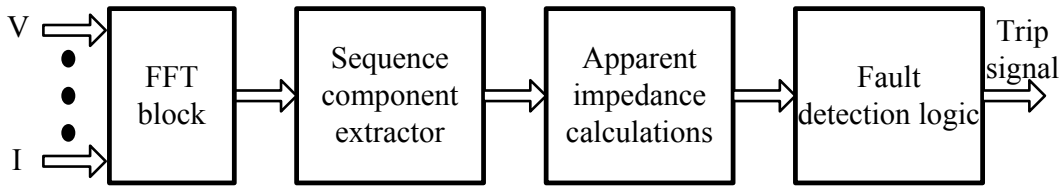


Figure 3.1: Block Diagram of the Numerical Distance Relay

The apparent impedance calculation block uses the extracted signals to compute the fundamental positive sequence fault impedance, at d% of line (dZ_1) for all fault types. This is necessary, as the reach of the relay has been set in terms of positive sequence impedance of the line (Z_1). The dZ_1 of a symmetrical three phase fault can be found by dividing the voltage phasor (V) by the current phasor (I). But, this method does not yield correct value of dZ_1 in case of asymmetrical faults. Therefore some modifications as discussed in following paragraphs are necessary in such faults, which will lead to an accurate fault impedance measurement. In order to measure the correct fault impedance in terms of Z_1, ground distance relays use the respective phase voltage V_x and compensated current $(I_x + 3KI_0)$ signals.

Where,

x is any one phase of three-phase system with ABC phase sequence

K= $\frac{Z_0 - Z_1}{3Z_1}$ is known as the compensation factor, Z_0 and Z_1 are the zero sequence and positive sequence impedances of the line.

Most of the times 'k' is treated as a scalar quantity. But for the accurate measurement of Phase-ground impedance both magnitude and direction of the k is desired (Sanaye-Pasand and Seyedi, 2003). Table 3.1 illustrates the effect of ignoring the angle part

of 'k'. In this table measured values of both resistance and reactance with/without considering phase angle of K are tabulated. It can be seen that, measured values differ significantly from the actual values when the angle part is ignored. Therefore in the present study, both magnitude and phase angle of the 'k' factor are considered.

Table 3.1: Effect of ignoring the k factor angle on measured R& X

Sl No	Fault distance in (KM)	Actual R+jX(Ω)	R + jX with $\|K\|$ only (Ω)	R+jX with k $\angle$ (Ω)
1	90	3.21+j45.69	8.261+j44	3.21+j45.85
2	120	4.28+j60.9	10.78+j58	4.26+j61.08
3	150	5.36+j76.6	13.26+j74	5.34+j76.82

In case of phase faults, delta voltages (V_{xy}) and delta currents (I_{xy}) are used to measure phase fault impedance Z_{xy} which is equal to dZ_1. The value of Z_{xy} is calculated by using the following equation,

$$Z_{(xy)} = \frac{V_{xy}}{I_{xy}}$$

Where,

$V_{xy} = V_x - V_y$,

x and y are any two phases of three-phase system with ABC phase sequence,

$I_{xy} = I_x - I_y$

The formula used by the apparent impedance calculation block for different types of faults is listed in the table 3.2 (K.P.Vittal, 1999).

Table 3.2: Formula used for impedance calculation

Fault type	Formula
ABC	$\frac{V}{I}$
AG	$\frac{V_A}{I_A+3KI_0}$
BG	$\frac{V_B}{I_B+3KI_0}$
CG	$\frac{V_C}{I_C+3KI_0}$
AB	$\frac{V_A-V_B}{I_A-I_B}$
B C	$\frac{V_B-V_C}{I_B-I_C}$
CA	$\frac{V_C-V_A}{I_C-I_A}$

Once the system impedance has been calculated, it is processed by a fault detector block, which decides the occurrence and nature of the fault. A Mho relay characteristic has been implemented to detect the fault. The protection relay of this type will issue the trip signal, whenever the measured impedance falls within the relay boundary. The performance of the distance relay model has been evaluated by subjecting to various fault conditions. This is detailed in the following section.

3.3 Performance Evaluation of Numerical Distance Relay Model

High speed protective relays are required to detect faulty condition of power system by processing transient voltage and current signals. Computer simulation provides a means to create the signals seen by the relay under such conditions. A transient simulation test signal obtained through Electro-Magnetic Transient Program (EMTP) model is very accurate. It closely represents the actual power system transient behaviour including decaying dc and high frequency components. These signals can be used as test signals to evaluate the performance of the relay model. This also helps to arrive at proper relay setting and determination of relay response time (Jodice, 1997).

In this work, the distance relay model built in EMTDC/PSCAD, has been evaluated using the model system shown in the figure 3.2. This is the same model power system described in the previous chapter. But here, the STATCOM is not connected to the power system and the distance relay has been deployed at the sending end.

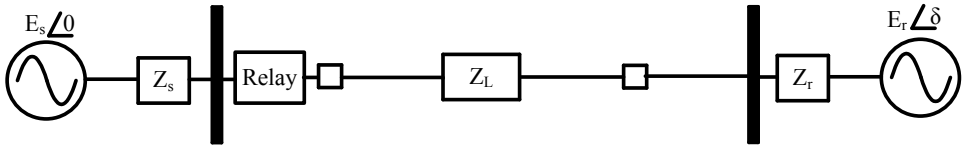


Figure 3.2: Simplified power system model

The dynamic behavior of the distance relay model has been evaluated over its entire protection zone (80%) of the line length, for both phase to phase and phase to ground units. For this purpose, faults are applied at every 10% length of the protected transmission line. At every fault instant, voltage and current signals comprising of two cycles of prefault samples, followed by three cycles of post fault signals have been captured and stored in the respective files. A sample voltage and current signals obtained at relay location for an A-G fault applied at 160 kilometer (KM) of the transmission line is shown in the figures 3.3 and 3.4 respectively.

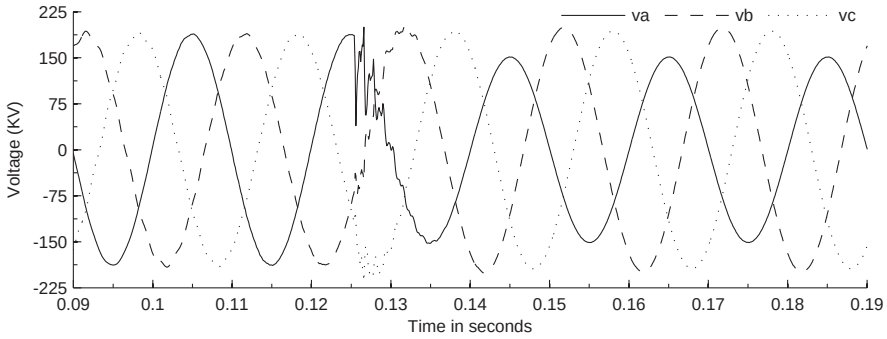


Figure 3.3: Voltage signals seen by the relay, A-G fault(160KM)

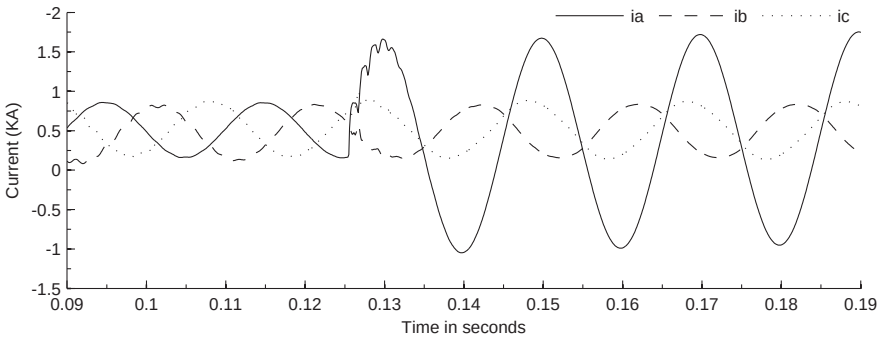


Figure 3.4: Current signals seen by the relay, A-G fault(160KM)

The fault data files created as mentioned above are used for testing the relay performance. Steady state resistance (R) and reactance (X) corresponding to all test cases have been noted. The evaluation results show that, actual values of R and X closely matched with measured values, which validate the relay model.

Another method in-order to depict the operation of the distance relay is to plot the impedance trajectory seen by the relay on R-X diagram. The relay characteristic is also superimposed on the R-X plot to visualize dynamic behaviour of the distance relay. Figure 3.5 shows the impedance trajectory seen by the relay for A-G fault at 160KM. The relay operating zone and the impedance trajectory computed by the relay can be clearly seen, and the fault location can also be estimated from the R-X plot.

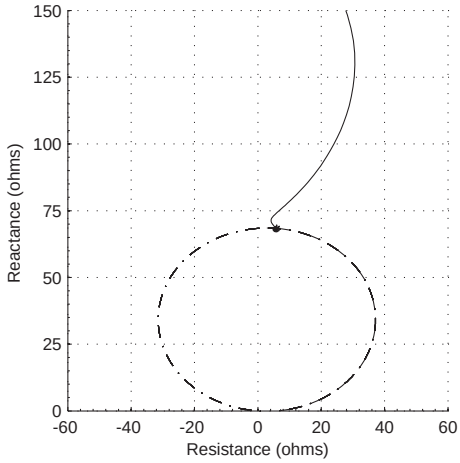


Figure 3.5: Impedance trajectory for A-G fault (160KM)

Table 3.3 show the operating time of the relay for few specific fault cases. These test cases are selected at the zone end of relay setting. This is because the distance relays show higher tendency to maloperate at these locations.

Table 3.3: Mho relay dynamic performance

Case	Nature of fault	Fault at voltage zero/peak	Fault distance(KM)	Time of operation(ms)
I	AB	peak	180	NOP
II	-do-	zero	180	NOP
III	AG	peak	160	19.68
IV	-do-	zero	160	19.94
V	BC-G	peak	140	18.00
VI	-do-	zero	140	18.70

In all the cases studied, relay took about 20 ms to issue the trip signal. This is because of the fact that, the FCWF algorithm is used to estimate the fundamental component of voltage and current signals. The measured impedance, transits from the prefault state to the fault state, with transition period equal to a full cycle of the FCWF data window. Before fault inception, FCWF window is filled with prefault data samples. After one cycle of fundamental 50Hz signal, the data window contains the first full cycle of fault data, and the impedance seen by the relay is close to the actual transmission line fault impedance (K.P.Vittal, 1999).

The performance of the PSCAD/EMTDC relay model, for the wide range of tests conducted has been satisfactory. Hence, same has been deployed for analysing protection system of a STATCOM connected transmission line.

The main objective of this chapter is to investigate STATCOM's influence on the distance relay performance under both steady state and dynamic conditions. The following section presents the analytical approach to derive mathematical equations which describe the apparent impedance error due to STATCOM under steady state conditions.

3.4 Analytical Approach to Study the STATCOM's Influence on the Distance Relay Performance

The distance relays provide protection for the transmission lines by measuring the apparent fault impedance. Any error in measurement of apparent impedance seen by relay, affects the reach accuracy of the relay. The review of literature revealed that, the installation of STATCOM affects the measured impedance seen by the relay. To confirm this fact, equations for the steady state measured impedance error has been derived, using model power system. The motive is to find the measured impedance error in the STATCOM connected transmission line. In-order to accomplish this task, two major cases have been considered they are,

- Case I : Faults transpiring within 50 % of the line length(i.e. before STATCOM connection).
- Case II: Faults transpiring beyond 50% of the line length (i.e. after STATCOM connection).

3.4.1 Case I

Figure 3.6 shows single phase equivalent circuit of the model power system for case I.

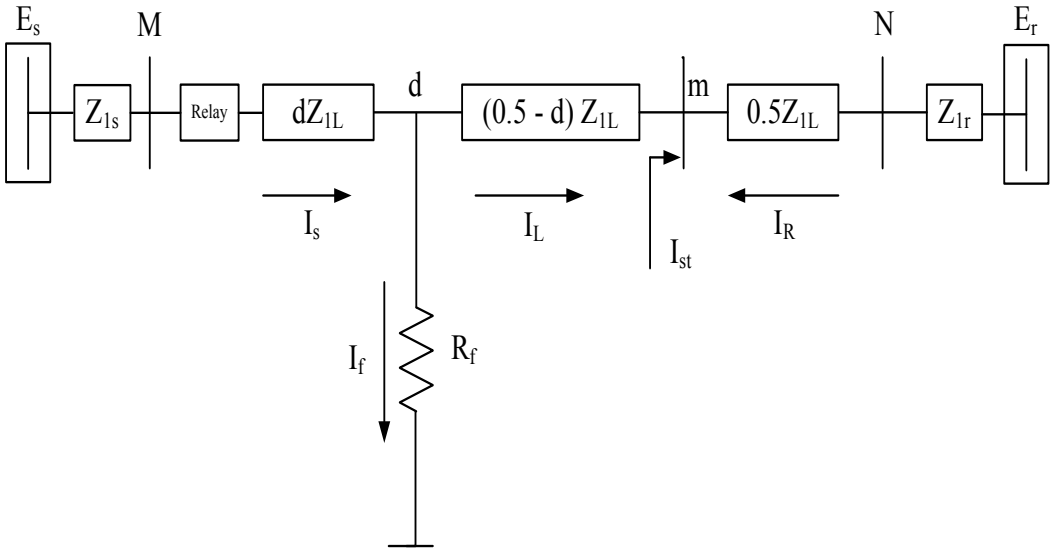


Figure 3.6: Simplified faulted network for the study system for case I

Where,

d is the percentage length of the line at which fault occurs

Z_{1L} is the Positive sequence impedance of the line

R_f is the fault resistance

I_{st} is STATCOM current

X_{st} is the reactance of the coupling transformer

From the figure 3.6 impedance measured by the relay at M can be written as,

$$Z_{relay} = dZ_{1L} + R_f \left(\frac{I_f}{I_s} \right) \tag{3.1}$$

From the equation 3.1 it can be seen that, the measured impedance is more than the actual impedance dZ_{1L}. It is affected by both fault resistance R_f and the STATCOM current I_{st}. But for solid faults the measured impedance will not be affected by the presence of STATCOM.

3.4.2 Case II

Figure 3.7 shows the single phase equivalent circuit for the second case.

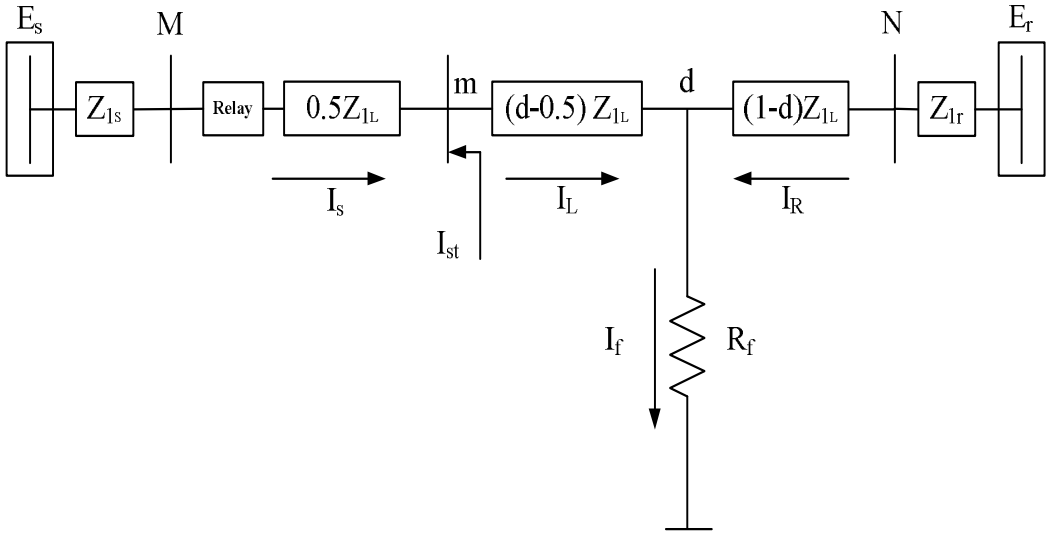


Figure 3.7: Simplified faulted network for the study system for case II

With the help of this circuit, the apparent impedance seen by the relay for different types of faults have been derived. Also, the expression for error in the measured impedance is presented in this section.

3.4.2.1 Single line to ground faults

The sequence voltages at the relay location (V_{Rx}) for single line to ground fault with respect to figure 3.7 can be written as;

$$V_{Rx} = 0.5Z_{Lx}I_{sx} + (d-0.5)\,Z_{Lx}I_{Lx} + I_{fx}R_f \tag{3.2}$$

where x = 1, 2, or 0; a suffix denotes the positive, negative and zero sequence components respectively,
and $I_{Lx} = I_{sx} + I_{stx}$, substituting this in equation 3.2 we have:

$$V_{Rx} = 0.5Z_{Lx}I_{sx} + (d-0.5)\,Z_{Lx}(I_{sx} + I_{stx}) + I_{fx}R_f \tag{3.3}$$

From equation 3.3, all the sequence voltages at the relay location can be expressed as follows:

$$\begin{aligned} V_{R1} &= 0.5Z_{L1}I_{s1} + (d-0.5)\,Z_{L1}(I_{s1} + I_{st1}) + I_{f1}R_f \\ V_{R2} &= 0.5Z_{L2}I_{s2} + (d-0.5)\,Z_{L2}(I_{s2} + I_{st2}) + I_{f2}R_f \\ V_{R0} &= 0.5Z_{L0}I_{s0} + (d-0.5)\,Z_{L0}(I_{s0} + I_{st0}) + I_{f0}R_f \end{aligned} \tag{3.4}$$

Phase voltage at relay location can be calculated by adding all sequence voltages i.e.,

$$V_R = V_{R1} + V_{R2} + V_{R0} \tag{3.5}$$

Substituting equation 3.4 into equation 3.5 yields,

$$V_R = dZ_{L1}I_{s1} + dZ_{L2}I_{s2} + dZ_{L0}I_{s0} + (d-0.5)\left(Z_{L1}I_{st1} + Z_{L2}I_{st2} + Z_{L0}I_{st0}\right) + I_f R_f \quad (3.6)$$

after simplification, equation 3.6 can be written as,

$$V_R = dZ_{L1}\left(I_s + k_0 I_{s0}\right) + (d-0.5)Z_{L1}(I_{st1} + k_0 I_{st0}) + I_f R_f \quad (3.7)$$

Where, $k_0 = \frac{Z_{L0}-Z_{L1}}{Z_{L1}}$ is the zero sequence compensation factor.

For single phase to ground fault, the apparent impedance of distance relay can be calculated using the following equation,

$$Z_{Relay} = \frac{V_R}{I_{Relay}} \quad (3.8)$$

Where, I_{Relay} is equal to $I_s + k_0 I_{s0}$, substituting this into equation 3.8 we get,

$$Z_{Relay} = \frac{V_R}{I_s + k_0 I_{s0}} \quad (3.9)$$

substituting equation 3.7 into equation 3.9, yields 3.10

$$Z_{Relay} = dZ_{L1} + (d-0.5)Z_{L1}\left(\frac{I_{st} + k_0 I_{st0}}{I_{Relay}}\right) + R_f\left(\frac{I_f}{I_{Relay}}\right) \quad (3.10)$$

In practice, one side of the shunt transformer is connected in delta, so there is no zero sequence current injected by STATCOM, hence , I_{st0}=0, thus the equation 3.10 can be rewritten as,

$$Z_{Relay} = dZ_{L1} + (d-0.5)Z_{L1}\left(\frac{I_{st}}{I_{Relay}}\right) + R_f\left(\frac{I_f}{I_{Relay}}\right) \quad (3.11)$$

The apparent impedance for solid fault can be written as,

$$Z_{Relay} = dZ_{L1} + (d-0.5)Z_{L1}\left(\frac{I_{st}}{I_{Relay}}\right) \tag{3.12}$$

3.4.2.2 Three Phase Faults

Three phase faults are considered as balanced faults. Under such conditions, system can be represented only by positive sequence circuit. The voltage at the relay location can be written as (Albasri *et al.*, 2006),

$$V_R = 0.5Z_{L1}I_s + (d-0.5)\,Z_{L1}(I_s + I_{st}) + I_f R_f \tag{3.13}$$

The apparent impedance seen by the relay for three phase bolted fault can be derived by using equation 3.8, after rearranging it can be written as,

$$Z_{Relay} = dZ_{L1} + (d-0.5)Z_{L1}\left(\frac{I_{st}}{I_{Relay}}\right) \tag{3.14}$$

3.4.2.3 Phase to phase faults

The apparent impedance for a phase-to-phase faults can be found from the delta voltage and delta current signals. Now by considering a BC fault on the transmission line the apparent impedance seen by the relay can be found by equation 3.15 (Khederzadeh and Ghorbani, 2011)

$$Z_{Relay} = \frac{V_B - V_C}{I_B - I_C} = \frac{V_{Relay}}{I_{Relay}} \tag{3.15}$$

By symmetrical component method we have the following equations

$$V_A = V_{a1} + V_{a2} + V_{a0} \tag{3.16a}$$

$$V_B = \alpha^2 V_{a1} + \alpha V_{a2} + V_{a0} \tag{3.16b}$$

$$V_C = \alpha V_{a1} + \alpha^2 V_{a2} + V_{a0} \tag{3.16c}$$

Where, α is symmetrical component operator which is equal to $1\angle 120^0$
from which we can write;

$$\begin{aligned} V_B - V_C &= \alpha^2(V_{a1} - V_{a2}) + \alpha(V_{a2} - V_{a1}) \\ &= \alpha^2(V_{a1} - V_{a2}) - \alpha(V_{a1} - V_{a2}) \\ &= (V_{a1} - V_{a2})(\alpha^2 - \alpha) \end{aligned} \tag{3.17}$$

similarly we can write,

$$I_B - I_C = (I_{a1} - I_{a2})(\alpha^2 - \alpha) \tag{3.18}$$

Therefore, from equations 3.17 and 3.18, Z_{Relay} can be written as,

$$Z_{Relay} = \frac{V_{a1} - V_{a2}}{I_{a1} - I_{a2}} \tag{3.19}$$

By using equations 3.4 in equation 3.19 and after performing few mathematical operations apparent impedance for solid phase-phase faults can be written as,

From the figure 3.7, the sequence voltages at the relay point can be expressed as follows:

$$V_{a1} = I_{a1}0.5Z_{L1} + (I_{a1} + I_{st1})(dZ_{L1} - 0.5Z_{L1}) + R_f I_{f1} \tag{3.20}$$

$$V_{a2} = I_{a2}0.5Z_{L1} + (I_{a2} + I_{st2})(dZ_{L1} - 0.5Z_{L1}) + R_f I_{f2} \tag{3.21}$$

Therefore,

$$V_{a1} - V_{a2} = dZ_{L1}(I_{a1} - I_{a2}) + (d - 0.5)Z_{L1}(I_{st1} - I_{st2}) + R_f(I_{f1} - I_{f2}) \tag{3.22}$$

By dividing equation 3.22 by $I_{a1} - I_{a2}$ we get,

$$\frac{V_{a1} - V_{a2}}{I_{a1} - I_{a2}} = dZ_{L1} + (d - 0.5)Z_{L1}\frac{(I_{st1} - I_{st2})}{(I_{a1} - I_{a2})} + \frac{R_f(I_{f1} - I_{f2})}{(I_{a1} - I_{a2})} \tag{3.23}$$

For solid faults third term in the equation 3.23 can be eliminated and it can be written

as

$$\frac{V_{a1}-V_{a2}}{I_{a1}-I_{a2}} = dZ_{L1} + (d-0.5)Z_{L1}\frac{(I_{st1}-I_{st2})}{(I_{a1}-I_{a2})} \tag{3.24}$$

Multiplying and dividing the second term in the equation 3.24 by $(\alpha^2-\alpha)$ we get,

$$\frac{V_{a1}-V_{a2}}{I_{a1}-I_{a2}} = dZ_{L1} + (d-0.5)Z_{L1}\frac{(I_{st1}-I_{st2})}{(I_{a1}-I_{a2})}\frac{(\alpha^2-\alpha)}{(\alpha^2-\alpha)} \tag{3.25}$$

By using equations 3.18 and 3.25 we get,

$$Z_{Relay} = dZ_{L1} + (d-0.5)Z_{L1}\left(\frac{I_{st}}{I_{Relay}}\right) \tag{3.26}$$

where, $I_{st} = I_{st(B)} - I_{st(C)}$

From equations 3.12, 3.14 and 3.26 it can be seen that, for all types of faults, apparent fault impedance computed by the relay differs from the actual fault impedance i.e., dZ_{L1}. The apparent impedance error due the installation of STATCOM can be expressed as:

$$Z_{error} = (d-0.5)Z_{L1}\left(\frac{I_{st}}{I_{Relay}}\right) \tag{3.27}$$

The equation 3.27 shows that, measured apparent impedance error is directly proportional to the fault distance from the relay location and the ratio of STATCOM current to the relay current $\left(\frac{I_{st}}{I_{Relay}}\right)$. The magnitude and sign of this ratio determines the type and extent of reach error. The sign of the current ratio will be positive or negative as result of current injection or absorption by the STATCOM. A positive value of this ratio leads to under-reach of the relay, as a result of higher impedance seen by the relay. On the other hand, the negative value of the current ratio would result in over-reach of the relay, as a result of lesser impedance seen by the relay.

The following section presents the dynamic simulation carried out to study the distance relay performance in the presence of STATCOM.

3.5 Simulation Studies on Performance of Distance Relay Under Dynamic Operating Conditions of STATCOM

In the previous section influence of STATCOM on distance protection during steady sate conditions has been presented. In-order to gain more insight into the problem, dynamic behaviour of the STATCOM required to be considered. Therefore the study has been extended further, to explore the impact of STATCOM on distance relay performance, under dynamic operating conditions. Also, many other factors which influence relay performance such as, STATCOM rating, load level, types of faults and the fault locations have been considered in the analysis. The EMTDC/PSCAD model power system described in the section 2.8 of previous chapter has been used for the simulation purpose.

3.5.1 Rating of STATCOM

Figure 3.8 shows the rating of STATCOM required to maintain PCC voltage exactly at 1.0 p.u. for the different power transmission levels. Two STATCOM models with rated power capacities of $\pm$ 100 MVA and $\pm$200 MVA are considered for simulation in this study. Integration of STATCOM with such ratings will enhance power transmission up to 300 MW and 420 MW respectively, while maintaining the PCC at 1.0 p.u. These STATCOM models can be used to transfer higher power as shown in table3.4, provided PCC voltage level is relaxed by $\pm$0.05 p.u. The corresponding load angles are also tabulated in the same table.

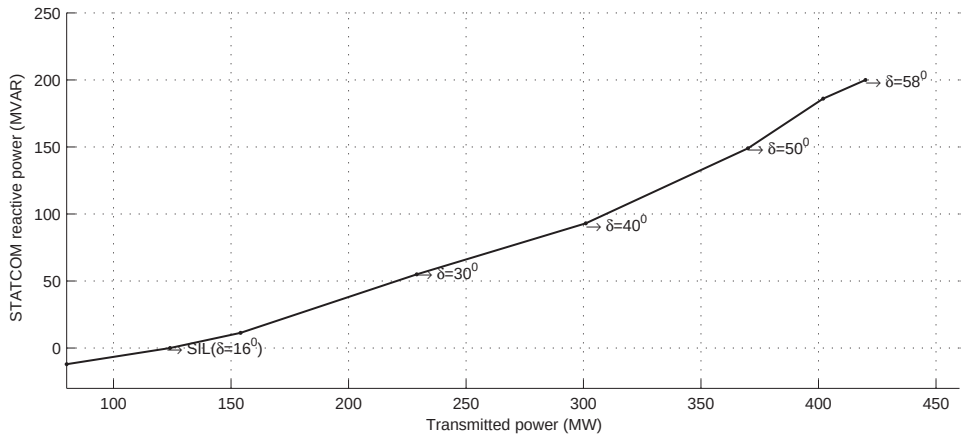


Figure 3.8: STATCOM rating versus power levels.

Table 3.4: power levels achieved with different STATCOM rating

STATCOM rating (MVAR)	Load angle (degrees)	Transmittable power (MW)
$\pm$ 100	0 to 55	upto 383
$\pm$ 200	0 to 67	upto 454

3.5.2 Simulation Results

The test cases encompassing all possible fault conditions are planned to evaluate the distance relay performance. Table 3.5 shows the parameters list with respective ranges, considered in the study with 100 MVA and 200 MVA STATCOM models respectively. For each case the apparent impedance seen by the relay, located at the sending end with and without STATCOM have been noted.

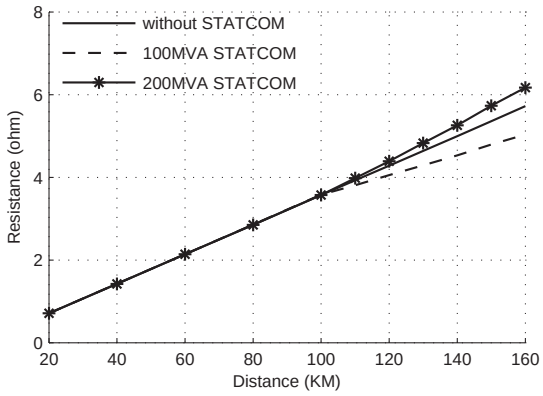
Table 3.5: Test cases planned for relay performance evaluation

STATCOM rating (MVA)	Fault location (KM)	Type of fault	Load angle (degree)
100	10 to 160 in steps of 10	AG, BC, AB-G and ABC	15, 35 and 55
200	10 to 160 in steps of 10	AG, BC, AB-G and ABC	15, 35, and 55

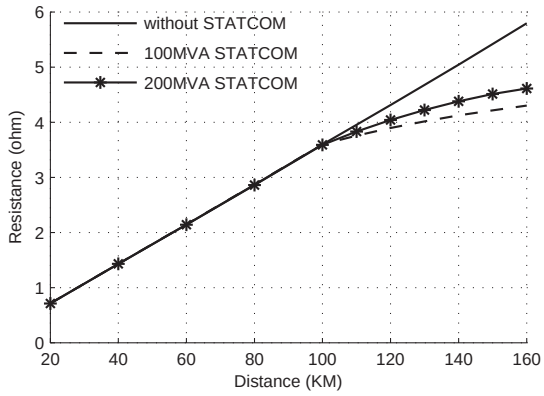
Figures from 3.9 to 3.16 show the simulation results for the cases mentioned in the table 3.5. These results are obtained, when the STATCOM was configured to maintain the PCC voltage at 1.0 p.u. in voltage control mode. The impedance seen by the relay is presented in the rectangular coordinate format. The measured resistance and the reactance are plotted separately for all the cases with and without STATCOM.

3.5.2.1 Single line to ground faults

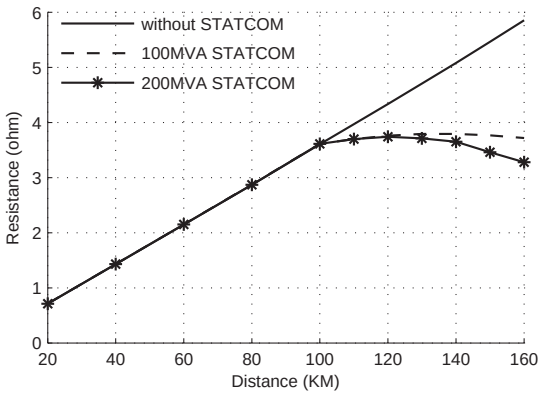
Figures 3.9(a), (b) and (c) show the apparent resistance seen by the relay for different load conditions during single line to ground faults. It can be seen that for a STATCOM connected system apparent resistance seen by the relay, decreases with the increase in the load angle.



(a) $\delta = 15^0$



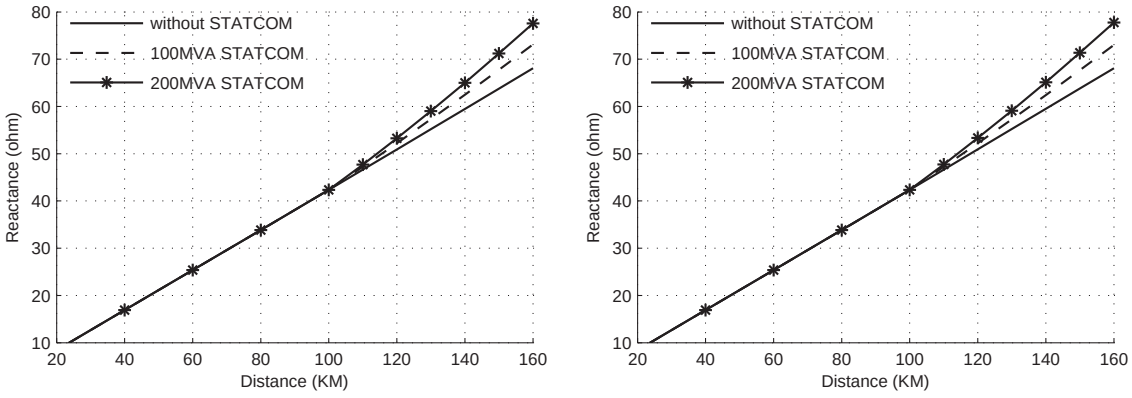
(b) $\delta = 35^0$



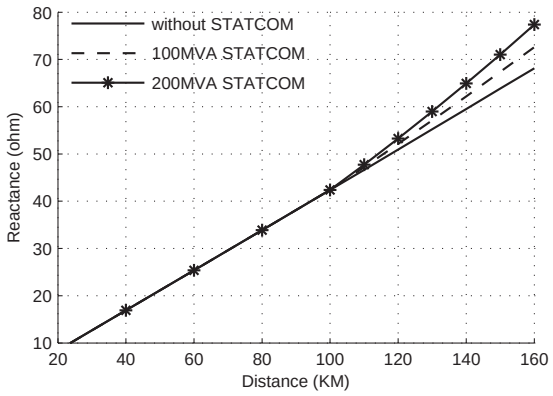
(c) $\delta = 55^0$

Figure 3.9: Resistance seen by the relay at different load angles (δ) for AG fault

The apparent reactance seen by the relay for single line to ground faults is shown in the figures 3.10(a), (b) and (c). The apparent reactance differ in value for the line with STATCOM and without STATCOM, particularly for the faults after midpoint. The apparent reactance increases as the fault location moves farther from the relay location. From the same figures it may also be observed that, increase in the STATCOM rating results in an increase in the measured reactance. The line loading level has no influence on the measured reactance.



(a) $\delta = 15^0$ (b) $\delta = 35^0$

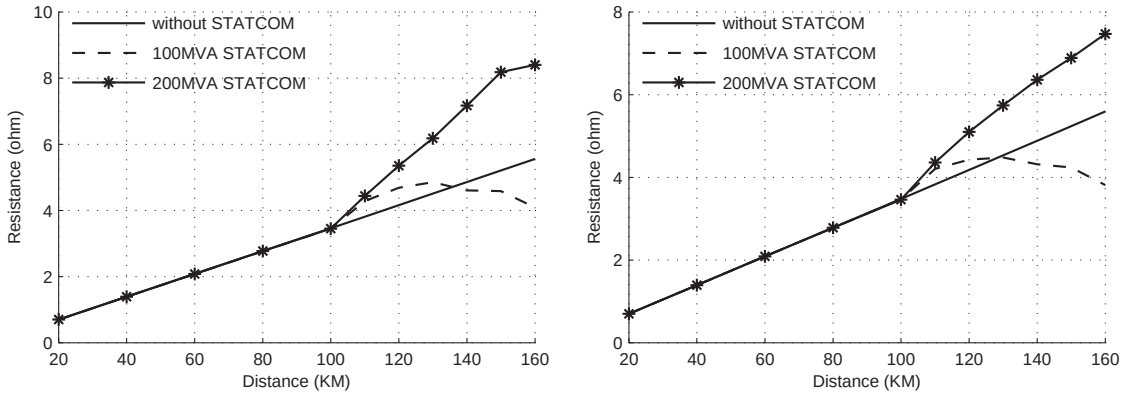


(c) $\delta = 55^0$

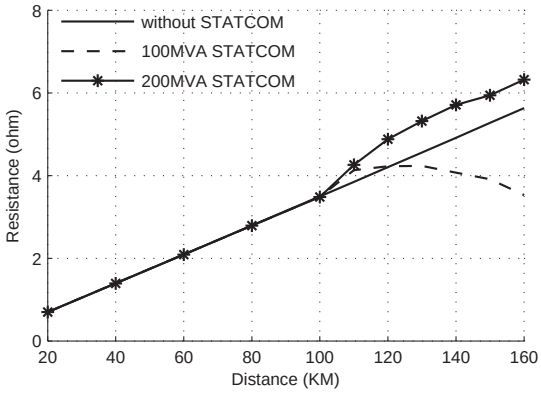
Figure 3.10: Reactance seen by the relay at different load angles (δ) for AG fault

3.5.2.2 Double line to ground faults

For double line to ground faults the apparent resistance seen by the relay is shown in the figures 3.11(a), (b) and (c). Apparent resistance decreases with the increase in the load angle, as in the case of single line to ground faults for STATCOM connected lines.



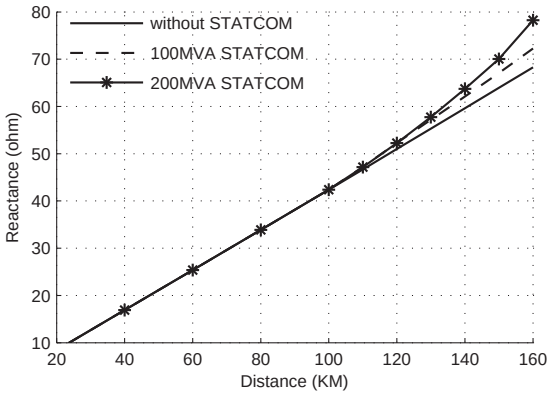
(a) $\delta = 15^0$ (b) $\delta = 35^0$



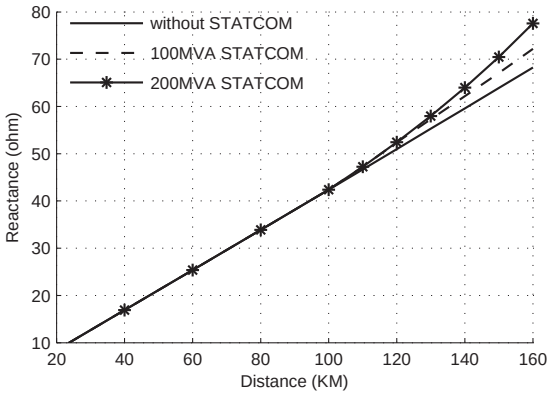
(c) $\delta = 55^0$

Figure 3.11: Resistance seen by the relay at different load angles (δ) for ABG fault

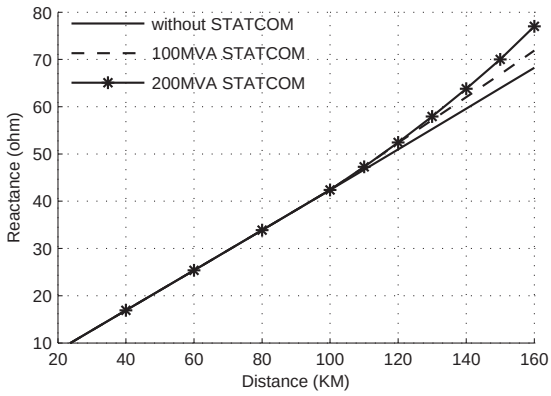
The apparent reactance show similar variation as in the case of single line to ground faults. Figures 3.12(a), (b) and (c) show the apparent reactance seen by the relay for double line to ground faults under various load conditions.



(a) $\delta = 15^0$



(b) $\delta = 35^0$

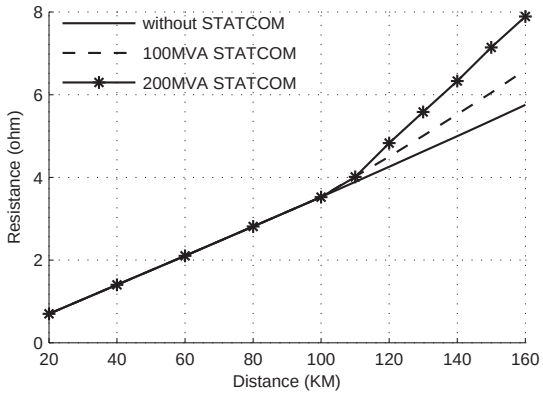


(c) $\delta = 55^0$

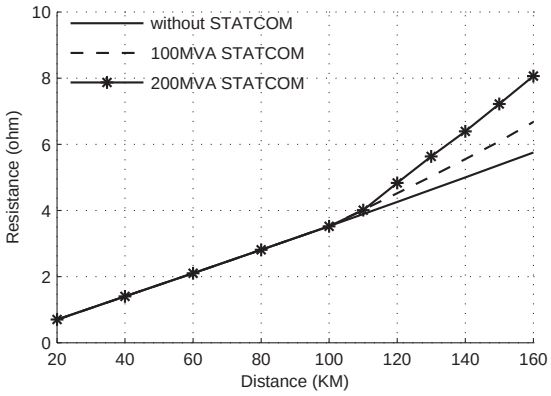
Figure 3.12: Reactance seen by the relay at different load angles (δ) for ABG fault

3.5.2.3 Three phase faults

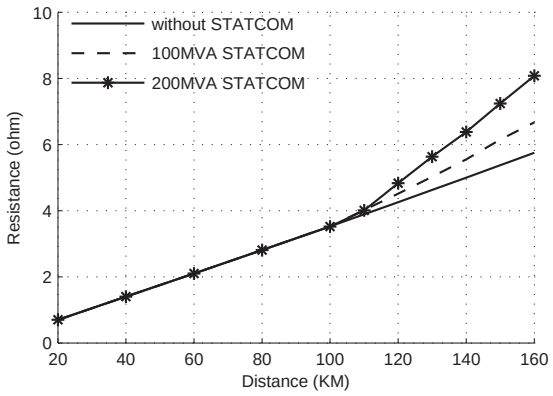
The apparent resistance seen by the relay for three phase fault is shown in the figures 3.13(a), (b) and (c). It can be seen that, the apparent resistance increases as the rating of the STATCOM increases.



(a) $\delta = 15^0$



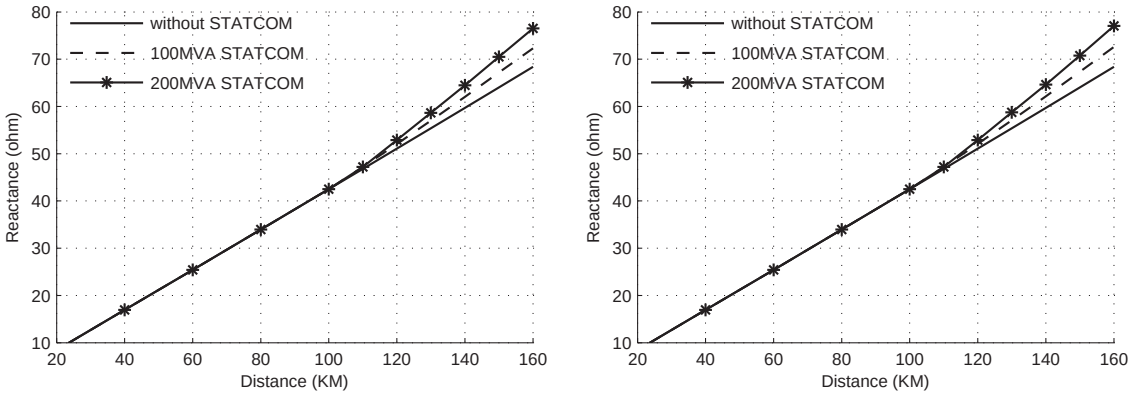
(b) $\delta = 35^0$



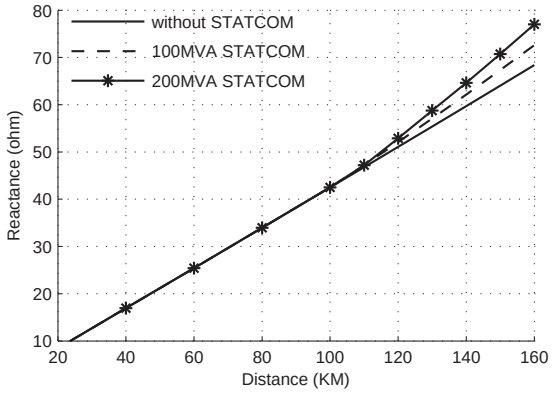
(c) $\delta = 55^0$

Figure 3.13: Resistance seen by the relay at different load angles (δ) for ABC fault

The apparent reactance seen by the relay for three phase faults also show similar behaviour as in the case of of resistance. It is shown in the figures 3.14(a), (b) and (c). The change in load angle had no influence on measured resistance and reactance.



(a) $\delta = 15^0$ (b) $\delta = 35^0$

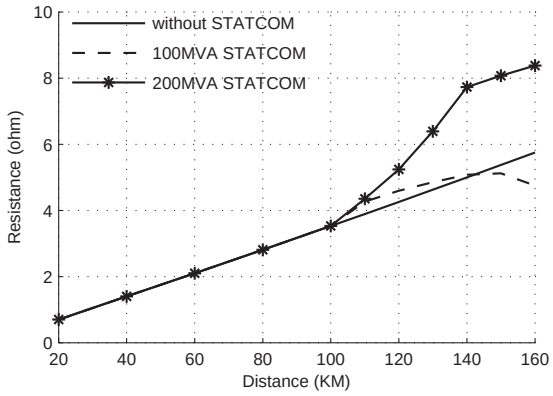


(c) $\delta = 55^0$

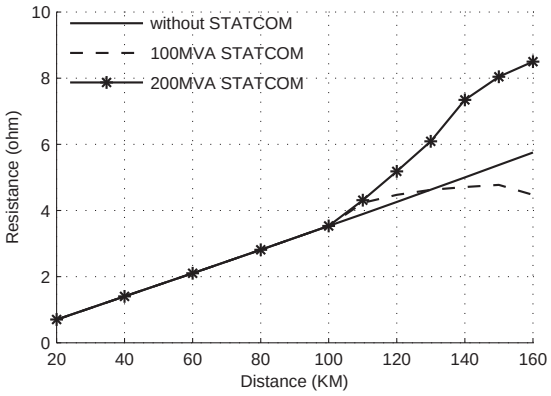
Figure 3.14: Reactance seen by the relay at different load angles (δ) for ABC fault

3.5.2.4 Phase-phase faults

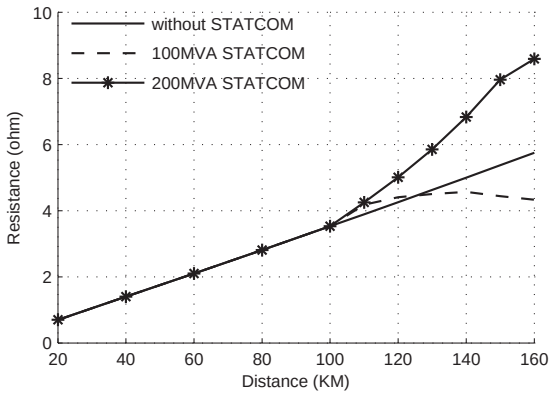
The apparent resistance seen by the relay for line to line fault is shown in the figures 3.15(a), (b) and (c). Change in the load angle has no impact on the apparent resistance, but it increases with the increase in STATCOM rating.



(a) $\delta = 15^0$



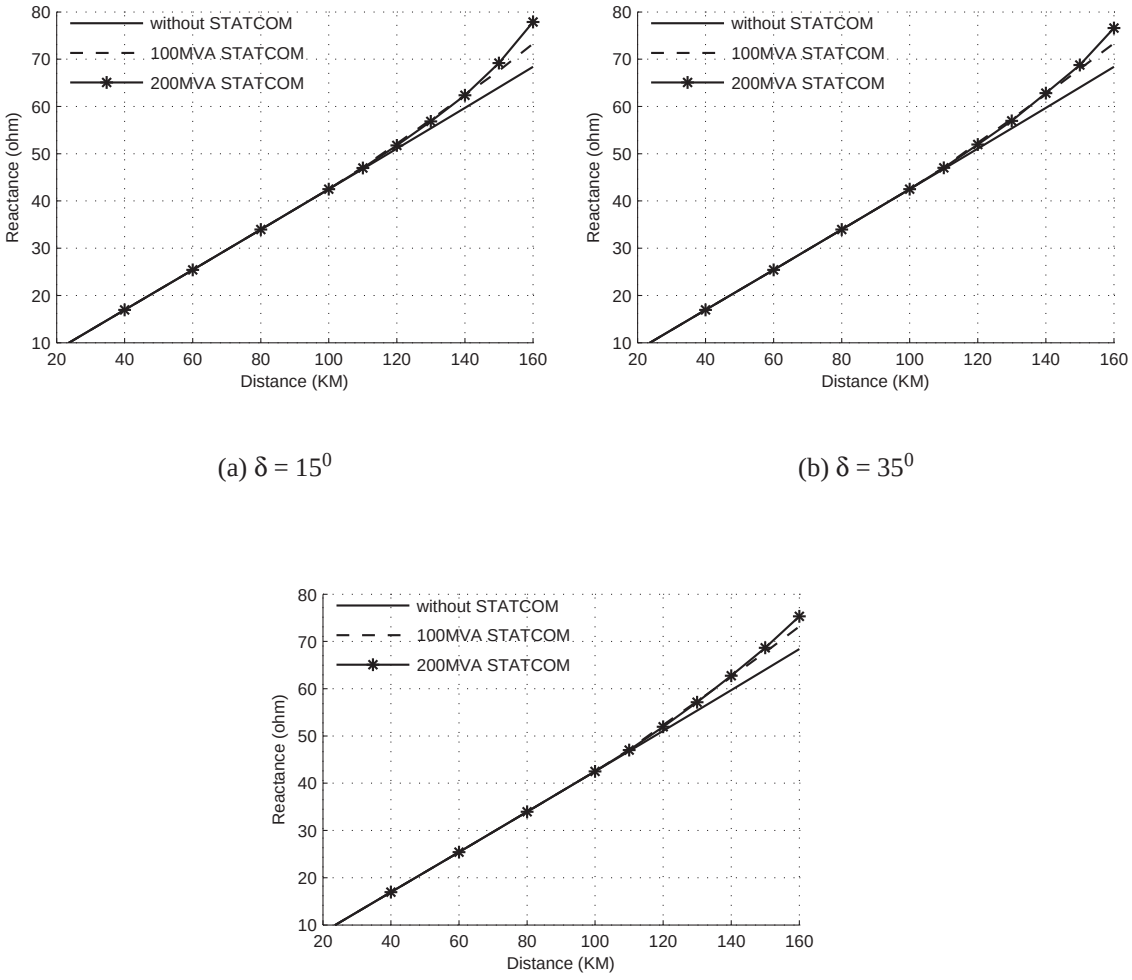
(b) $\delta = 35^0$



(c) $\delta = 55^0$

Figure 3.15: Resistance seen by the relay at different load angles (δ) for BC fault

The apparent reactance seen by the relay for phase-phase faults is shown in the figures 3.16(a), (b) and (c). It also show the similar behavior as in the case of other types of faults. But difference in the apparent reactance measured with 100 MVA and 200 MVA STATCOM is less when compared with other types of faults.



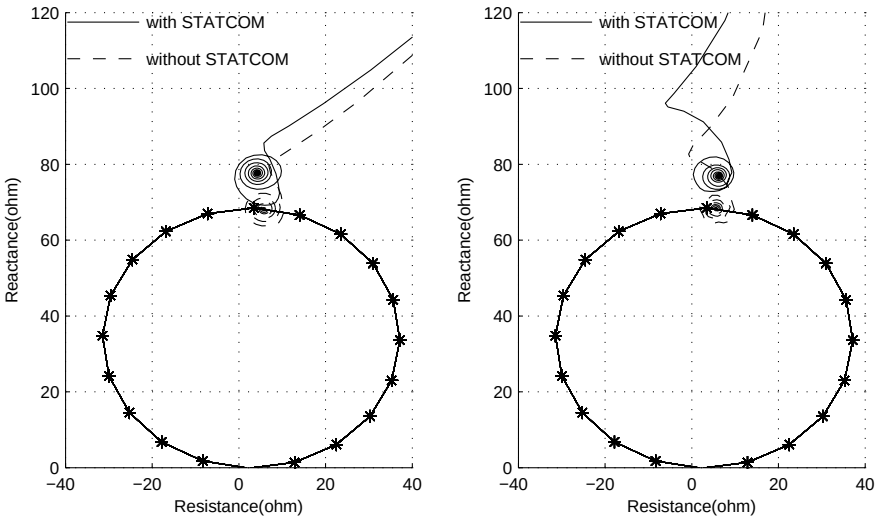
(a) $\delta = 15^0$

(b) $\delta = 35^0$

(c) $\delta = 55^0$

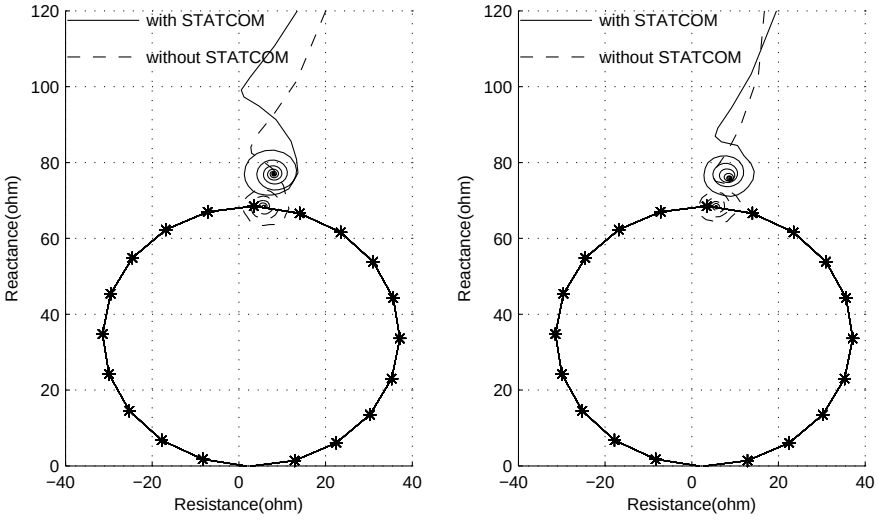
Figure 3.16: Reactance seen by the relay at different load angles (δ) for BC fault

The impedance trajectory seen by the relay, with and without 200 MVA STATCOM is plotted on the R-X diagram, for all types of faults at the reach setting of the relay(80% of the line) in the figure 3.17. It can be seen that the relay under reaches its setting in all cases.



(a) AG fault

(b) ABG fault



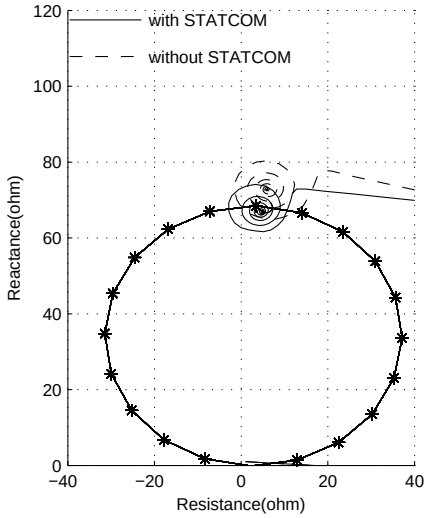
(c) ABC fault

(d) BC fault

Figure 3.17: Impedance trajectory seen by the relay with/without STATCOM(200 MVA)

3.5.3 VAR Control Mode

In the reactive control mode the mid point voltage was set at 0.95 p.u. This requires absorption of 100 MVAR inductive reactive power from the power system by the STATCOM controller. Therefore, quadrature current controller reference for the the $\pm$ 100 MVA STATCOM was set to 1.0 p.u. The voltage controller is inhibited from operation in this mode. A three phase fault at 170 KM on the transmission line was simulated and the result is presented in the figure 3.18. It can be seen from the figure that, the impedance trajectory seen by relay without STATCOM, settles outside the boundary of the mho relay setting, where as the relay saw the fault with STATCOM connected system. Hence the relay over reached its setting while operating in the reactive power control mode.



(a) ABC fault

Figure 3.18: Impedance trajectory seen by the relay with/without STATCOM(100 MVA) operating in reactive power control mode

The simulation results closely matched with the analytical results. Imperative inferences drawn from the simulation study, are summarized below,

- only case II category faults affect the distance protection performance
- STATCOM operating mode prior to fault occurrence influences relay reach

- influence of STATCOM is less severe for phase-phase faults
- apparent impedance increases with increase in STATCOM rating
- apparent impedance increases with increase in fault distance

From the above conclusions it is clear that, the standalone distance protection is not adequate to protect STATCOM connected transmission lines. The next chapter presents the development of an adaptive distance relaying scheme to mitigate the adverse impact of STATCOM on the distance protection.

CHAPTER 4

DEVELOPMENT and TESTING of ADAPTIVE DISTANCE RELAY

4.1 Introduction

The results of investigation in previous chapter proved that the STATCOM connected at the mid point, creates reach problems for the distance relay, deployed for the transmission line protection. The relay under-reached or over- reached zone setting, in the presence of STATCOM especially, for the faults beyond midpoint of the line. This also results in incorrect information about the fault location. But, accurate fault location information is valuable to operations personnel and power system protection engineers. This information helps to expedite the system restoration process. Now a days, impedance based fault location techniques are widely in use because it is simple and fast (Tziouvaras *et al.*, 2001). This technique makes use of fundamental frequency voltages and currents for the calculation of impedance. But, the relationship between voltage and current is disturbed when there is in-feed or out-feed, as in the case of STATCOM connected power systems. This can make the relay experience severe under-reach or over-reach problems. However, such undesired operations can be corrected through the deployment of futuristic concept, popularly known as; "adaptive relaying schemes". The adaptive protection makes automatic adjustments in various protection functions and computational procedures in order to make them respond to prevailing system conditions (Phadke, 1993; Coury *et al.*, 2000). This chapter presents the development of an adaptive distance relaying scheme and illustrates how this scheme mitigates reach problems posed by conventional relaying. The performance of newly proposed adaptive relaying scheme under various fault condition is evaluated through simulation studies and results are presented.

4.2 Development of Adaptive Distance Relay Scheme

The impedance seen by the relay for all types of faults with STATCOM has been derived in the previous chapter as,

$$Z_{Relay} = dZ_{L1} + (d - 0.5)Z_{L1}C_{ratio} \tag{4.1}$$

By rearranging the terms in the equation 4.1 the actual fault impedance can be calculated as given by the equation 4.2

$$dZ_{L1} = \frac{Z_{relay} + 0.5Z_{L1}C_{ratio}}{1 + C_{ratio}} \tag{4.2}$$

Where, C_{ratio} is the ratio of STATCOM current to the relay current, defined as the current ratio factor.

Equation 4.2 indicates that if the time stamped three phase STATCOM currents made available to the relay, fault impedance can be calculated accurately. To achieve this, a dedicated communication channel between relay location and STATCOM location should be established (Yu *et al.*, 2002; Chen *et al.*, 2002; Jiang *et al.*, 2003). Communication channel has not been modeled in this work. But for simulation purpose, STATCOM currents obtained through simulations are directly used in the relay program. The block diagram of the adaptive distance scheme along with the power system is shown in the fig.4.1.

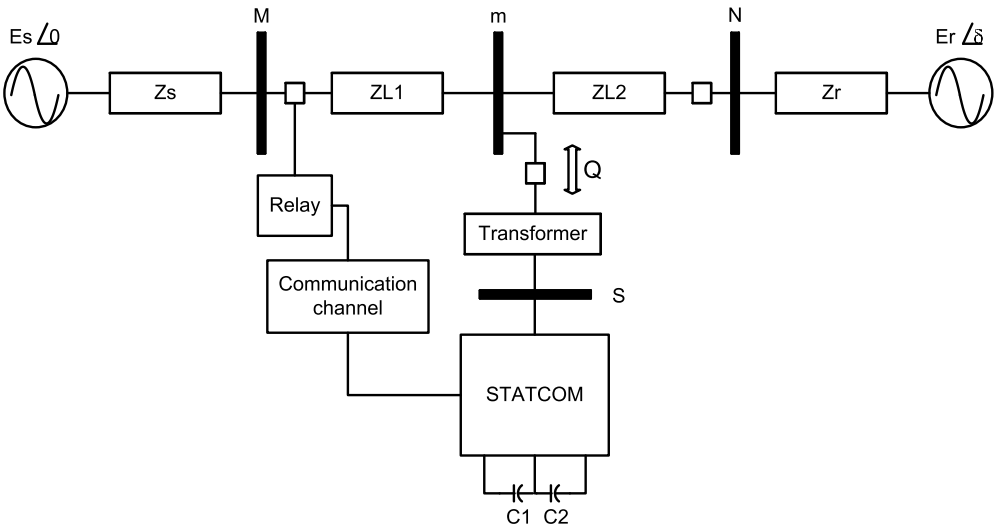


Figure 4.1: Block Diagram of the adaptive distance relaying scheme

From the analysis carried out in the previous chapter, it can be seen that the C_{ratio} is different for ground faults and phase faults. The C_{ratio} for phase-ground and phase-phase relay units can be calculated by using equations 4.3 and 4.4, respectively.

$$(C_{ratio})_x = \left[\frac{I_{st(x)}}{I_x + kI_{(0)}}\right] \tag{4.3}$$

Where, x $\in$ {A,B or C}

$$(C_{ratio})_{xy} = \left[\frac{I_{st(x)} - I_{st(y)}}{I_x - I_y}\right] \tag{4.4}$$

Where, x,y $\in$ {A,B,C} and x $\neq$ y.Where,

k : Zero sequence compensation factor of transmission line

$I_{st(x)}$: STATCOM phase X current

I_x : Phase x current at relay location

I_0 : Zero sequence current at relay location

The relay software automatically adapts equations 4.2 - 4.4 in impedance measurement procedure after being tested positive for a threshold impedance(Z_{thr}) condition.

The value of Z_{thr} is selected based on the simulation results obtained in chapter 3. These results indicated that the performance of the relay is affected only for the faults beyond the STATCOM installation point, which is 50% of the transmission line length. Therefore, Z_{thr} is set as 50% of the total positive sequence line impedance. Selection of this value for Z_{thr} ensures shift from conventional relay to adaptive relay for the faults beyond midpoint of the transmission line. In the sections that follow, the flow chart and the evaluation test results of the adaptive distance relay is presented.

4.2.1 Flow Sequence of Adaptive Relay Logic

The performance of the newly developed distance protection scheme, has been evaluated by using large set of test data generated through simulation. The fault data files obtained from EMTDC/PSCAD simulation, serves as the input test data for the evaluation of the adaptive relay. Adaptive distance relay program is developed in MATLAB. The filtered voltage and current signals from the EMTDC/PSCAD form input fault data set for feeding model developed in MATLAB. The fundamental voltage and current phasors are calculated using the full cycle window Fourier algorithm. The zero sequence component is computed using the three phase current phasors, which serves as the threshold to determine the fault type. The impedances computed by the phase - ground units and the phase - phase units are compared with the Z_{thr}. The relay software will switch to adaptive equations, whenever the measured impedance of any of the relays exceed Z_{thr}. This will compensate for the measured impedance error due to the STATCOM. After computing the fault impedance, phase/phases which are involved in the fault are detected using the faulted phase detection algorithm (K.P.Vittal, 1999). The results of the evaluation tests conducted to assess the performance of the adaptive relay are presented in the following paragraphs. The complete software sequence of the adaptive relay is shown in figure 4.2, and the sequential procedural steps are given below :

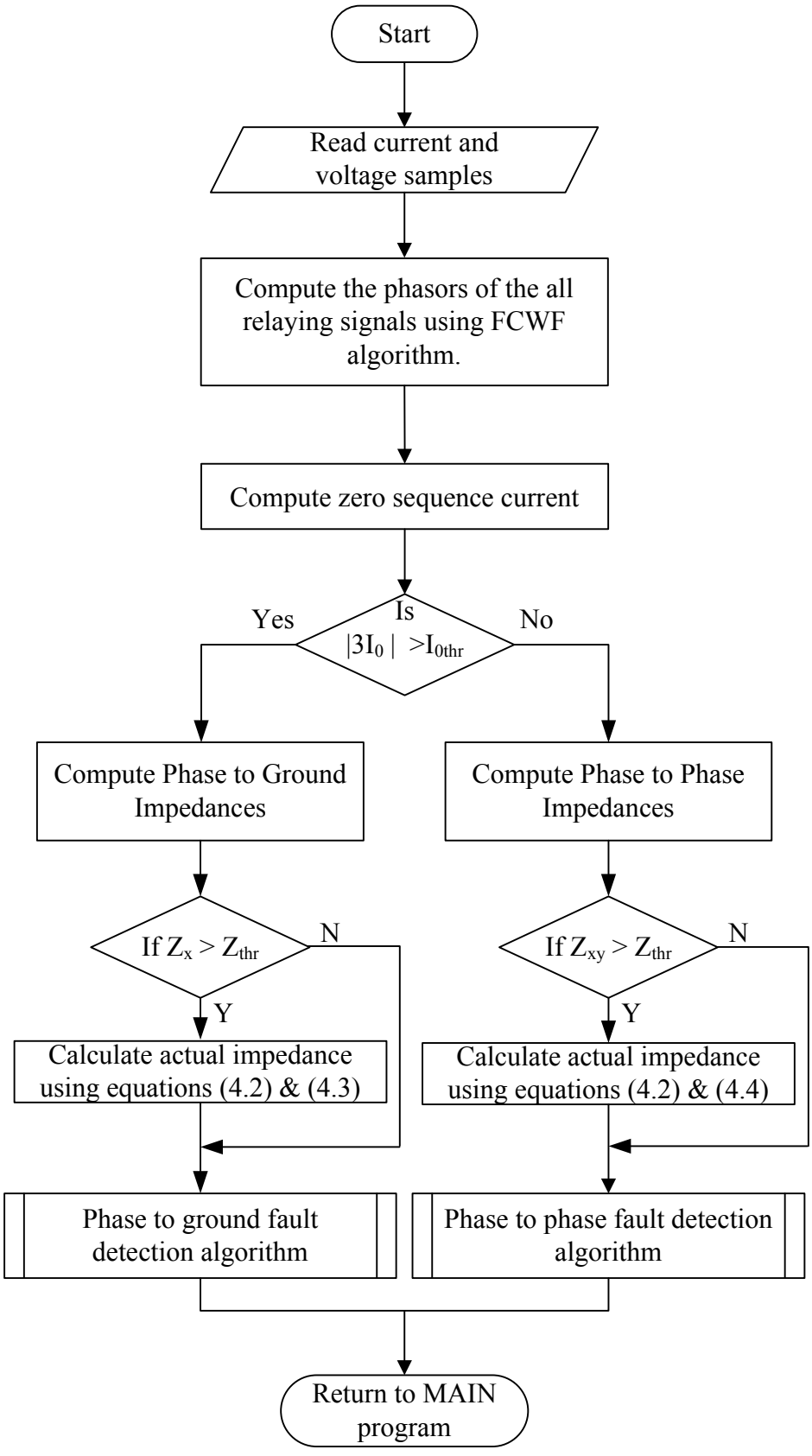


Figure 4.2: Adaptive distance relay logic flow diagram

Step 1: once relay logic sub-program is called in main loop of relaying program, samples of all nine required relaying signals namely, three-phase voltages, three-phase currents at relay location and three-phase STATCOM currents are read from the fault data files.

Step 2: The relay operation cycle begins, with the extraction of fundamental phasors of all the relaying quantities, using FCWF algorithm. The equations for computing the fundamental frequency sine/cosine components using FCWF algorithm are given as,

$$X_s = \frac{2}{N}\sum_{i=1}^{N} X_{(k-N+i)} sin\left(\frac{2\pi i}{N}\right) \tag{4.5}$$

$$X_c = \frac{2}{N}\sum_{i=1}^{N} X_{(k-N+i)} cos\left(\frac{2\pi i}{N}\right) \tag{4.6}$$

Where, N=Number of samples per cycle

k= sampling point

X_s, X_c =sine, cosine components of the fundamental frequency signal.

From these components, the magnitude and phase of the fundamental frequency signal can be calculated as,

$$X_m = \sqrt{X_s^2 + X_c^2} \tag{4.7}$$

$$\theta_X = \tan^{-1}\left(\frac{X_s}{X_c}\right) \tag{4.8}$$

FCWF has band pass structure and has wide acceptance in accurate extraction of specific frequency phasor. Figure 4.3 shows its frequency response when tuned for extracting fundamental component phasor. The frequency response characteristic consists of a main lobe followed by side lobes, with zero gain for d.c. and all integral harmonics. The fundamental frequency has a gain of unity.

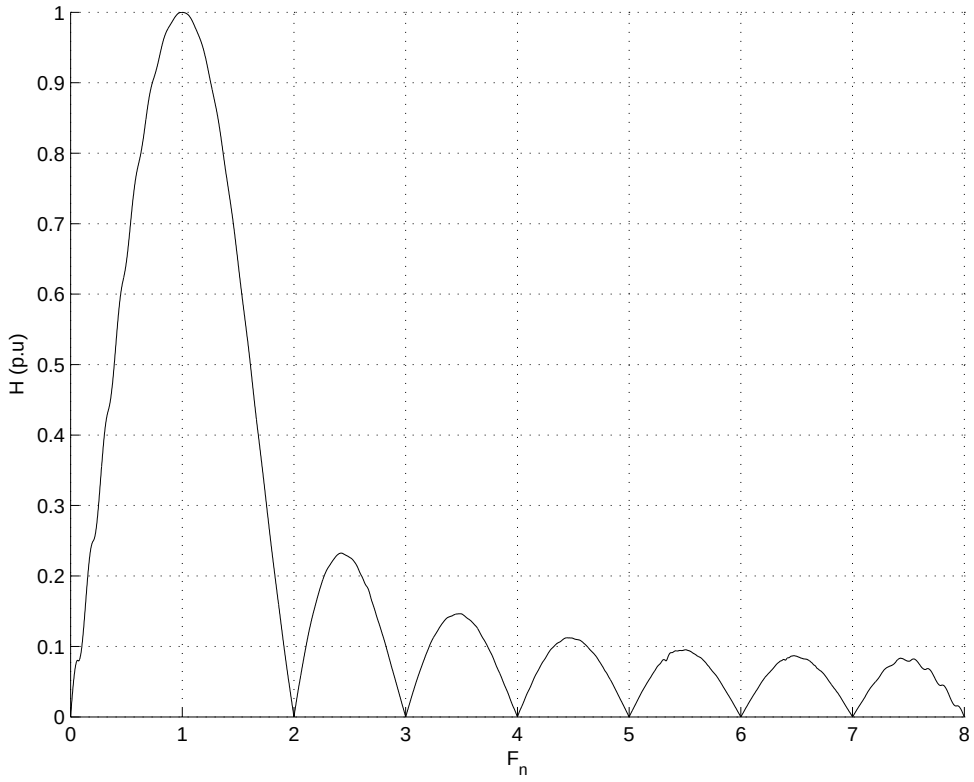


Figure 4.3: Frequency response of FCWF algorithm.

Step 3: To have a criterion for classifying the fault as a grounded fault or phase fault, the zero sequence current (I_0) at the k^{th} sampling instance is calculated from the samples of relaying current signals as,

$$3I_0(k) = (I_a(k) + I_b(k) + I_c(k)) \tag{4.9}$$

Step 4: If $3I_0(k)$ magnitude exceeds a threshold I_{0thr} (0.1 p.u.) then, fault is considered to be ground fault, else it is treated as phase fault.

Step 5: The ground(Z_x) or phase(Z_{xy}) impedances are computed as determined in above step, using the formula mentioned in the table 3.2 of chapter 3 as,

$$Z_x = \frac{V_x}{I_x + 3KI_0} \tag{4.10}$$

$$Z_{xy} = \frac{V_x - V_y}{I_x - I_y} \tag{4.11}$$

Step 6: The computed values of Z_x and Z_{xy} are compared with the Z_{thr} to determine whether fault location is beyond 50% of the line length from the relay end.

Step 7: If the step 6 returns true, then equations 4.2-4.3 and 4.3- 4.4 are adapted by ground and phase impedance relays respectively for accurate impedance calculations. Then goto step 8; Else goto step 8.

Step 8: Relay logic subprogram is initiated to check for fault/no-fault status of the system. The relay logic subprogram compares the computed (R,X) with (R,X) setting of the relay. The fault is detected, if computed (R,X) falls in the trip region of the relay. If the relay logic detects a fault, then the trip counter is incremented, otherwise it will be reset. When trip counter, counts 3, trip signal is issued. Determine the type of fault and phases involved in the fault, using the fault detection algorithm.

Step 9: Return to Main program.

The above steps are performed in the relaying algorithm at each sampling point 'k'. The performance of the adaptive relay has been evaluated by considering various fault scenarios on model power system. In this work both mho and quadrilateral type relays have been implemented for the purpose of fault detection. The following sections presents the development of both types of relays in detail.

4.2.1.1 Mho relay characteristic implementation

The protection relay of this type simply calculates apparent impedance of the line under its protection. This measured impedance from relay to fault location is then compared with the protection reach settings. If line impedance measured falls within relay characteristics it will operate and issue trip signal. Figure 4.4 shows the mho relay characteristics selected for implementation.

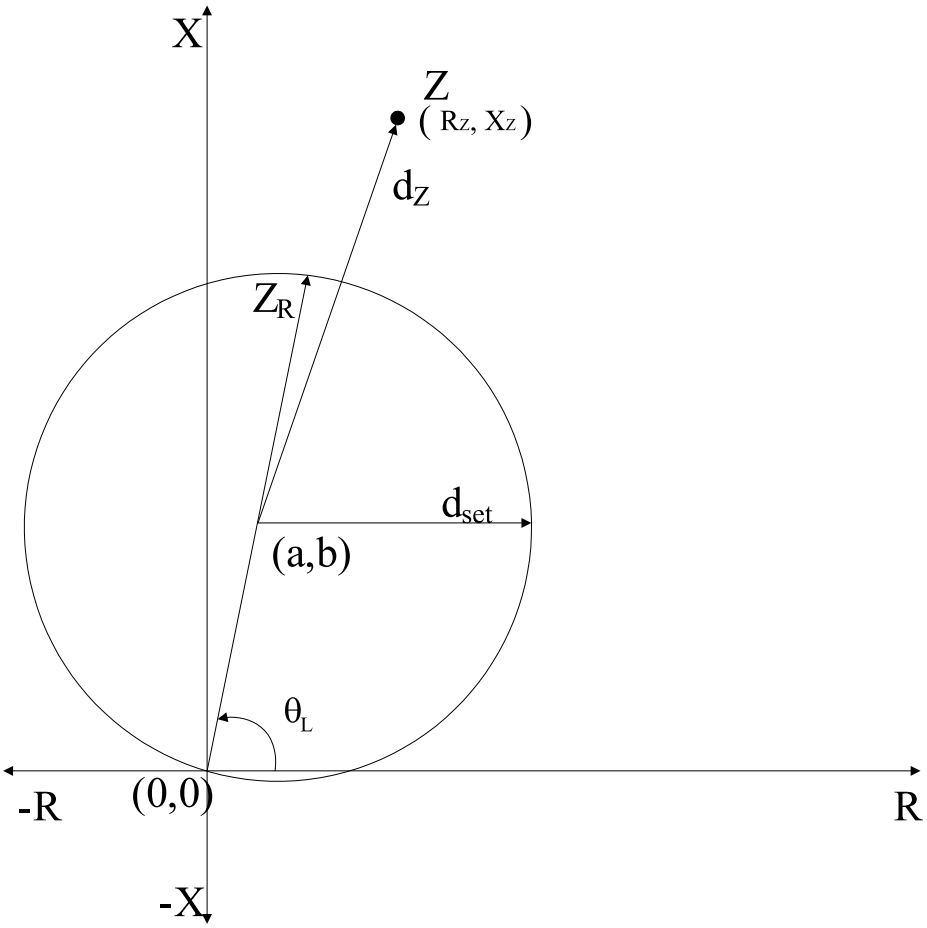


Figure 4.4: Mho relay characteristics chosen for implementation.

Where,

a and b are the circle center co-ordinates

R_Z and X_Z are the resistance and reactance components of Z

d_Z is the distance between center of the circle to Z

Z_R is the reach setting of the relay

θ_L is the transmission line angle

d_{set} is the radius of the mho circle.

The following sequence of steps explains implementation of mho relay logic with the help of flow chart shown in figure 4.5 by considering a sample apparent impedance Z computed at present sampling instant.

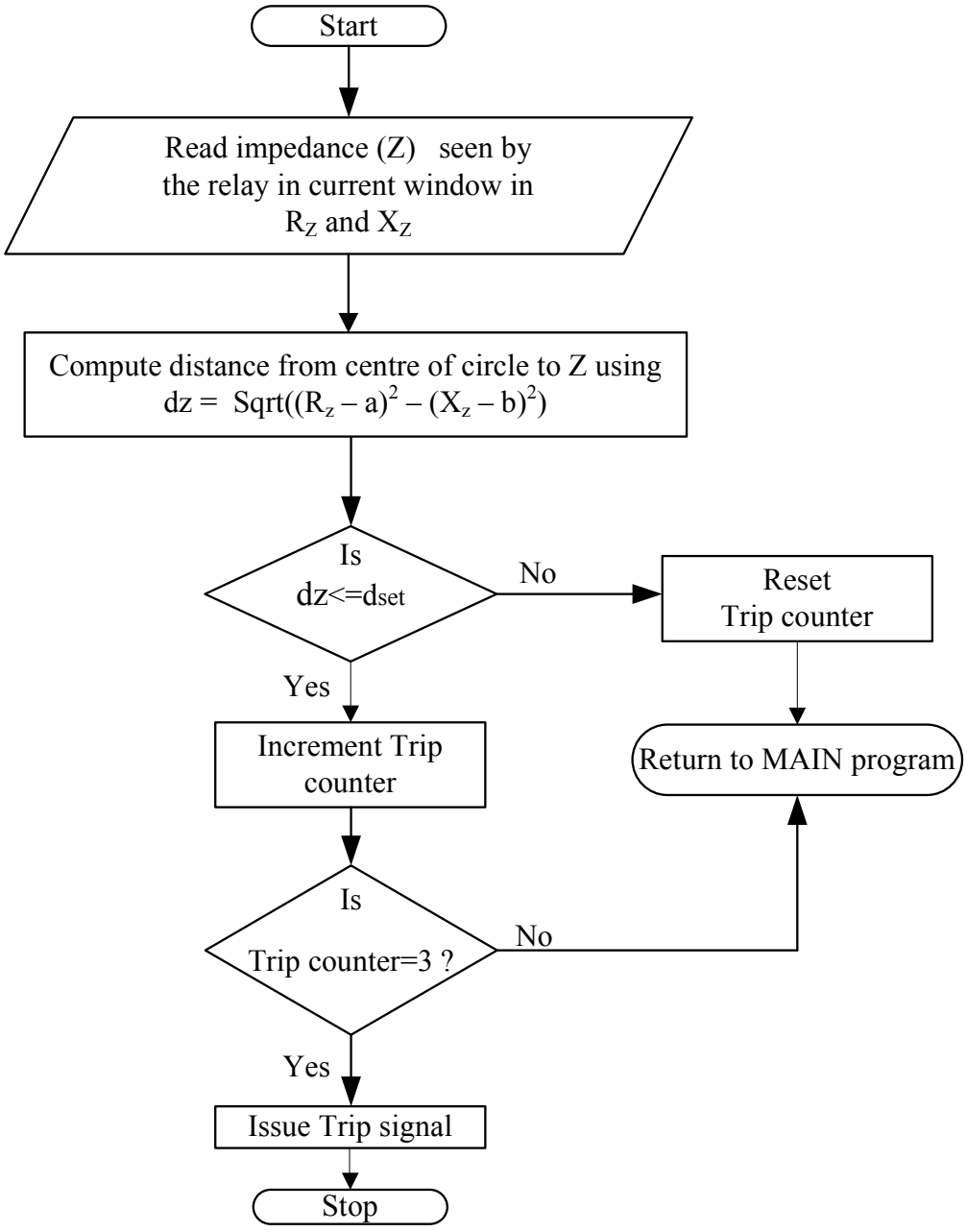


Figure 4.5: Flow chart of mho relay logic

Step 1 : Read the resistive (R_z) and reactive (X_z) components apparent impedance Z computed in the current sampling instant.

Step 2 : Compute the distance from center of the circle (a,b) to Z using the distance formula given below;

$$d_Z = \sqrt{(R_Z - a)^2 + (X_Z - b)^2} \tag{4.12}$$

Step 3 : Evaluate : $d_Z \leq d_{set}$, to determine whether, the impedance point lies inside the trip boundary or not. If this condition returns true, implies that apparent impedance Z lies inside mho circle. Hence, increment trip counter and goto Step 4.
else, reset trip counter and goto Step 5.

Step 4 : The relay has been programmed to issue trip signal only after ensuring measured impedance falling inside the circle three times consecutively, failing which the trip counter will be reset. This is done in order to inhibit false tripping of the relay for momentary transient signals. Therefore the value of Trip counter is compared with 3. If the condition is found to be true, then issue the trip signal and goto step 6; Else goto step 5

Step 5 : Return to main program.

Step 6 : Display trip status and wait for operator / remote control input probing loop program.

The same logic is used in both ground and line type mho relays to detect the faults.

4.2.1.2 Quadrilateral relay characteristic implementation

The mho relay logic has been incorporated just to compare relay performance with conventional relay types. But, since numerical relays give flexibility of shaping relay characteristics, the performance is evaluated with specifically shaped quadrilateral characteristics. Section that follows explains program to implement this relay logic.

The mho type relays under-reach zone settings, in case of resistive faults due to lack of resistive reach capability. Therefore, quadrilateral relays are preferred in such cases. The resistive reach of quadrilateral relay can be set to cover fault resistance without affecting the reactive reach of the relay. Typical quadrilateral characteristic is shown in figure 4.6. It is formed by 4 lines L_1,L_2,L_3 and L_4; Where, (L_1x_1 , L_1y_1) and (L_1x_2 , L_1y_2) are the pair of points, which define position of lines on a two - dimensional plane. Z(R_Z ,X_Z) is the apparent impedance seen by relay at the present sampling instant. R_Z and X_Z are resistive and reactive components of Z.

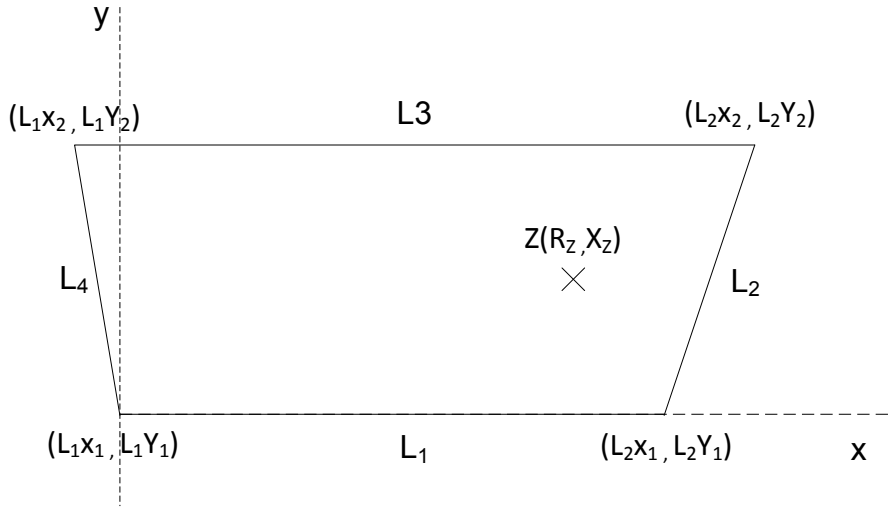


Figure 4.6: Typical quadrilateral characteristic

The quadrilateral relay evaluates position of Z in-order to confer trip decision. Relay issues trip signal only if the point Z lies inside its operating zone. The relay program considers one side of quadrilateral at a time and determines position of Z with respect to the line using equation 4.13. It is illustrated below by considering line L_2 and Z,

$$S_2 = dot((p - p1), pv) \tag{4.13}$$

Where,

$p = (R_z, X_z)$; point to be tested

$p1 = (L_2x_1, L_2y_1)$; starting point of line L_2

pv = perpendicular vectors given by equation 4.14

$$\begin{bmatrix} L_2x_1 - L_2x_2 \\ L_2y_1 - L_2y_2 \end{bmatrix} \tag{4.14}$$

Substituting values of p p_1 and pv in equation 4.13 yields,

$$S_2 = dot \begin{bmatrix} R_z - L_2x_1 & L_2x_1 - L_2x_2 \\ X_z - L_2y_1 & L_2y_1 - L_2y_2 \end{bmatrix} \tag{4.15}$$

Value of S_2 can be obtained by performing the dot product operation, as shown in equation 4.16, which is used as discriminator to determine the position of Z

$$S_2 = (R_z - L_2x_1) * (L_2y_1 - L_2y_2) - (X_z - L_2y_1)(L_2x_1 - L_2x_2) \tag{4.16}$$

S_2 = 0; point lies on the line L_2

$S_2 < 0$; point lies on RHS of the line L_2

$S_2 > 0$; lies on LHS of the line L_2

This procedure is applied to all lines and position of Z with respect to each line is evaluated. The following sequence of steps explains implementation of quadrilateral relay logic with the help of flow chart shown in figure 4.7.

Step 1 : Read the resistive (R_z) and reactive (X_z) components apparent impedance Z computed in the current sampling instant.

Step 2 : Compute the value of discriminators S_1, S_2, S_3 and S_4 of lines L_1, L_2, L_3 and L_4 respectively using equation 4.16.

Step 3 : In the figure 4.6 for the point Z to be inside the quadrilateral it should satisfy the following conditions.

$S_1 \geq 0$, i.e. Z has to be on above of line L_1

$S_2 \geq 0$, i.e. Z has to be on LHS of line L_2

$S_3 \leq 0$, i.e. Z has to be on below of line L_3

$S_4 \leq 0$. i.e. Z has to be on RHS of line L_4

Evaluation of these conditions are performed sequentially starting from S_1 to S_4. The result of evaluation at each stage decides the flow sequence of the program. The evaluation of subsequent condition is considered if the result of previous stage returns true, otherwise reset the trip counter; goto step 6.

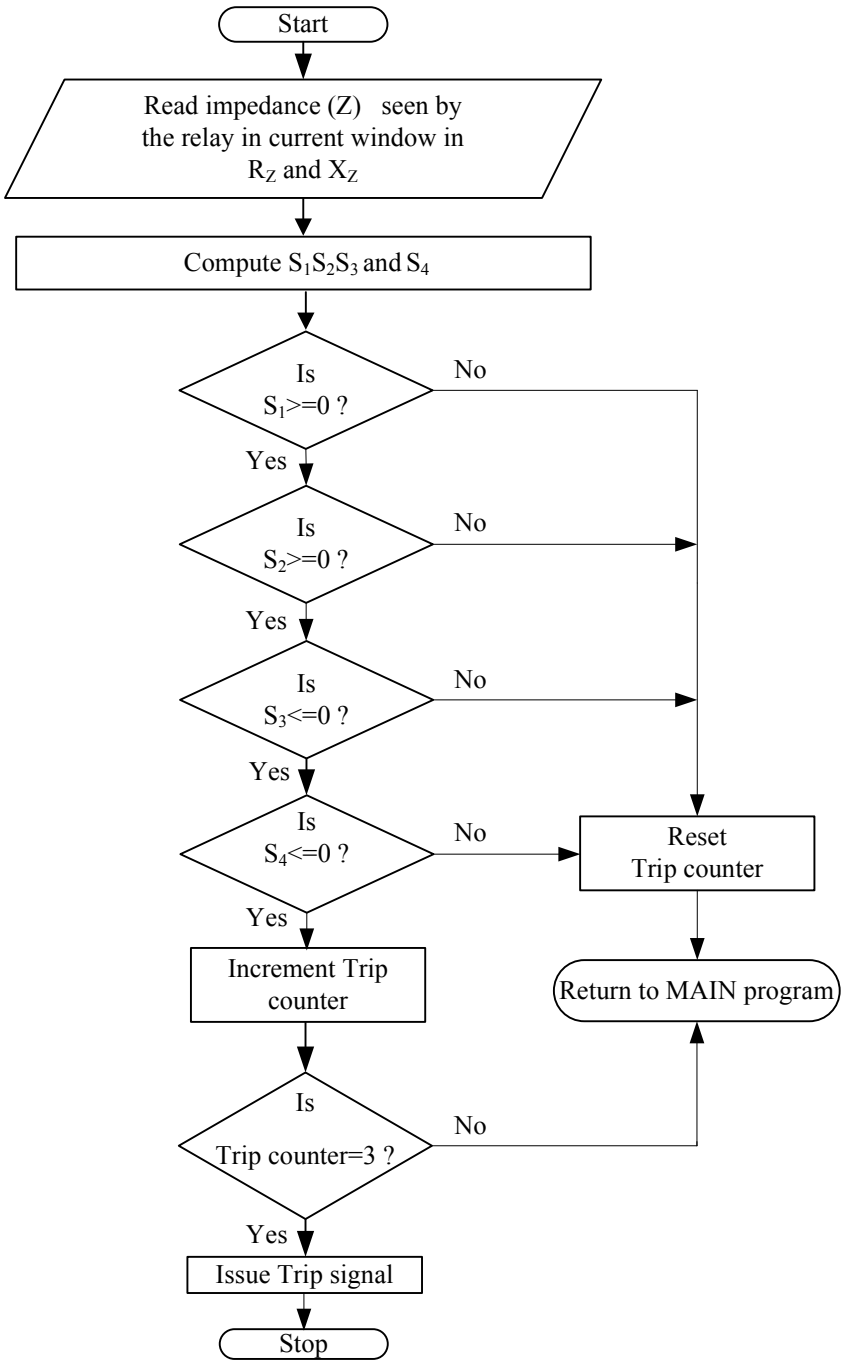


Figure 4.7: Flow chart of quadrilateral relay implementation

Step 4 : If $S_4 \leq 0$ is true, it implies that the point Z lies inside the trip characteristic. Hence increment the trip counter.

Step 5 : Evaluate Tripcounter =3: issue trip signal if condition is true, goto step 7.

Else goto step 6.

Step 6 : Return

Step 7: Stop

The following section presents the simulation results for various types of faults.

4.2.2 Simulation Results

The figure 4.8 shows the performance of conventional relay and the adaptive relay for STATCOM connected transmission line for phase - ground zone end fault (i.e, 80% of the line).

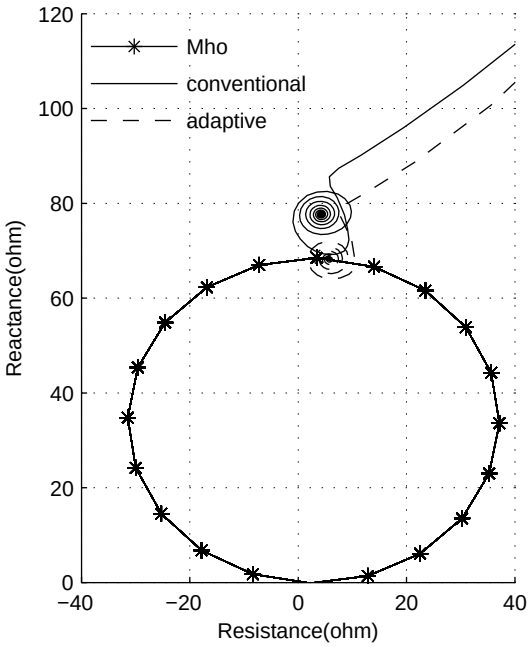


Figure 4.8: Performance of conventional and adaptive relays for phase to ground zone end fault

It can be seen that the adaptive relay measures the exact fault impedance with MHO characteristics and impedance trajectory settles on the boundary of the relay. Whereas, the impedance trajectory seen by the conventional relay settles outside the trip characteristic, causes the relay to under-reach. Simulations have been carried out on the entire

range of relay operation and the results are tabulated in the table 4.1. It can be seen that the impedance measured by the adaptive relay with STATCOM is almost the same as that of the impedance seen by the conventional relay without STATCOM. This indicates that apparent impedance measured by adaptive relay is free from transient reach error due to STATCOM and do not maloperate.

Table 4.1: Performance of conventional and adaptive relays for phase to ground(AG) faults

Fault distance	Conventional relay				Adaptive relay	
	Without STATCOM		With STATCOM		With STATCOM	
	Resistance	Reactance	Resistance	Reactance	Resistance	Reactance
(KM)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)
20.00	0.71	8.46	0.71	8.46	0.71	8.46
40.00	1.43	16.92	1.43	16.92	1.43	16.92
60.00	2.15	25.39	2.15	25.39	2.15	25.39
80.00	2.87	33.87	2.87	33.87	2.87	33.87
100.00	3.61	42.38	3.61	42.37	3.61	42.38
110.00	3.97	46.66	3.70	47.71	3.94	47.00
120.00	4.33	50.94	3.74	53.25	4.27	50.86
130.00	4.70	55.22	3.71	58.98	4.71	55.13
140.00	5.08	59.52	3.65	64.93	5.12	59.62
150.00	5.46	63.82	3.46	71.04	5.48	64.02
160.00	5.85	68.13	3.28	77.37	5.80	68.32

Similarly, impedance trajectories for zone end three phase, line-line and double line to ground faults are shown in the figures 4.9, 4.10 and 4.11 respectively. From these figures it can be observed that conventional relay under-reached first zone setting for all types of faults, but the adaptive relay has seen the correct impedance to the fault.

Tables 4.2, 4.3 and 4.4 show the impedance measured by conventional and adaptive relays for the above mentioned fault cases. It can be seen that in these cases also, fault impedance measured by the adaptive distance relay is free from the influence of STATCOM.

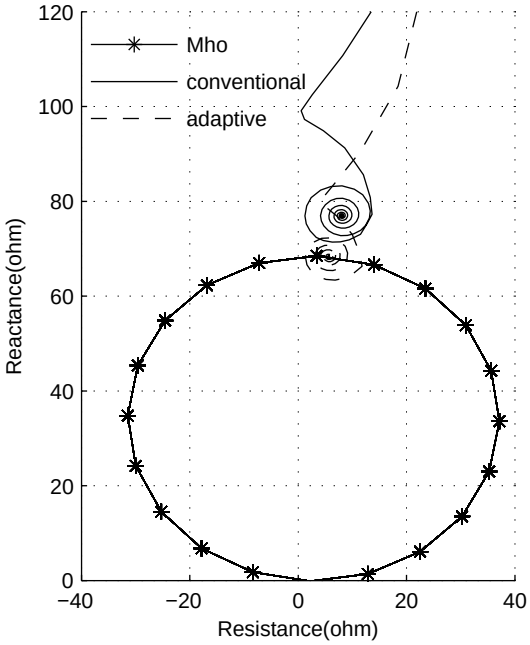


Figure 4.9: Performance of conventional and adaptive relays for three phase zone end fault

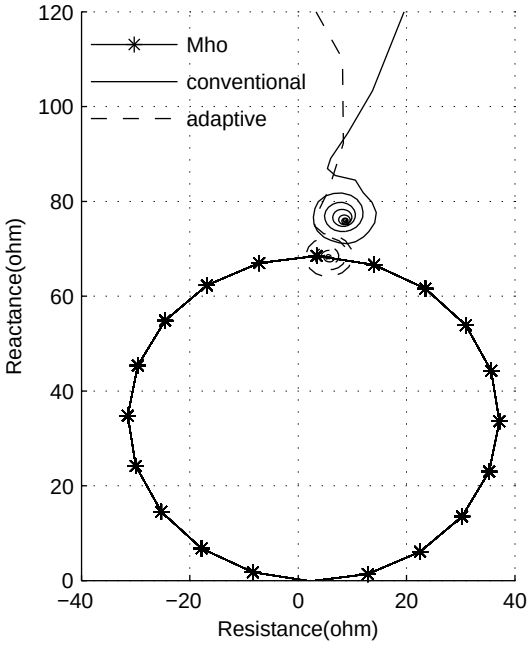


Figure 4.10: Performance of conventional and adaptive relays for phase-phase zone end fault

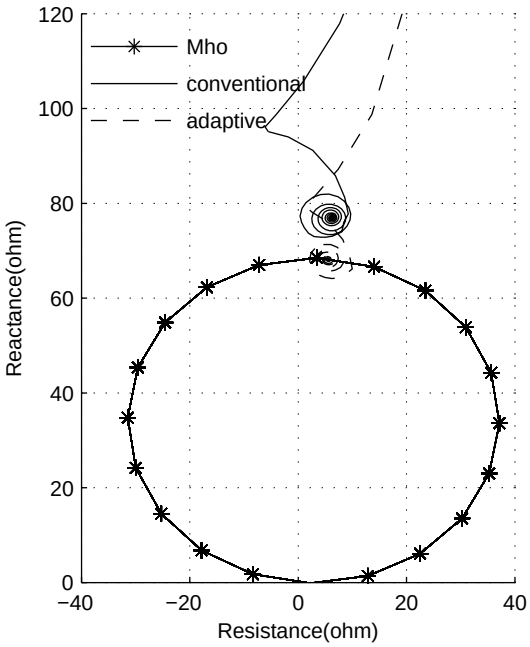


Figure 4.11: Performance of conventional and adaptive relays for L-L-G zone end fault

Table 4.2: Performance of conventional and adaptive relays for three phase(ABC) faults

Fault distance	Conventional relay				Adaptive relay	
	Without STATCOM		With STATCOM		With STATCOM	
	Resistance	Reactance	Resistance	Reactance	Resistance	Reactance
(KM)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)
20.00	0.70	8.47	0.70	8.47	0.70	8.47
40.00	1.40	16.94	1.40	16.94	1.40	16.94
60.00	2.10	25.43	2.10	25.43	2.10	25.43
80.00	2.81	33.94	2.81	33.94	2.81	33.94
100.00	3.53	42.48	3.52	42.48	3.53	42.48
110.00	3.89	46.77	4.01	47.20	3.89	46.80
120.00	4.26	51.07	4.83	52.89	4.14	51.05
130.00	4.62	55.38	5.63	58.74	4.59	55.44
140.00	5.00	59.70	6.38	64.63	4.90	59.39
150.00	5.37	64.03	7.24	70.72	5.26	64.11
160.00	5.75	68.38	8.08	77.02	5.72	68.58

Table 4.3: Performance of conventional and adaptive relays for line to line (BC) faults

Fault distance	Conventional relay				Adaptive relay	
	Without STATCOM		With STATCOM		With STATCOM	
	Resistance	Reactance	Resistance	Reactance	Resistance	Reactance
(KM)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)
20.00	0.70	8.47	0.70	8.47	0.70	8.47
40.00	1.40	16.94	1.40	16.94	1.40	16.94
60.00	2.10	25.43	2.10	25.43	2.10	25.43
80.00	2.81	33.94	2.81	33.94	2.81	33.94
100.00	3.53	42.48	3.53	42.48	3.53	42.48
110.00	3.89	46.77	4.25	47.03	3.89	46.68
120.00	4.26	51.07	5.01	51.95	4.31	51.00
130.00	4.62	55.38	5.85	57.12	4.58	55.44
140.00	5.00	59.70	6.83	62.73	4.93	59.53
150.00	5.37	64.03	7.96	68.65	5.33	64.10
160.00	5.75	68.38	9.19	75.33	5.71	68.41

Table 4.4: Performance of conventional and adaptive relays for L-L-G (BC-G) faults

Fault distance	Conventional relay				Adaptive relay	
	Without STATCOM		With STATCOM		With STATCOM	
	Resistance	Reactance	Resistance	Reactance	Resistance	Reactance
(KM)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)	(ohm)
20.00	0.70	8.45	0.70	8.45	0.70	8.45
40.00	1.40	16.91	1.39	16.91	1.39	16.89
60.00	2.09	25.38	2.09	25.38	2.09	25.35
80.00	2.79	33.88	2.79	33.87	2.79	33.82
100.00	3.49	42.39	3.48	42.39	3.51	42.39
110.00	3.85	46.68	4.26	47.27	3.56	46.68
120.00	4.20	50.97	4.88	52.44	4.18	50.97
130.00	4.56	55.27	5.32	57.93	4.56	55.27
140.00	4.92	59.58	5.71	63.79	4.82	59.52
150.00	5.27	63.90	5.94	70.00	5.27	63.58
160.00	5.63	68.23	6.32	77.02	5.62	68.16

As discussed in the previous chapter, the conventional relay over-reached zone setting for three phase fault during lightly loaded condition. The adaptive relay has also been subjected to same operating condition in-order to evaluate its response. The simulation result for this case is shown in the figure 4.12. It can be seen that the adaptive relay has seen the correct impedance to the fault and does not maloperate.

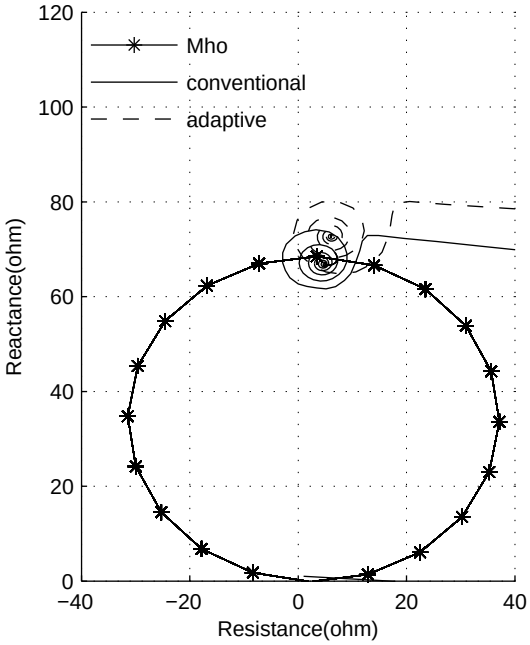


Figure 4.12: Performance of conventional and adaptive relays for fault out side relay trip zone

The practical power system faults are not ideal, but instead they involve fault resistance (R_f). For phase faults the fault arc between two conductors acts as fault resistance, where as the arc between conductor and shield wire or tower footing resistance is the source for fault resistance in case of ground faults. Therefore, simulations have also been extended to study influence of fault resistance on performance of the relay. Both phase and ground faults with R_f up-to 50 Ω have been simulated.

The figure 4.13 shows the ground relay characteristic. It is obtained by applying single line to ground fault (AG) on the transmission line at an interval of 10 Km each from sending to reach setting of the relay for various values of R_f and actual STATCOM quadrature current (I_q). The I_q values of 0.25 p.u, 0.50 p.u. and 1.00 p.u have

been considered for simulation. For each value of I_q, AG fault has been applied as mentioned above by considering different values of R_f = 0,10,20,30,40 and 50 Ω respectively and the steady state impedance is recorded. Each values of measured impedance is resolved into resistive and reactive components and plotted on a R-X diagram. This results in set of relay characteristics pertaining to selected values of I_q and R_f combinations respectively. The accuracy of the relay can be enhanced by obtaining more set of characteristics at smaller steps of I_q.

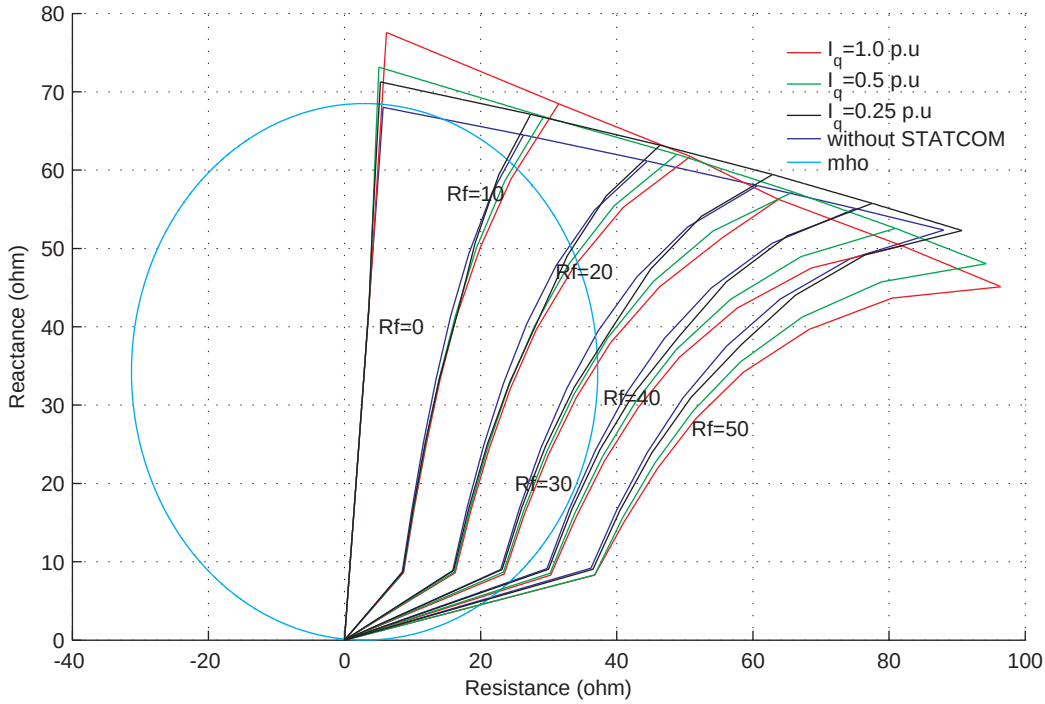


Figure 4.13: Ground relay trip characteristics

The following observations have been made from the figure 4.13.

- The measured impedance increases with increase in the STATCOM rating.
- The measured impedance increases with increase in the value of R_f.
- The solid faults (R_f=0) affect measured impedance values for case II types of faults(i.e. faults transpiring after STATCOM) only. Whereas, measured impedance values are influenced by STATCOM for both case I and case II types of faults when $R_f \neq 0$. This error increase with the increase in the value of R_f.
- Mho relay severely under-reach zone setting, when R_f is involved in the fault.
- Quadrilateral characteristic offers superior reach coverage and enhances the accuracy of the relay.

From the above discussions it can be inferred that, the actual relay characteristics derived by simulation studies are desired against the stand alone mho characteristic for the protection of STATCOM connected transmission line. The figure 4.14 shows the realization of actual trip characteristic for I_q=1.0 p.u. and R_f = 50 Ω. The actual trip characteristic is formed by three straight lines and a curve on the right hand side. This curve shape has been retrofitted with short line segments, viz., L_1, L_2, L_3 and L_4 without loss of accuracy.

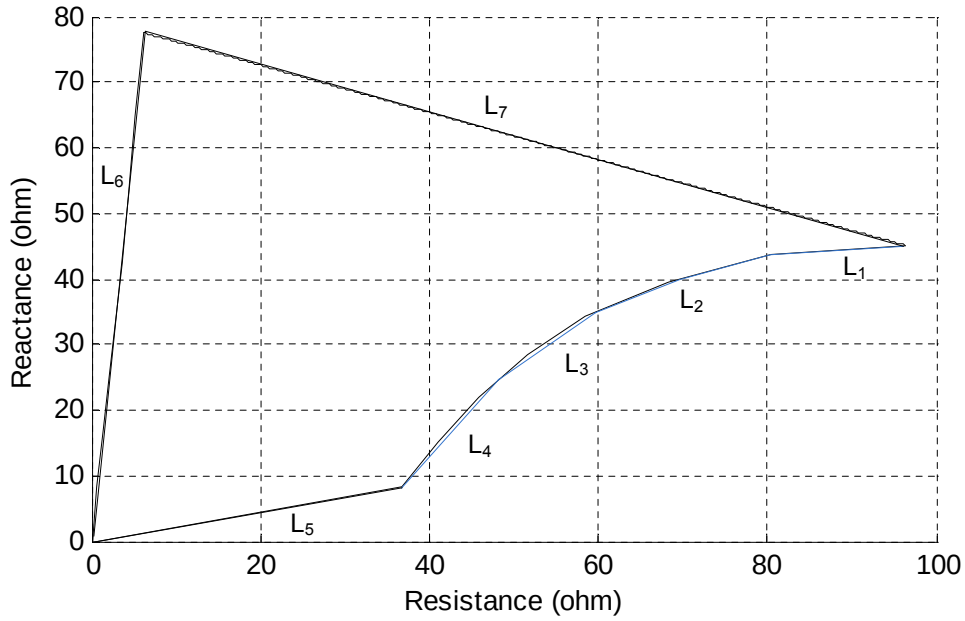


Figure 4.14: Realization of actual trip characteristic

In total the trip characteristic is comprised of 7 line segments L_1 - L_7. The coordinates of all the line segments are stored in the look up table (LUT). The trip counter will be incremented if the measured impedance in the present sampling window falls inside the relay characteristic.

The following sequence of steps describes the quadrilateral relay sub program implementation along with the flow chart shown in figure 4.15.

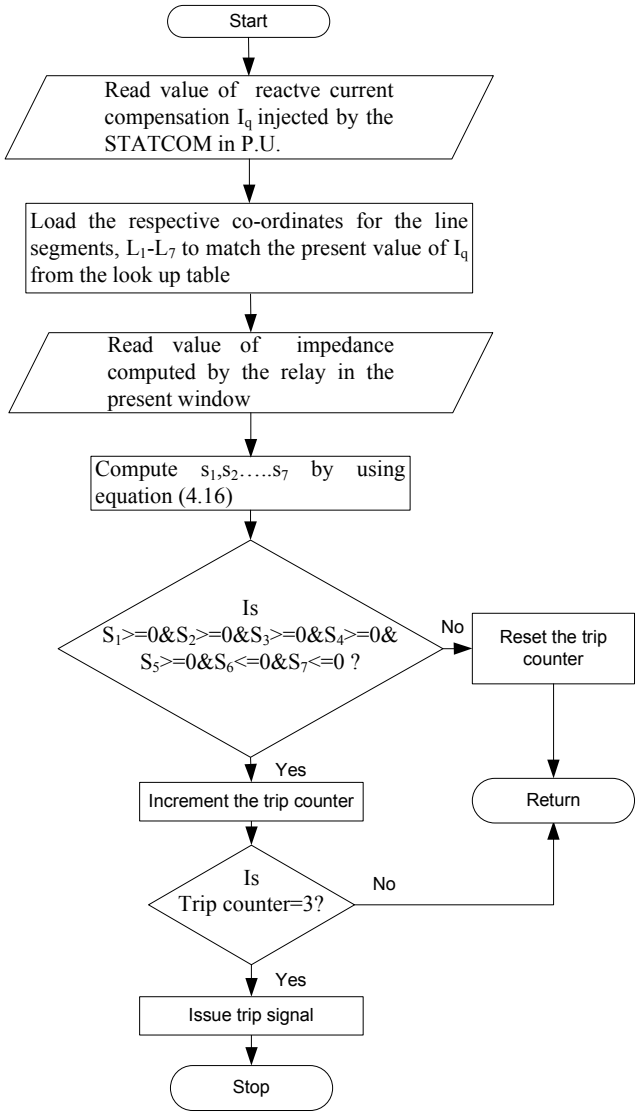


Figure 4.15: Adaptive relay flowchart

Step 1 : Read the value of STATCOM reactive current I_q. This is accomplished using a communication link between STATCOM location and the relay installation point.

Step 2: Load the respective co-ordinates for the line segments, L_1 - L_7 to match the present value of I_q from the look up table.

Step 3: Read value of impedance(Z) computed by the relay in the present window.

Step 4: In-order to determine whether Z lies inside the relay characteristic or not a discriminator S has been evaluated for each line segment. The value of S for any line

segment n can be calculated using the equation 4.16. Details of this derivation can be found in the section 4.2.1.2 of the thesis.

Step 5: The value of S determines the position of Z with respect to line n as given below.

S_n = 0; point lies on the line L_n

$S_n < 0$; point lies on RHS of the line L_n

$S_n > 0$; lies on LHS of the line L_n

.

Therefore for a point z to be inside relay characteristic shown in the figure 4.14 it must satisfy the following condition

$S1 >= 0 \& S2 >= 0 \& S3 >= 0 \& S4 >= 0 \& S5 >= 0 \& S6 <= 0 \& S7 <= 0$ If this condition return false, then reset the trip counter , return else increment the trip counter.

Step 6: Check for trip counter value =3

If no , return If yes issue trip signal.

Step 7: Stop

This adds three additional if-else structures in relay software program when compared with the quadrilateral characteristic described in the section 4.2.1.2. But by virtue of state-of-the-art digital signal controller used in this work, such computations can be handled conveniently. The features and details of hardware implementation are discussed in the next chapter.

Similar simulations have been carried out to frame the phase relay characteristic. The simulation results are presented on a R-X diagram as shown in the figure 4.16.The following observations have been made from the figure.

- The measured impedance increases with increase in the STATCOM rating. But for lower range of I_q values difference in the measured impedance is not significant. This can verified from the relay characteristics obtained with I_q=0.5 p.u. and 0.25 p.u. shown in the figure 4.16.
- The measured impedance increases with increase in the value of R_f as in the case of ground relays. But it is less when compared with the ground relays.
- The STATCOM influences the measured impedance of faults belonging to both

the cases, whenever R_f is involved in the fault.

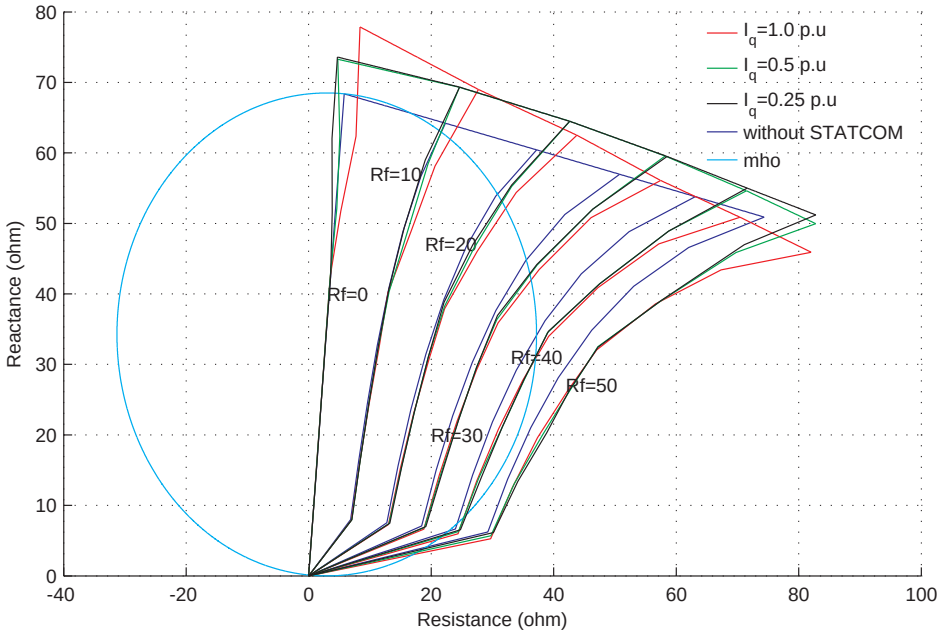


Figure 4.16: Phase relay trip characteristics

The simulation results hint at making use of I_q in designing adaptive relay setting for the system under consideration. For the faults during voltage control mode, STATCOM injects 1.0 p.u. reactive power as the voltage at the PCC will be much below the set reference value (Ghorbani, 2011). Therefore, under this mode of operation relay adapts characteristic corresponding to I_q = 1.0 p.u.

For the faults during VAR control mode, value of I_q is necessary. The value of I_q is computed by using the STATCOM currents acquired at the relay location or I_q computed by the STATCOM controller at the STATCOM location may be acquired from the same communication link. Depending upon the value of I_q the relay program enforces the respective relay characteristic. This process is continuous and relay attunes itself to the prevailing value of I_q. In this relaying scheme real time values of STATCOM current is not necessary, while performing the impedance computation, but it is required at regular intervals for computation of I_q. Whereas, in the adaptive scheme presented in the section 4.2 time stamped STATCOM currents are necessary to compute the phase and ground impedances.

In-order to test performance of the relay it has been subjected to various fault conditions. The figures 4.17 and 4.18 shows the impedance trajectory seen by the ground and phase relays for zone end single line to ground fault(AG) and phase-phase fault(BC) respectively. In both the cases I_q and R_f have been set to 1.0 p.u. and 50 Ω respectively. It can be seen that relay enforces quadrilateral characteristic derived with I_q=1 p.u. in both the cases and detects the fault on the boundary corresponding to R_f = 50 Ω.

Same faults have been applied with I_q=0 p.u. emulating no STATCOM condition. In this case both ground and phase relays have invoked the relay characteristic fitted with I_q=0 p.u. (without STATCOM) and detects the fault on the boundary corresponding to R_f = 50 Ω.

Similarly, a zone end BC fault with R_f = 25 Ω has been applied with I_q=1.0 p.u. The figure 4.19 shows the impedance trajectory seen by the relay. Here also the relay enforces quadrilateral characteristic derived with I_q=1.0 p.u., but detects the fault on the boundary corresponding to R_f = 30 Ω. From the same figure it may be observed that for system without STATCOM relay invokes relay characteristic fitted with I_q=0 p.u. and detects the fault near the relay boundary corresponding to R_f = 30 Ω.

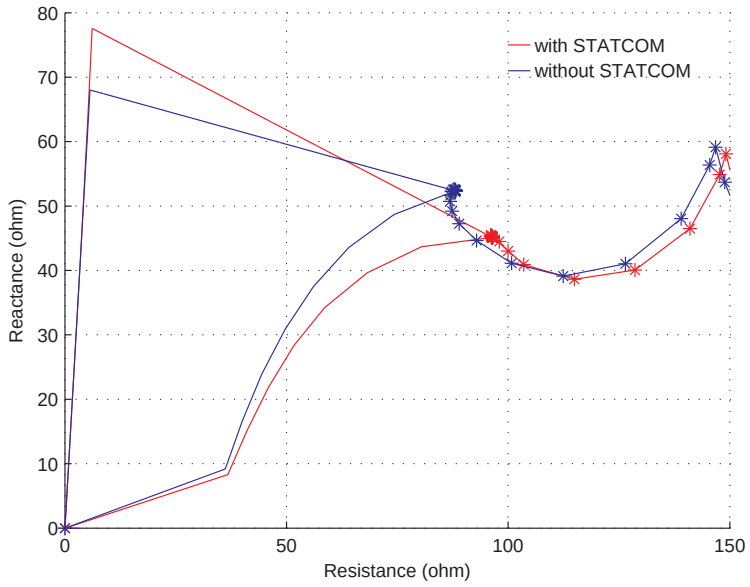


Figure 4.17: Impedance trajectory seen by the relay for zone end AG fault

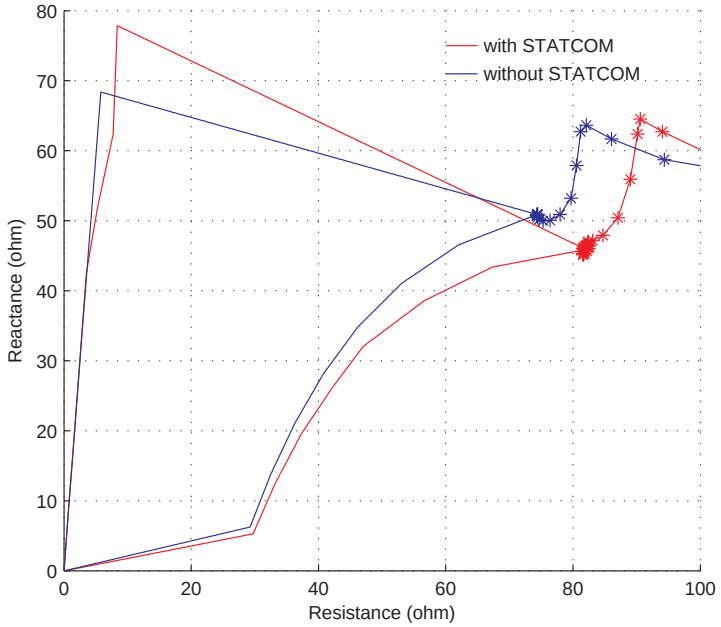


Figure 4.18: Impedance trajectory seen by the relay for zone end BC fault

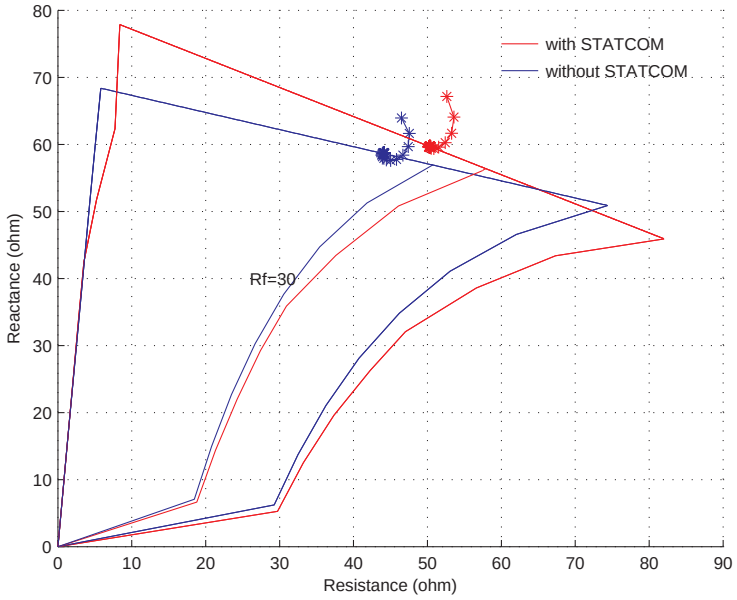


Figure 4.19: Impedance trajectory seen by the relay for zone end BC fault

The elaborate simulations carried out in this chapter prove the efficacy of the adaptive distance relay. The adaptive distance relay, outperformed the conventional relay deployed for the protection of STATCOM connected transmission line. It proved to

exhibit precise reach for all types of fault. After, ensuring the performance of the adaptive relaying scheme, development of a numerical adaptive relay hardware has been put-forth. This becomes essential, in-order to explore the feasibility and functionality of the adaptive relay in real time. Proper real time test results will fortify the simulation results. In the next chapter, development and testing of a fully functional adaptive distance relay hardware, based on a 32-bit floating point digital signal controller (DSC) TMS320F28335, supported with analog to digital converter (ADC) ADS8556 is reported in detail.

CHAPTER 5

DSP BASED ADAPTIVE DISTANCE RELAY HARDWARE DEVELOPMENT and its TESTING USING HIL METHOD

5.1 Introduction

Distance relays are widely used for the protection of transmission lines. They provide an excellent way of obtaining zone discrimination, selectivity, and speed of operation by ensuring precision trip decision up to a certain range of distance (Phadke and Horowitz, 1992; Ravindranath and Chander, 2007; Blackburn and Domin, 2006). The advancements in digital technology have given birth to numerical relays and have gained wide acceptance in power utilities. These relays being programmable use both hardware and software components. The relay hardware mainly consists of signal conditioning circuits (SCC), analog to digital converters (ADC) and digital signal controllers (DSC) modules. The accuracy and operating speed of the relay depends greatly upon these modules. Therefore, the selection of ADC and DSC devices is crucial from the numerical relay design point of view. The following paragraph briefs about the key points for the selection of these devices.

The ADC used in numerical relay applications should have high dynamic input range, in-order to support fault transient signals, while maintaining the measurement accuracy across the entire input range. For an application like distance relay, the phase relationship between the signals sampled from different channels is as important as the value of the signal to measure the impedance accurately. Therefore, a simultaneous sampling bipolar ADC is required in these applications (Gadgil, 2010). The distance relaying algorithms demand considerable computation power, owing to extraction of fundamental frequency phasor of relaying signals and complex impedance computational

procedures. Therefore, a floating-point processor will be preferred over a fixed point processor for achieving higher accuracy, and faster computations. Steady fall in the cost of floating-point DSPs has enabled the protection engineer to fulfill the above requirement. A fully functional distance relay hardware, based on DSC (TMS320F28335) supported with ADC (ADS8556) has been implemented in this work. The specifications of both devices meet the requirements of modern numerical distance relay hardware configuration.

It is standard practice nowadays to integrate relay development and testing. Performance of the newly developed relays are evaluated with the help of relay test benches, prior to actual installation. This process ensures the functionality of the relay, before pressing into real operation. In this work, a Hardware-In-Loop (HIL) test set-up, comprising of the Doble F6150 power system simulator has been configured to test the newly developed adaptive distance relay hardware. This test set-up is capable of generating the real-time relaying signals corresponding to the fault data files obtained through EMTDC/PSCAD simulations.

This chapter presents the design, development and testing of an adaptive distance relay hardware. This encompasses the design of low pass filter, discussion on various sampling techniques, basis for selection of appropriate ADC and DSC, HIL configuration and real time evaluation test results. All the above aspects are detailed in this chapter.

5.2 Numerical Adaptive Distance Relay Hardware Development

The adaptive distance relay hardware has been developed in two phases. In the first phase, a conventional numerical distance relay has been developed and tested using HIL technique. In the second phase, proposed adaptive distance protection scheme has been implemented with minor modifications in hardware and software modules of the

conventional relay. In the present scheme of relay implementation, the conventional input surge protection and signal conditioning circuits are not considered in the hardware as they are standard requirements while deploying relay in the field. The following section presents the conventional relay hardware development.

5.2.1 Conventional Distance Relay Hardware Development

The block diagram of the numerical distance relay hardware is shown in the figure 5.1. It consists of data acquisition system to process six analog channels namely, three phase voltage($V_a, V_b \& V_c$) and three phase current($I_a, I_b \& I_c$) signals. The voltage and current signals are prescaled, before they are applied to the second order analog low pass filter (LPF). The filtered analog signals are simultaneously digitized by ADC (ADS8556), which is suitably interfaced with DSC (TMS320F28335). The DSC, TMS320F28335 generates necessary timing and control signals to acquire the digitized data from the ADC. Acquired data is processed by distance relay logic program deployed on the DSC. The functions of each block is discussed in detail in the following section.

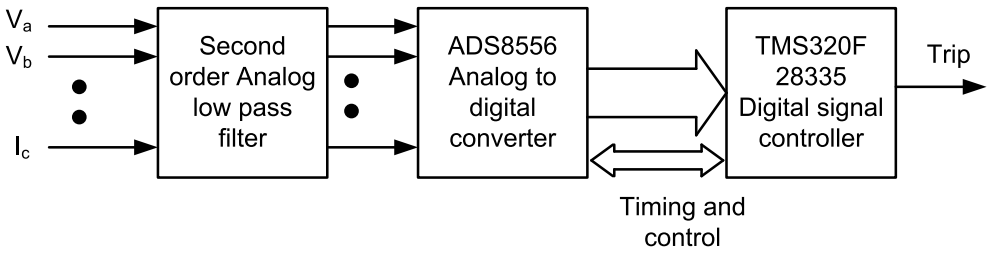


Figure 5.1: Block diagram of conventional distance relay

5.2.2 Analog Low Pass Filter Design

A DSP is designed to process the data in digital format. But most of the real world signals are analog in nature. Therefore, the analog signals have to be sampled in discrete time intervals and converted to digital format by ADC, before they are fed to DSP. A typical phenomenon encountered, when signals are sampled in time, is known

as aliasing. The aliasing pose problems in ADC systems when an input signal contains frequency components above half the ADC sampling rate. This is known as the Nyquist rate. Frequencies above Nyquist appear as false low-frequency aliases. The best approach for eliminating false lower frequencies is to use a low-pass filter, which inhibits aliasing by limiting the bandwidth to below half the sampling rate. Band limiting the input signal eliminates unwanted high frequency components. Therefore, a LPF is regarded as an important element of any data acquisition system (DAS).

In the present work, a LPF based on Sallen-Key topology, has been designed with cut-off frequency equal to 400 Hz. The circuit diagram of the designed filter is as shown in the figure 5.2. It consists of an operational amplifier LM324, which is configured as voltage follower i.e. unity gain mode and produces non-inverting output voltage. The resistors R1,R2 and two capacitors C1,C2 are used to get the desired cut-off frequency.

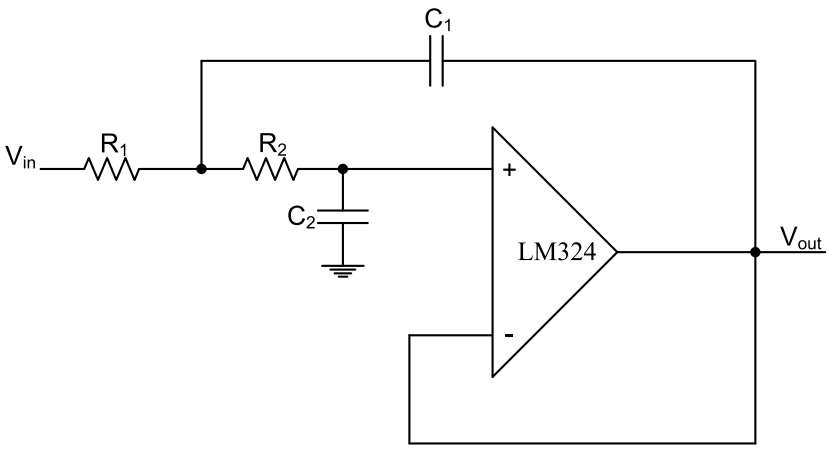


Figure 5.2: Schematic diagram of a second order low pass filter

The filter component values are calculated using the following equations,

$$\omega_c = 2 * pi * f_c = \frac{1}{\sqrt{(R_1 R_2 C_1 C_2)}} \quad {}^{rad}/_{\text{sec}} \tag{5.1}$$

By assuming, $R_1 = R_2$ and $C_2 = \frac{C_1}{2}$

$$\omega_c = 2 * pi * f_c = \frac{1}{\sqrt{\left((R_1)^2 * \frac{(C_1)^2}{2}\right)}} \quad {}^{rad}/_{\text{sec}} \tag{5.2}$$

Let, $R_1 = R_2 = 5.6\ k\Omega$ and $f_c = 400$ Hz, value of C_1 can be found by substituting these values into equation 5.2 as,

$$C_1 = \frac{\sqrt{2}}{2 * pi * f_c * R_1} \quad \mu F \quad = \quad 0.1 \quad \mu F$$

Therefore,

$$C_2 = \frac{C_1}{2} \quad \mu F \quad = \quad 0.05 \quad \mu F \quad \approx \quad 0.047 \quad \mu F$$

The simulated frequency response of the designed filter is as shown in the figure 5.3. From the frequency plot, it may be observed that the actual cut-off frequency achieved is around 465 Hz. This is attributed to the discrepancy in the actual values of designed components. Hence the minimum sampling frequency required will be 930Hz.

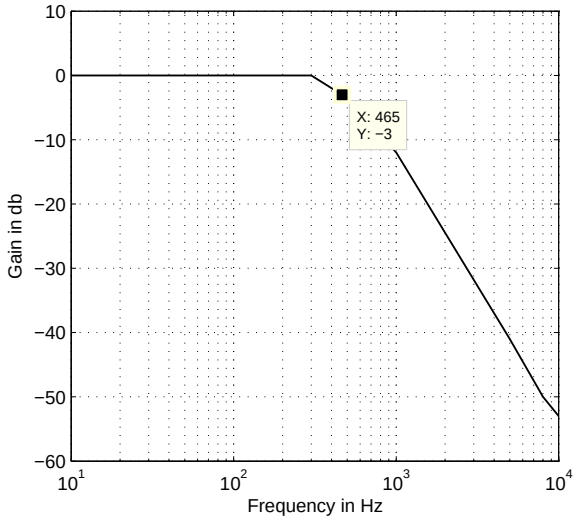


Figure 5.3: Frequency response of designed second order LPF

The LPF circuit shown in the figure 5.2 has been implemented on a printed circuit

board (PCB), after verifying the performance through simulations. Figure 5.4, is the screen shot taken from the Agilent mixed signal oscilloscope. It shows delay caused by the LPF for a 50 Hz ac input signal. It can be seen from the figure that delay of 307.6 μseconds has been introduced between input and output signals.

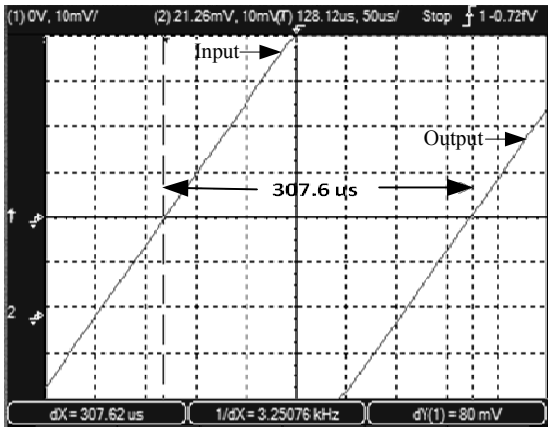


Figure 5.4: Delay caused by the low pass filter

The analog relaying signals are passed through the LPF before being applied to ADC input channel. The following section presents the details of ADC used in this work.

5.2.3 Analog to Digital Converter

An ADC is a device that converts input analog signals to a digital number proportional to the magnitude of the input. It is a vital part of any data acquisition system. The DAS are broadly classified into three types based on the sampling and conversion methods as mentioned below,

1. Non simultaneous sampling
2. Simultaneous sampling and sequential conversion
3. Simultaneous sampling and simultaneous conversion

Each of these sampling methods will be described briefly in the following sections.

5.2.3.1 Non simultaneous sampling

Figure 5.5 shows the block diagram of n-channel non simultaneous sampling DAS.

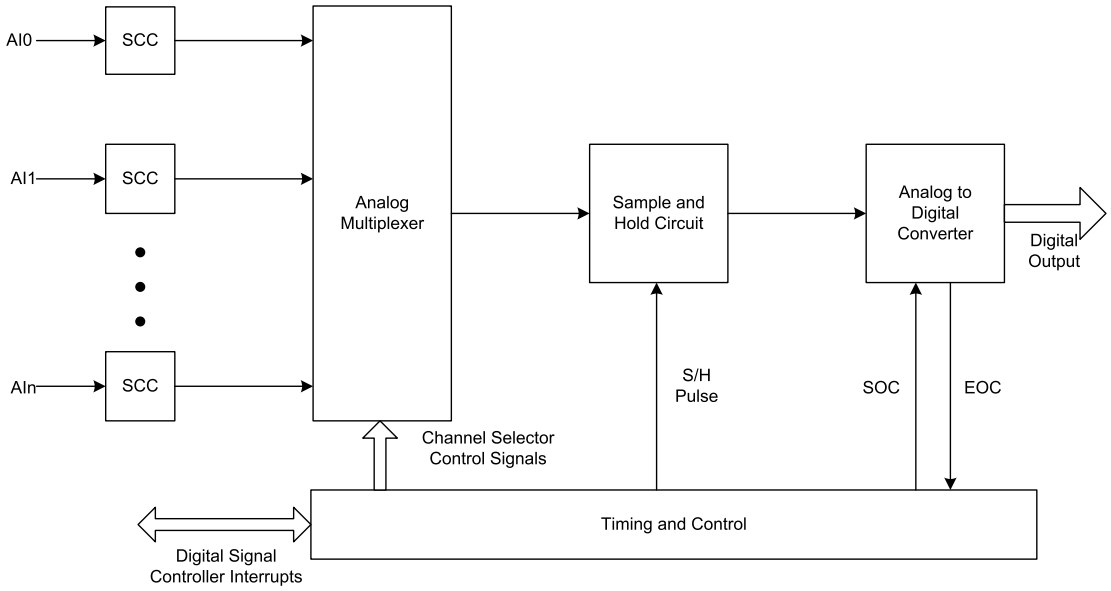


Figure 5.5: Block diagram of non simultaneous sampling

It consists of signal conditioning circuits (SCC) comprising of an amplifier, LPF whose function and design has been discussed in the previous section. An analog multiplexer (mux) is a device that selects one of several analog input signals and forwards the selected input into a single line output. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to switch to the output. Thus, a multiplexer makes it possible for several channels to share a common resource. For example, all the analog input channels, AIO - AIn can share a single sample and hold (S/H) circuit and ADC as shown in the figure 5.5. The S/H circuit, is used to sample a continuously varying analog signal at predetermined sampling intervals and holds its value at a constant level for a minimum period, which is equal to the conversion time of ADC. This is necessary to ensure accurate results from the ADC. In this type of DAS, at any sampling instant one signal is selected after completion of conversion of the previous channel. It means that the channels are converted sequentially one at a time. Figure 5.6 illustrate the consequences of non simultaneous sampling in a two channel data acquisition sys-

tem. It can be seen from the figure that the sampling instants for the channel-1 is t_1 and channel-2 is t_1'. They differ by a finite time interval, known as the channel conversion time, which is the total sum of multiplexer settling time, S/H acquisition time and ADC conversion time. In this DAS example, channel-1 is voltage and the second channel is current, then the impedance calculated from the sampled data will have a phase angle error of $\omega(t_1' - t_1)$ radians. This will affect the operation of the impedance relays and hence such type of ADCs are not suitable for distance relay applications.

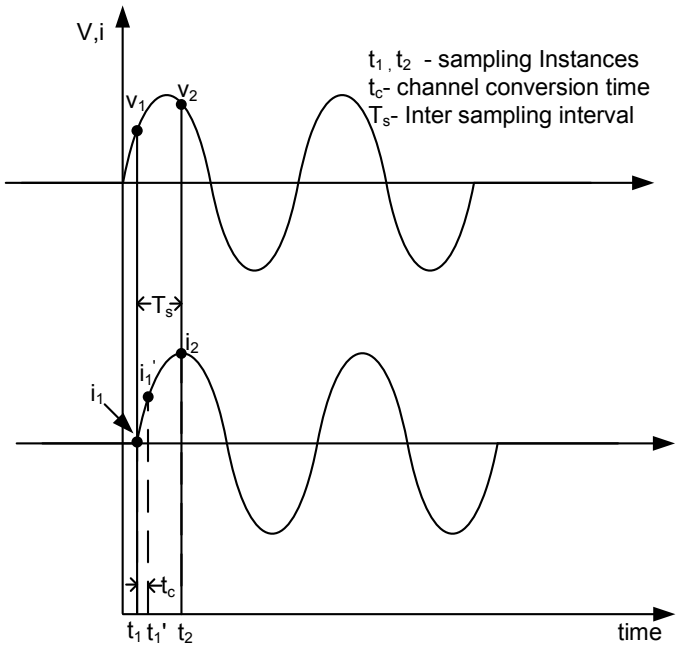


Figure 5.6: Effect of non simultaneous sampling

5.2.3.2 Simultaneous sampling and sequential conversion

The demerits of the non simultaneous DAS can be overcome by simultaneous sampling technique shown in the figure 5.7. In this type of DAS, all the analog input channels are sampled at a same sampling instant, by simultaneously issuing the S/H pulse to all the S/H circuits. An analog multiplexer will switch the channels to the ADC one at a time as determined by the channel selector logic. The benefits obtained are,

1. No time lag introduced between channels.
2. Total conversion time of all channels is reduced by (n-1)x (S/H acquisition time) for n channel system .

This type of DAS is more expensive owing to increase in the number of S/H circuits.

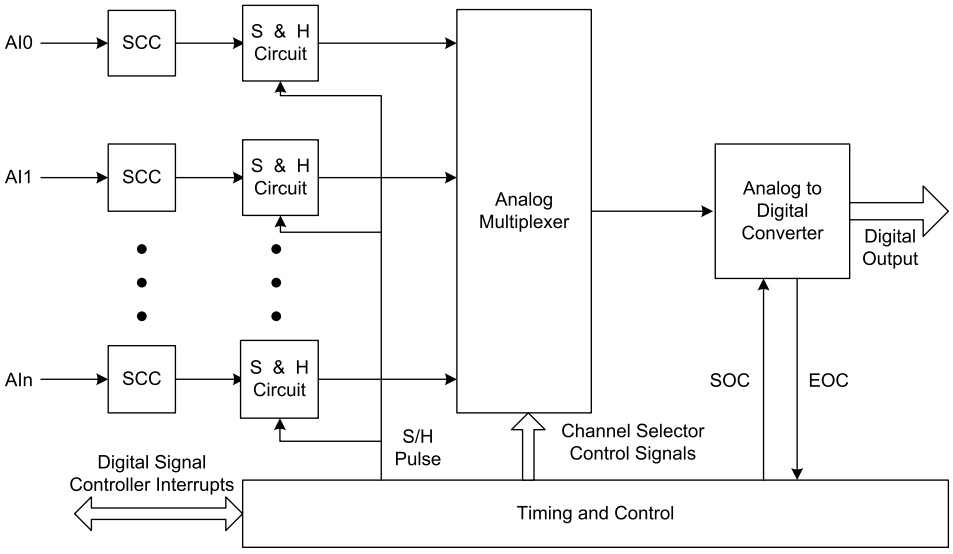


Figure 5.7: Block diagram of simultaneous sampling and sequential converter DAS

5.2.3.3 Simultaneous sampling and simultaneous conversion

In case of systems, where the phase information of the various input channels are required, simultaneous sampling with simultaneous conversion is preferred along with faster ADCs. In such configuration each channel has a dedicated S/H followed by an ADC as shown in the figure 5.8. Simultaneous sampling ADCs perform the task using multiple S/H circuit to sample the input channels at the same instant, then perform the simultaneous conversion on all channels. End of conversion signal will be used as a flag, to indicate the end of conversion, it will be set; once all the channels are converted and the data is ready for further processing.

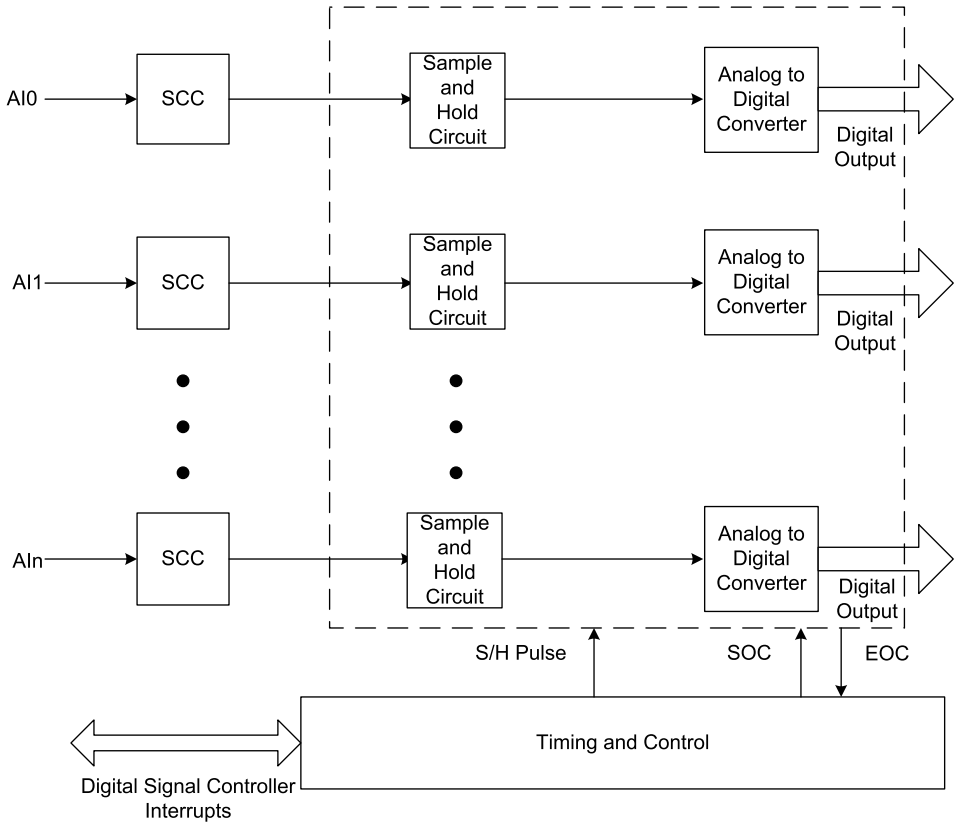


Figure 5.8: Block diagram of simultaneous sampling and simultaneous conversion DAS

The present research work demands accurate measurement of system impedance using the sampled three-phase voltage and current signals. It can be inferred from the above discussion that for this application, simultaneous sampling and conversion type of ADC is the preferred choice. It ensures accuracy in the measured impedance, by preserving the phase information of the sampled signals. Therefore, a six channels, 16-bit simultaneous sampling ADC, ADS8556 from Texas Instruments which suits best for this application has been selected.

The salient features of the ADS8556 are listed below(SLAU298, 2010; SBAS404B, 2012) .

- 16-Bit Successive Approximation Register (SAR) type analog to digital converter.
- Six SAR ADCs grouped in three pairs.
- Maximum data rate per channel with internal conversion clock and reference is

630 ksps.

- Maximum data rate with external conversion clock and reference is 800 ksps.
- Programmable input voltage ranges: Up to $\pm$12V
- Programmable and buffered internal reference: 0.5V to 2.5V.
- Selectable parallel or serial interface.
- Operating temperature range: -40°C to +125°C.
- Excellent signal-to-noise performance:91.5dB

The configuration of the ADC is presented in the next section.

5.2.3.4 ADS8556 configuration

In-order to save design time, a readily available ADS8556/7/8 evaluation module (EVM) has been used in this work. The figure 5.9 show the ADS8556 EVM prepared for testing. It can be programmed using hardware/software methods. It also has an option to transfer converted data in either serial/parallel mode. In this work, parallel data transfer mode has been selected, as it is easier and faster. The configuration of ADS8556 is described briefly in the following section.

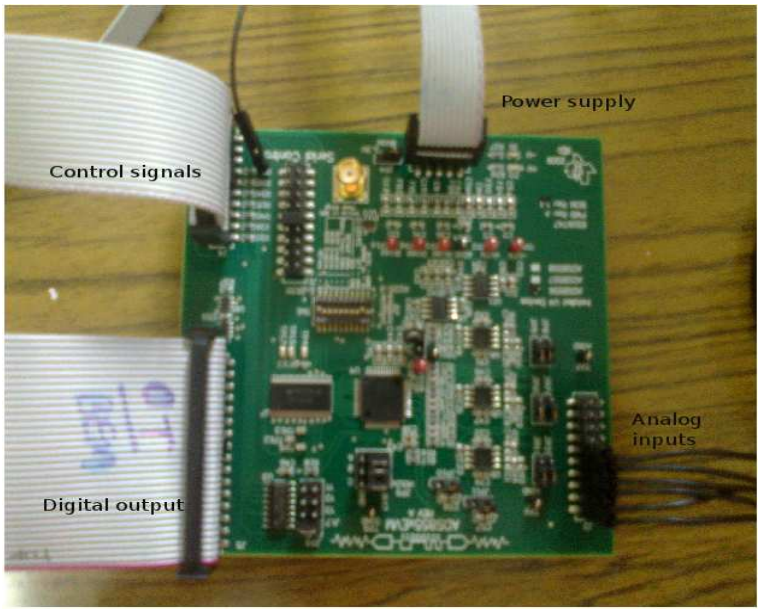


Figure 5.9: Photograph of the ADS8556 EVM

The functional schematic, of the ADS8556 is shown in the figure 5.10 (SBAS404B, 2012).

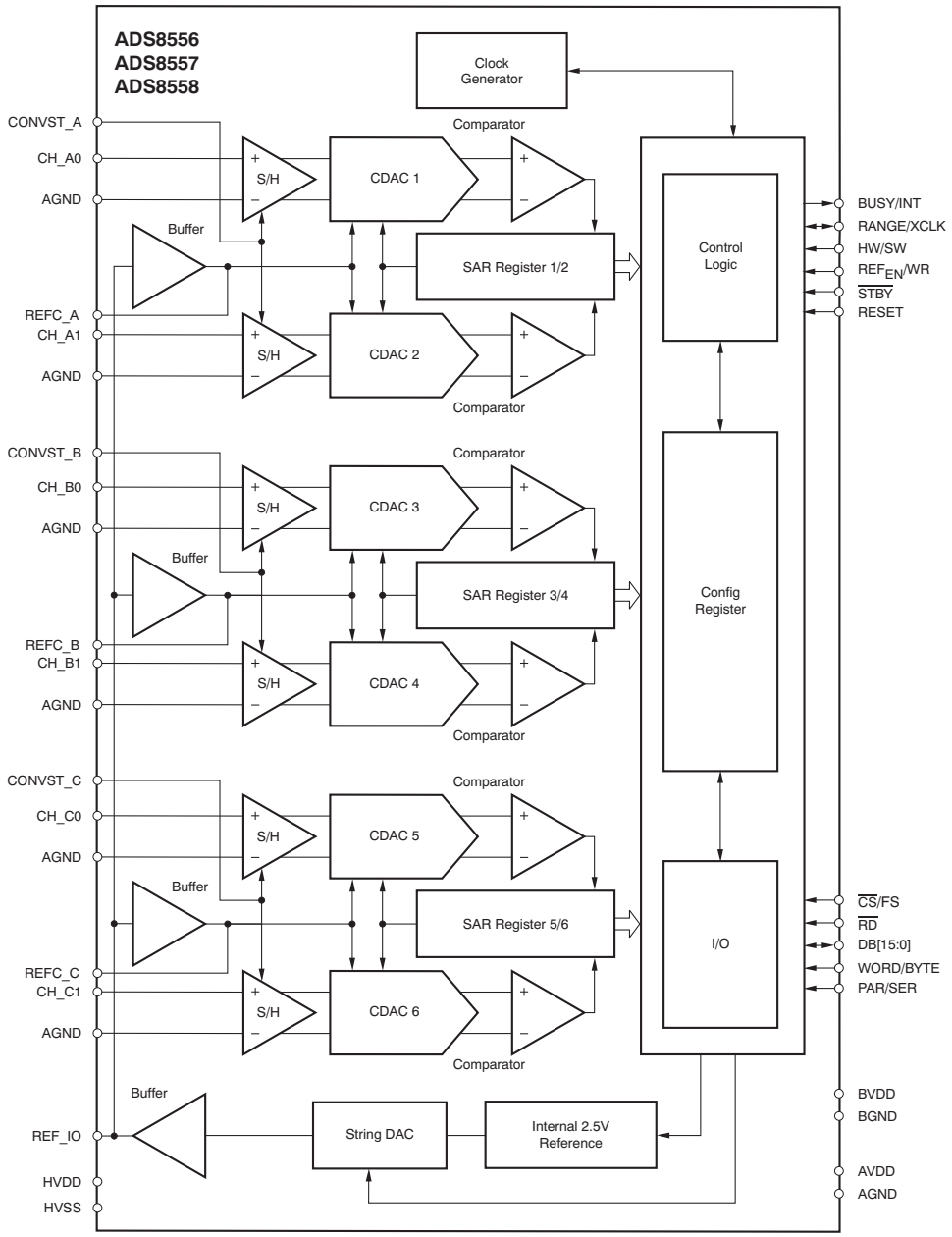


Figure 5.10: Functional block diagram of ADS8556 (SBAS404B, 2012)

The ADS8556 include six 16-bit ADCs respectively that operate based on the SAR principle. The six S/H circuits are divided into three pairs (A, B and C). Each pair of channels has a hold signal (CONVST_A, CONVST_B, and CONVST_C) which, when

strobed together, allows simultaneous sampling and conversion on all 6 analog inputs, preserving the relative phase information of the signals.

The control logic block offers host of features, which allow the user to configure the ADC as per application requirement. The settings done in this work is presented sequentially as follows,

- First, Standby mode input pin $\overline{STBY}$, is set to high so as to enable the device.
- This ADC can be controlled in hardware (HW)/software (SW) mode through mode selection input (HW/SW). In this work HW mode is enabled by connecting HW/SW to ground and ADC works according to the setting of external pins.
- The ADS8556 has an internal programmable 2.5 V reference source (VREF), which is enabled by setting REFen pin to high.
- This device accept single-ended, bipolar analog input signals in the selectable ranges of $\pm$ 4VREF or $\pm$2VREF with an absolute value of up to $\pm$ 12V. RANGE input pin is set to low in-order to select input voltage range as $\pm$ 4VREF. This sets the effective input voltage range of $\pm$ 10V.

The data transfer process can be configured using the I/O module shown in the figure 5.10. The configuration used in this work is given below.

- Parallel data interface mode is selected by setting pin PAR/SER to low .
- $\overline{RD}$ is set low to enable parallel data output.
- WORD/BYTE pin is set to low in-order to transfer the data in word mode using DB[15:0].

The details pertaining to parallel interface of ADS8556 is furnished in Appendix B

The section that follow, discusses the application of DSP with reference to power system relaying.

5.2.4 Application of DSP for Power System Relaying

The numerical relays use a programming device for implementing the protective relaying algorithms. These relaying algorithms have to operate in real time, in-order to facilitate rapid removal of a disturbance from a power system. The digital processing of signals in real time requires a highly sophisticated processors. Earlier microprocessors

were used to implement the relaying algorithms. But the microprocessors have low chip operating frequency, limited processing capacity, and memory allocation. The lack of these features, have put stiff constraints on the size of the program and few functions are compromised to operate in real time. Therefore, a specialized hardware such as DSP is preferred over microprocessors and microcontrollers. DSP is optimized to efficiently process the signal processing algorithms and output the data in real time (Inacio and Ombres, 1996; Smith *et al.*, 1997). Because of these advantages recent numerical relays employ DSPs instead of microprocessors as a programming platform (Goh *et al.*, 2011).

Major task of the relaying algorithm is to compute complex relaying quantities. These computations can be performed by using either a fixed point or floating point processors. Fixed point processors represent and manipulate numbers as integers. Therefore they use additional software routines, that emulate the behavior of a floating point device to perform floating point operations. However, such routines add considerable delay in the computation of relaying quantities in real time. Consequently, from the relay application view point floating point emulation is rarely used. Whereas, a floating point processor can perform high speed floating point arithmetic operations and provides wider dynamic range and high precision (Johns and Salman, 1997). Therefore, a floating point processor is preferred over a fixed point processor, for achieving higher accuracy and faster computations in applications such as, distance relays for power system protection. The recently released TMS320F28335 32-bit floating point digital signal processor by Texas instrument has been selected for implementing the distance relay in this work. The key features (SPRS439L, 2012; Peng, 2011) of this DSP are mentioned below,

- 6.67 ns instruction cycle time at 150 MHz
- Low power 3.3 volts design
- 256 Kw of on chip flash memory
- 32Kw of internal RAM memory
- IEEE-754 single-precision floating-point unit (FPU)
- 16 x 16 Dual MAC
- Harvard bus architecture

- Code efficient (in C/C++ and Assembly)
- Real time debug capability
- Three 32-bit timers
- Communications peripherals
- 88 multiplexed GPIO with 3.3 volts output
- 16 Channel 12-bit ADC

It can be seen from the key features list that, this DSC comes with an on board inbuilt ADC. But, unfortunately the features of this ADC could not satisfy the present relay hardware requirements. The reasons for the same are mentioned below;

- Even though on board ADC has 16 channels, only two channels can be sampled simultaneously.
- It is unipolar type ADC, with analog input range of 0 - 3.3 V
- Its input range is not sufficient enough to accommodate dynamic range of signals exhibited by power system during abnormal conditions.

For the reasons cited above, an external ADC (ADS8556) has been selected, whose merits have been already discussed in the section 5.2.3. This section has presented the details on the hardware components of the distance relay separately. The following section illustrates the overall distance relay hardware configuration.

5.2.5 Relay Hardware Configuration

The figure 5.11 shows the functional block diagram of relay hardware configured in the present work. It consists of LPF with cut-off frequency of 400 Hz, which band limits the analog signals. These are digitized by the ADS8556 and transferred to DSC28335 memory, which is further processed by the relaying algorithm.

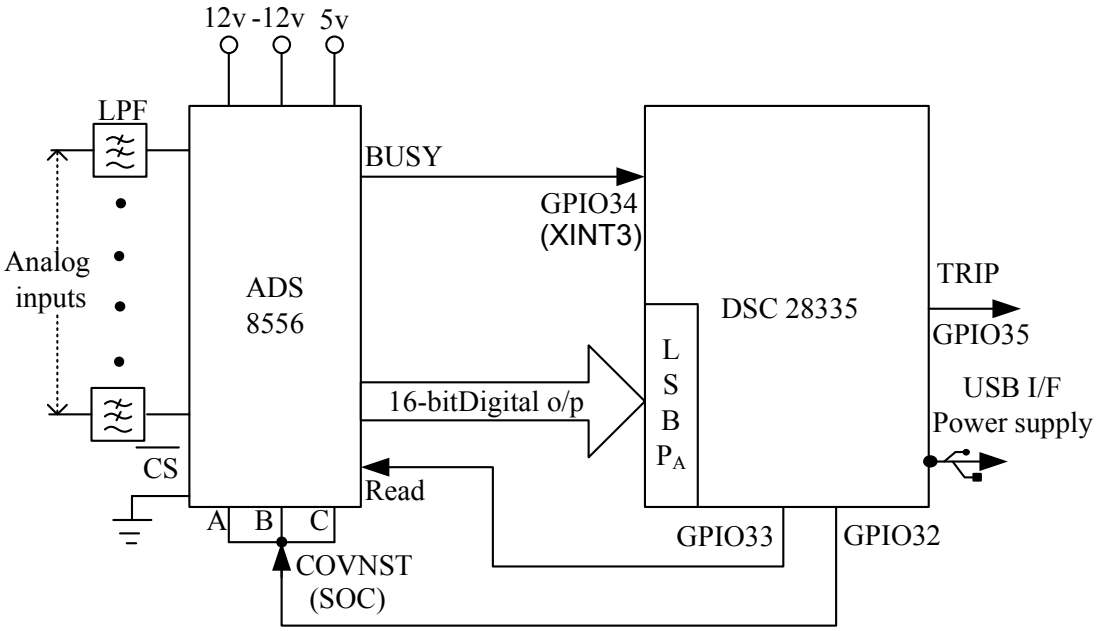


Figure 5.11: Functional block diagram of relay configuration

The process of generation, timing of the S/H pulses, and acquisition of data samples are managed by two interrupt routines. They are,

- Software timer interrupt service routine.
- ADC interrupt service routine.

Each of these above routines are explained in the subsequent sections.

5.2.5.1 Software timer interrupt service routine

This routine, times the sample and hold pulse making use of one of the on-chip software timer (Cputimer-0) of the DSC 28335 and a General Purpose I/O pin GPIO32. The Cputimer-0 has been configured to generate interrupt every 312.5 μseconds interval as shown in the figure 5.12 (a). In the ISR, GPIO32 is toggled at the occurrence of each interrupt to generate the SOC signal as shown in the figure 5.12 (b). It can be verified from the figure that the period of signal is 625 μseconds (1600 Hz). Also it can be seen that the SOC is held high for 312.5 μseconds, which is sufficient to complete signal conversion and data transfer process. With this sampling frequency 32 samples/cycle

of a fundamental 50 Hz signal can be obtained.

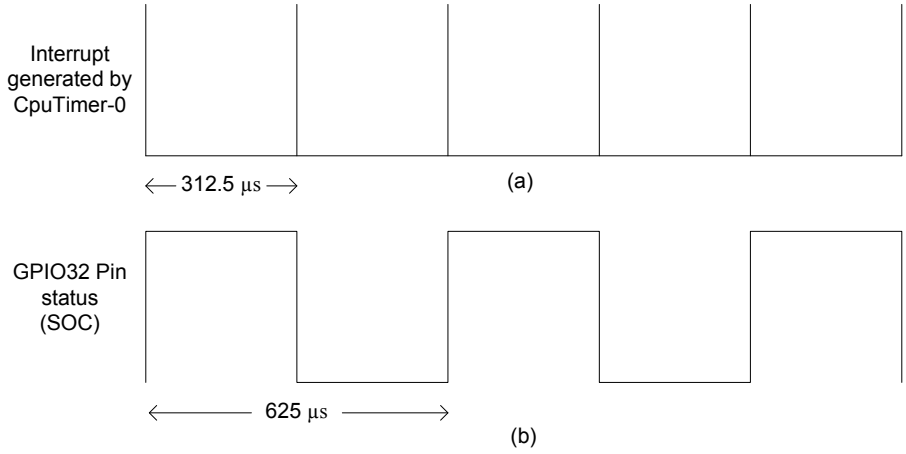


Figure 5.12: Generation of SOC signal

The SOC signal is applied to CONVST_A, CONVST_B and CONVST_C of the ADC pairs A, B and C respectively as shown in the figure 5.11. By applying a LOW to HIGH pulse for all these pins, all the analog input signals are simultaneously sampled and converted simultaneously. During the conversion period, BUSY signal will remain high and it becomes low, after conversion is finished. The data transfer process is accomplished by ADC interrupt service routine (ADC ISR). The configuration and functions of this ISR is described in the following section.

5.2.5.2 ADC interrupt service routine

The ADS8556 require toggling signal on ($\overline{RD}$) pin to facilitate data reading. This signal has to toggle high to low for reading data from each channel. The function of this ISR is to generate $\overline{RD}$ signal, such that all six analog channels are read and stored sequentially in the DSC memory. This ISR is awakened by the falling edge of the BUSY signal. The external interrupt, XINT3 resource available in the DSC28335 has been utilized for this purpose. It is configured to detect the falling edge of the signal by setting 'falling edge active' option available in the external interrupt configuration register (XIntruptRegs). The GPIO34 pin has been assigned as external interrupt XINT3 as shown in the figure

5.11. The sequential steps involved in $\overline{RD}$ signal generation and data transfer process is explained with the help of flow chart shown in the figure 5.13.

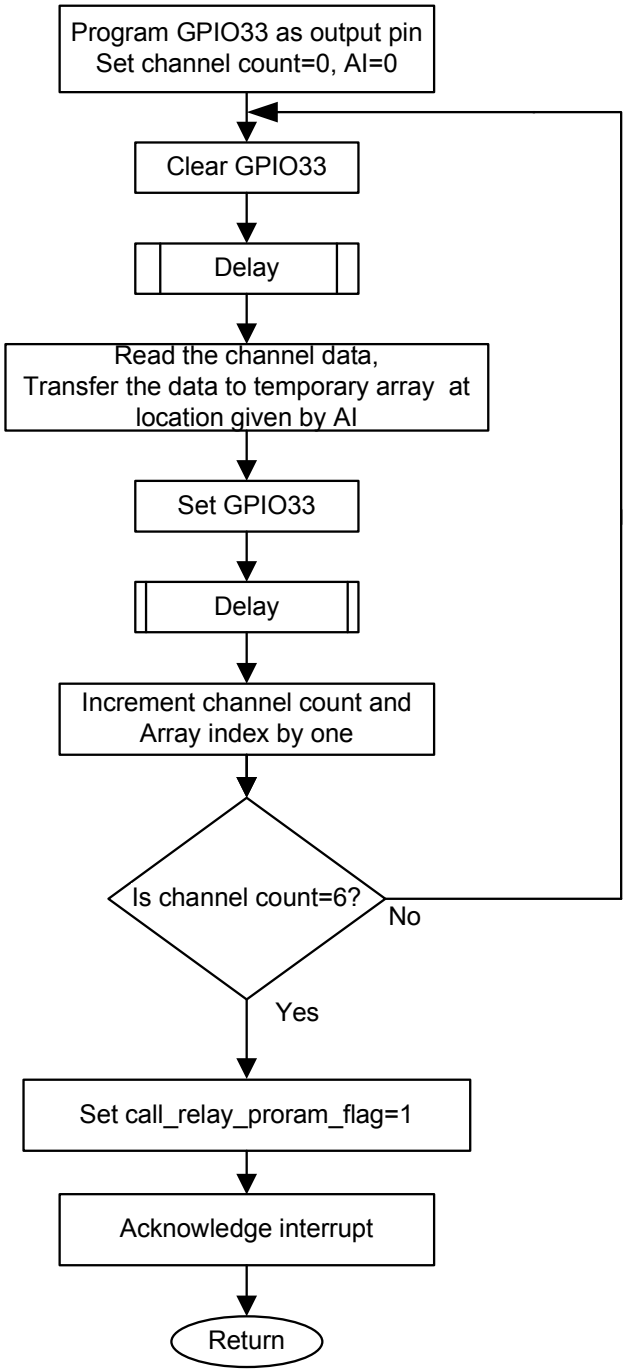


Figure 5.13: ADC ISR flow chart

Step 1 : The multiplexed GPIO33 pin is programmed as output pin and set to high. The channel count is set to 0. Each channel has been alloted specific address in data array with 6 memory locations to store all the six channels data corresponding to the current sampling instant. The data array index (AI) is initialized to zero.

Step 2 : Clear GPIO33.

Step 3 : GPIO33 is held at low state for 1 μsecond by calling delay subroutine. Thus the $\overline{RD}$ signal for the first channel is generated.

Step 4 : Read the present channel data and store it into the respective location given by AI.

Step 5 : After reading a channel GPIO33 pin is set and it is held for 1μsecond by calling delay subroutine, to facilitate generation of $\overline{RD}$ for reading next channel.

Step 6 : Increment the channel count and AI by one to indicate that a channel data has been acquired.

Step 7 : Compare channel count value with number of analog channels, which is six in this case. If present channel is not the last channel, goto step 2, to generate $\overline{RD}$ for reading next channel. If channel count is equal to six, then goto step 8.

Step 8 : Set call_relay_ proram_flag=1, which will be used as flag to call the distance relay program in the main program.

Step 9 : Acknowledge the interrupt and return to main.

The functioning of both software timer interrupt service routine and ADC interrupt service routine has been verified before implementing distance relay software. A 50 Hz sinusoidal signal from a signal generator has been applied to all analog channels of ADS8556. The control signals of ADC captured on mixed signal oscilloscope is as shown in figure 5.14. The first trace is SOC signal of frequency 1600 Hz (32 samples/cycle), which is used to initiate simultaneous sampling of all six channels. The

second trace is BUSY (EOC) signal issued by ADS8556 to indicate that the conversion over and data is ready for reading. The time taken by ADC to convert all six channels was 1.17 μseconds can be seen from the figure. The read pulses, generated to read all six channels digitized data is shown by the third trace.

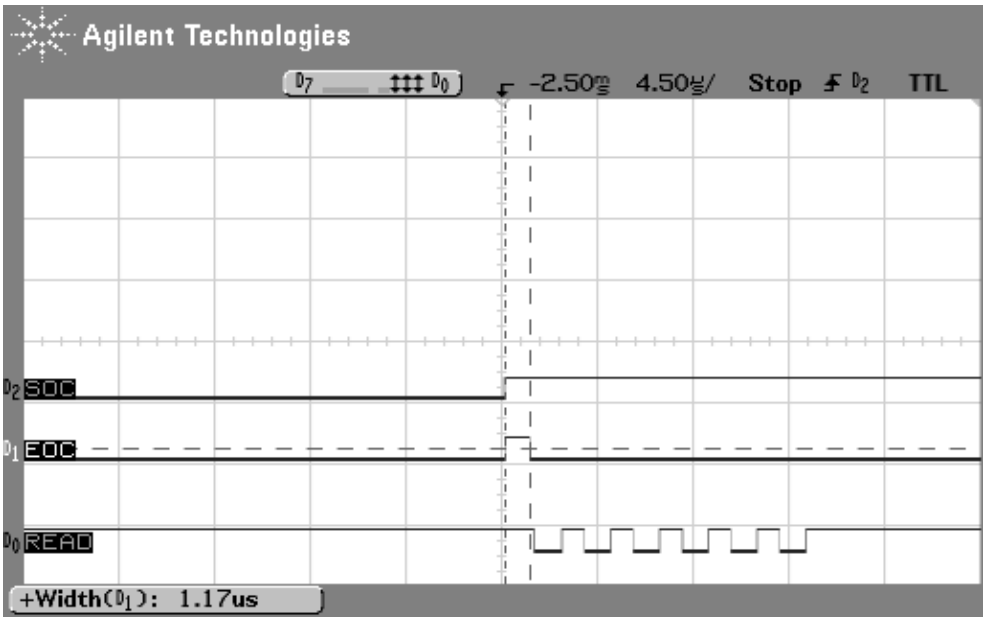


Figure 5.14: Control signals of ADS8556 captured on oscilloscope

The figure 5.15 shows the control signals recorded on a mixed signal oscilloscope while sampling a 50Hz fundamental sine at a sampling frequency of 800Hz, for illustration purpose. It can be seen that the SOC has been issued at an interval of 1.25 milliseconds so as to obtain 16 samples/cycle. Also, the digitized output of the ADS8556 over its entire operating range has been tested and tabulated in the table 5.1. Thus, the choice of ADS8556 for distance relay application has been verified in respect of the sampling frequency and the full analog input voltage range.

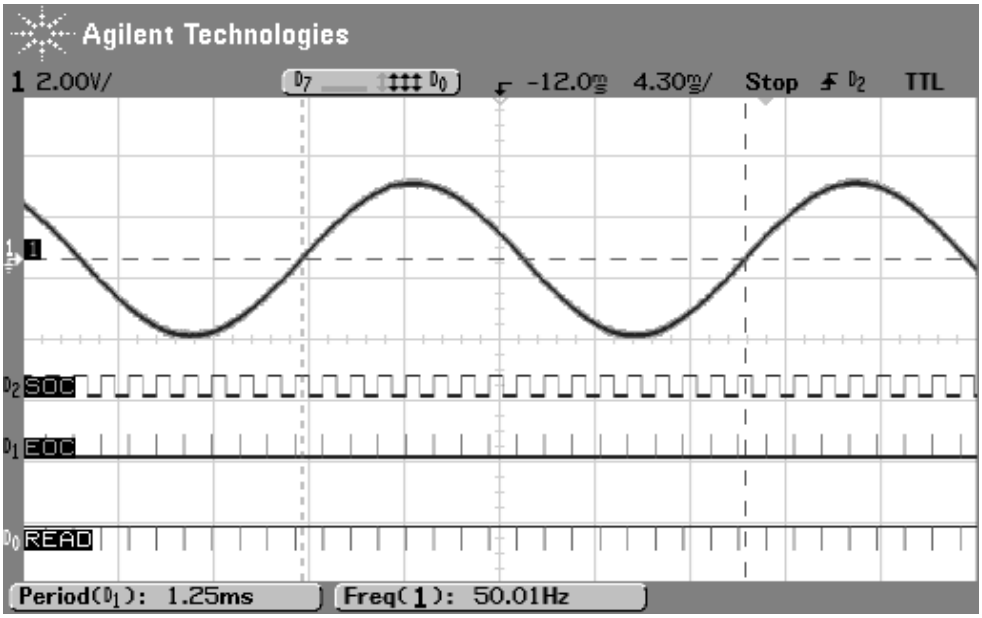


Figure 5.15: Control signals to sample a 50Hz sine wave at a sampling frequency of 800Hz

Table 5.1: Digitized output of the ADS8556

Input voltage (V)	output code (Hex)
10	7FFF
5	3FFF
0+	0
0-	FFFF
-5	C000
-10	8000

The section that follow presents the development of distance relay program.

5.3 Development of Distance Relay Program

This section describes the development of non switched mode distance relay using the sampled voltage and current signals. A non-switched mode of distance relaying scheme contains independent ground fault relay for each phase and phase fault relay for each phase pair. Such technique in sampled data distance relaying scheme can be realized by selecting each phase to ground fault relay logic program in sequence under ground fault relay logic subprogram. Similarly, phase to phase fault relay logic program for each phase pair will be in sequence in case of phase fault relay logic subprogram (K.P.Vittal, 1999). The relay program is called after execution of ADC interrupt service routine at every sampling instant. The complete software sequence of the relay for this mode of operation is shown in figure 5.16 and the sequential procedural steps are given below :

Step 1: Once the relay software routine is called, latest samples of all relaying signals are stored in a temporary array.

Step 2: Compute the real and imaginary component of all relaying signals using recursive FCWF. The FCWF window Fourier algorithm is used in recursive mode(RFCWF) for saving computation time. It reduces computation from 2N multiply add operation in normal discrete Fourier Transform (DFT) to 4 additions and 2 multiplications per update. The mechanism of RFCWF is explained in Appendix-C. The RFCWF is implemented by using stored samples in data table and temporary array. The size of the data table used is 32 X 6, in-order to store 32 samples of all six channels. The elements of data tables are accessed by a Data Table Pointer(DTP). The DTP is comprised of two index variables 'r' and 'c' corresponding to rows and columns. In the beginning of program all elements of data table and DTP are initialized zero. The structure of the data table is shown below,

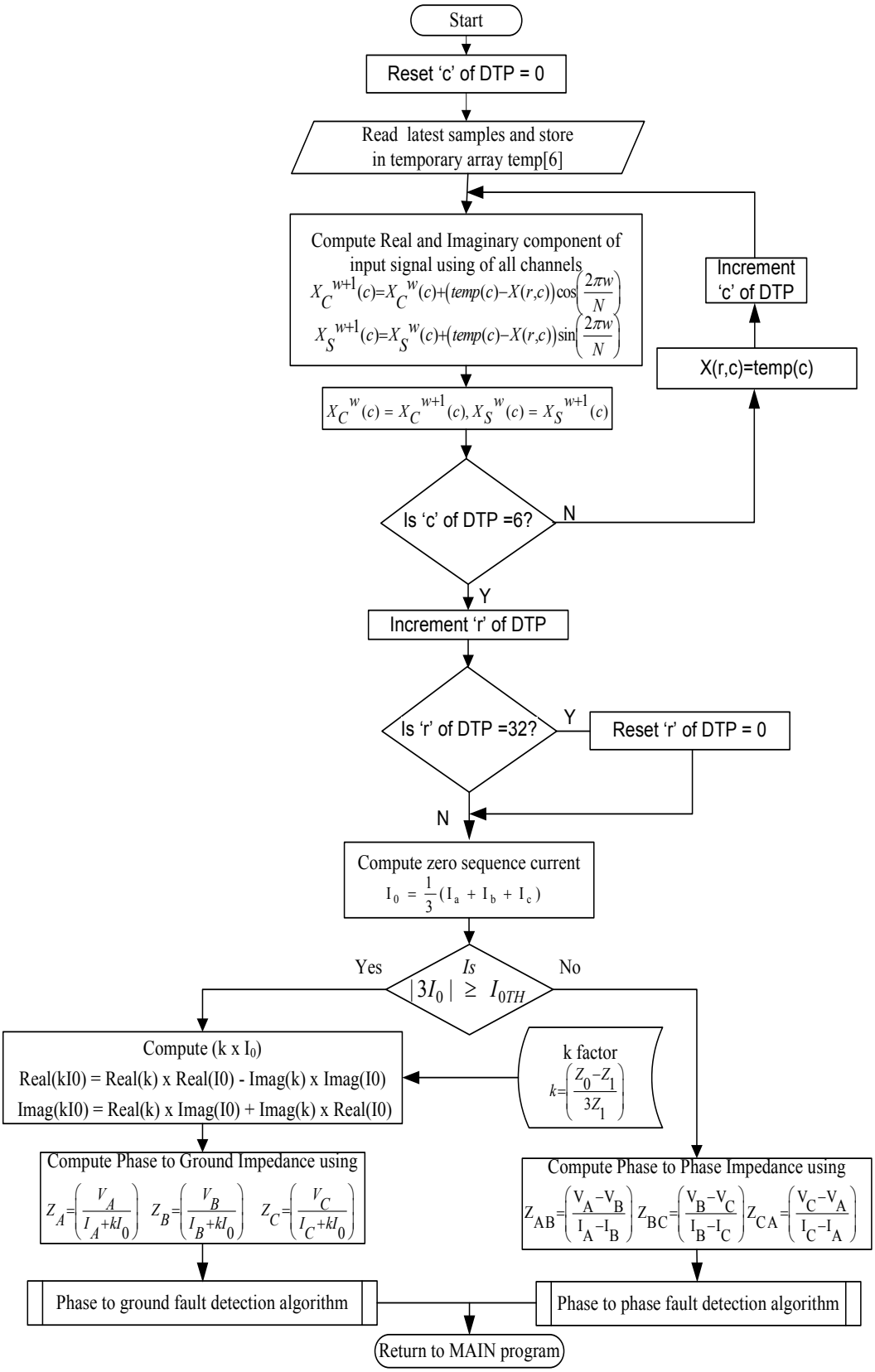


Figure 5.16: Flowchart of relay program

$$X[r,c] = \begin{bmatrix} V_{a(w)} & V_{b(w)} & V_{c(w)} & I_{a(w)} & I_{b(w)} & I_{c(w)} \\ V_{a(w+1)} & V_{b(w+1)} & V_{c(w+1)} & I_{a(w+1)} & I_{b(w+1)} & I_{c(w+1)} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ V_{a(w+N-1)} & V_{b(w+N-1)} & V_{c(w+N-1)} & I_{a(w+N-1)} & I_{b(w+N-1)} & I_{c(w+N-1)} \end{bmatrix}$$

In data table each of the phase voltages and phase currents have been assigned a separate column. The data table elements $V_{a(w)}$ and $V_{a(w+N-1)}$ denote oldest and latest samples of phase-A voltage obtained at W^{th} window respectively. Similarly, $V_{a(w+1)}$ forms oldest sample of phase-A voltage obtained at $(W+1)^{th}$ window and so on. The following equations are used to compute fundamental real and imaginary components of any given signal X at $(W+1)^{th}$ window,

$$X_C^{w+1} = X_C^w + (x_{w+N} - x_w)\cos\left(\frac{2\pi w}{N}\right) \tag{5.3}$$

$$X_S^{w+1} = X_S^w + (x_{w+N} - x_w)\sin\left(\frac{2\pi w}{N}\right) \tag{5.4}$$

Where,

N=Number of samples per cycle.

W= W^{th} window

X_C^W and X_S^W = fundamental cosine and sine components at the previous window respectively. Both X_C and X_S have been initialized to zero in main program before calling relay subroutine for the first time.

x_{w+N} and x_w = sampled data obtained at $(W+1)^{th}$ and W^{th} sampling instants respectively.

It can be seen from the equations 5.3 and 5.4 that for computation of X_C^{w+1} and X_S^{w+1} oldest sample in data table x_w and most recent sample x_{w+N} held in temporary

array are required. The above equations can be generalized to compute X_C^{w+1} and X_S^{w+1} pertaining to c^{th} column of r^{th} row in the data table X as shown in the equations 5.5 and 5.6.

$$X_C^{W+1}(c) = X_C^W(c) + (temp(c) - X(r,c)cos\left(\frac{2\pi W}{N}\right) \tag{5.5}$$

$$X_S^{W+1}(c) = X_S^W(c) + (temp(c) - X(r,c)sin\left(\frac{2\pi W}{N}\right) \tag{5.6}$$

Replace X_C^W(c) by X_C^{W+1}(c) and X_S^W(c) by X_S^{W+1}(c)

Step 3: Compare value of 'c' with 6; if the condition is false, then replace X(r,c) with temp(c) and increment column index 'c' to compute sine and cosine components of next signal i,e., goto step 2.

This condition returns true if cosine and sine components of all channels have been completed, then increment 'r' of DTP in-order to move to next sampling instant, continue.

Step 4: Compare value of 'r' with 32; if the condition is true, then reset 'r'=0. In this way data size of data table is always limited to 32 X 6 filled with most recent data samples. Goto step 5.

Else, continue.

Step 5 : Compute the zero sequence component of the three phase currents (I_0), which is used to discriminate between ground faults and phase faults as explained in the section 4.2.1 of chapter 4.

Step 6 : Compute 'K' factor.

Step 7 : Compute ground and phase impedances.

Step 8 : Call the fault detector algorithm. The fault detection algorithms explained in chapter 4 section 4.2.1.1 have been implemented on the DSC.

Step 9 : Return to main program.

This section presented the development of distance relay program on DSC28335. The following section provides details of complete flow sequence of relay software.

5.4 Complete Flow Sequence of Relay Software

The software for distance relay has been developed in embedded C language targeted for DSC TMS320F28335. The Code Composer Studio4 (CCS4) is used as development platform, provides easy debugging, and real time refreshing options (C2000, 2010). The complete software flow chart of distance relay is shown in figure 5.17. The software flow sequence is given below.

Step 1 : The relay program starts with initialization process. The objective of initialization process is to orient all variables and various resources of DSC involved in relay implementation to an initial state. The following tasks are carried out in initialization phase,

- DSC has an on board 30 MHz crystal for clock input. The operating frequency of DSC is by programming the PLL control register (PLLCR). The PLLCR has been loaded with 0xA for a 150Mhz CPU clock.
- Initialize a data table of size 32 X 6 locations to store 32 samples of all six channels. Initialize DTP to (0,0) so as to start storing the data from first location of the data table.
- Initialize arrays X_C and X_S and temp to zero.
- Initialize trip counter to zero
- Initialize relay settings item Initialize call_relay_proram_flag to zero.
- The DSC28335 has 96 multiplexed I/O pins(GPIO0 - GPIO95), organized in three 32 bit ports, namely, Port A (GPIO0-GPIO31), port B (GPIO32-GPIO63), and port C(GPIO64-95). This work is carried out using TMDSDOCK28335 - TMS320F28335 Experimenter Kit which allows access to multiplexed 88 I/O pins(GPIO0 - GPIO87). Each pin can be assigned up-to 4 different functions depending upon the user requirements. The functionality can be selected by using GPIO multiplexing (MUX) registers . When selected for digital I/O mode, GPxDIR registers registers provided option to configure the pin direction. In this

work all multiplexed I/O pins are configured as GPIOs, which can be set by writing 0 to all MUX registers. All 32 GPIO pins of port A are programmed as input pins to read the data from ADS8556. At present only lower 16 pins are used. The GPIO32, GPIO33 and GPIO35 are programmed as output to generate SOC, $\overline{RD}$ and trip signals respectively. GPIO34 is assigned to external interrupt(XINT3).

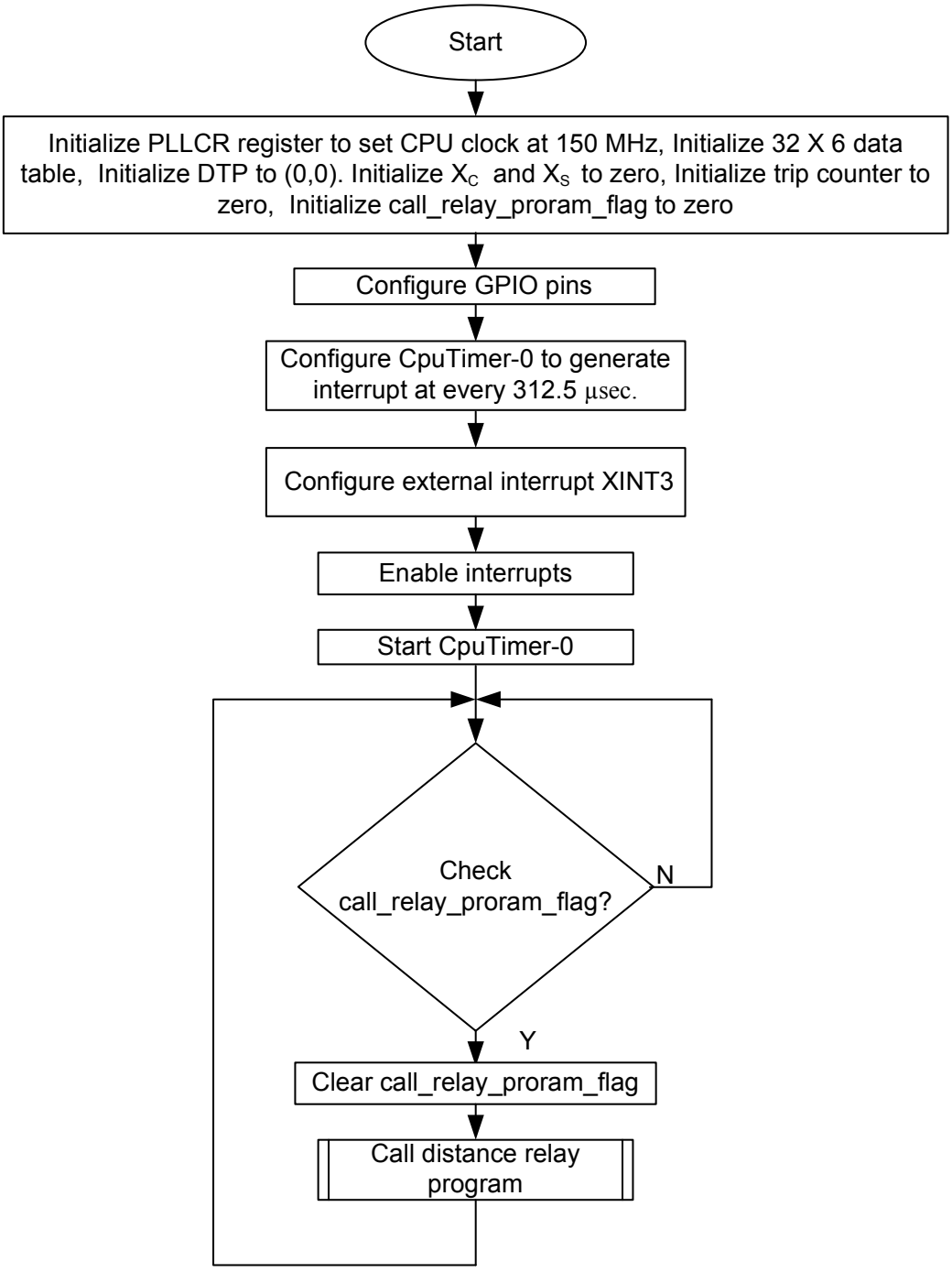


Figure 5.17: Complete Flow Sequence of Relay Software

The following sequence is used to achieve this functionality.

1. GpioCtrlRegs.GPAMUX1.all = 0x0000; GPIO functionality GPIO0-GPIO15
2. GpioCtrlRegs.GPAMUX2.all = 0x0000; GPIO functionality GPIO16-GPIO31
3. GpioCtrlRegs.GPBMUX1.all = 0x0000; GPIO functionality GPIO32-GPIO47
4. GpioCtrlRegs.GPBMUX2.all = 0x0000; GPIO functionality GPIO48-GPIO63
5. GpioCtrlRegs.GPCMUX1.all = 0x0000; GPIO functionality GPIO64-GPIO79
6. GpioCtrlRegs.GPADIR.all = 0x0000; GPIO0-GPIO31 as inputs
7. GpioCtrlRegs.GPAPUD.all = 0x00000000; Pullups enabled GPIO00-31
8. GpioCtrlRegs.GPBDIR.bit.GPIO32 = 1; GPIO32 as output (SOC)
9. GpioCtrlRegs.GPBDIR.bit.GPIO33 = 1; GPIO33 as output ($\overline{RD}$)
10. GpioCtrlRegs.GPBDIR.bit.GPIO35 = 1; GPIO35 as output (Trip signal)
11. GpioCtrlRegs.GPBPUD.bit.GPIO32 = 1;//disable pull up for GPIO32
12. GpioCtrlRegs.GPBPUD.bit.GPIO33 = 1;//disable pull up for GPIO33
13. GpioCtrlRegs.GPBPUD.bit.GPIO35 = 1;//disable pull up for GPIO35

- CpuTimer-0 is configured to generate interrupt signal at every 312.5 μs. The interrupts are handled by Peripheral Interrupt Expansion (PIE) block in DSC28335. This block can support up to 96 peripheral interrupts. The 96 interrupts are grouped into blocks of 8 (INTx1-INTx8) and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each interrupt is supported by its own vector stored in a dedicated RAM block. The CPU, upon servicing the interrupt, automatically fetches the appropriate interrupt vector(PieVectTable). This vector can be overwritten by the user. Also, PIE block facilitates to enable or disable individual interrupt (SPRUFB0D, 2010; SPRS439M, 2012).
  The configuration sequence of CpuTimer-0 is briefed as follows,

  1. DINT; All CPU interrupts are disabled.
  2. IER = 0x0000; Disable CPU Interrupt Enable Registers (IER).
  3. IFR = 0x0000; Clear all CPU Interrupt Flag Registers (IFR).
  4. PieVectTable.TINT0 = &cpu_timer0_isr; TINT0 re-mapped to ISR function declared in this program.
  5. PieCtrlRegs.PIECTRL.bit.ENPIE = 1; Enable the PIE block.
  6. InitCpuTimers(); This in-built function will set the core CpuTimer-0 to a known state and it will stop this timer.
  7. Texas Instruments (TI) has provided a function “ConfigCpuTimer()”. It requires 3 arguments namely, address of the core timer structure, the internal speed of the DSP in MHz, and the period time for the timer overflow in μs.

Hence to generate interrupt signal at every 312.5 μs using this function is written as, ConfigCpuTimer(&CpuTimer0, 150, 312.5).

8. PieCtrlRegs.PIEIER1.bit.INTx7 = 1; The CpuTimer0 interrupt, TINT0 is assigned INTx7 slot corresponding to INT1 CPU interrupt line. This command Enables TINT0.
9. IER |= M_INT1; Enable CPU INT1 which is connected to CPU-Timer 0.

- Configure external interrupt XINT3. The ADS8556 BUSY pin transits high to low level, which indicate completion of analog to digital conversion. This incidence is monitored through GPIO34 which is assigned as external interrupt (XINT3). The configuration sequence is given below.

  1. PieVectTable.XINT3 = &xint3_isr; XINT3 re-mapped to ISR function declared in this program.
  2. PieCtrlRegs.PIEIER12.bit.INTx1 = 1; The XINT3 interrupt, is assigned INTx1 slot corresponding to INT12 CPU interrupt line. This command Enables XINT3.
  3. GpioIntRegs.GPIOXINT3SEL.bit.GPIOSEL = 2; In this DSC there are no dedicated pins for the external interrupts. XINT1 XINT2, and XNMI interrupts can accept inputs from GPIO0-GPIO31 pins. XINT3-XINT7 interrupts can accept inputs from GPIO32-GPIO63 pins. Here, XINT3 is assigned to GPIO34. GPIOSEL is assigned a value 2, which actually means GPIO34 in case of XINT3.
  4. XIntruptRegs.XINT3CR.bit.POLARITY = 0; To configure XINT3 as Falling edge interrupt.
  5. XIntruptRegs.XINT3CR.ENABLE=1; Enable XINT3.
  6. IER |= M_INT12; Enable CPU int12.

Step 2 : All the interrupts are enabled by writing the command EINT.

Step 3 : Start CpuTimer-0 by writing CpuTimer0Regs.TCR.bit.TSS = 0. This will start the process of SOC generation.

Step 4 : Monitor call_relay_proram_flag status. This flag will be set in the ADC ISR after all channels are read stored in the data array. Goto step 5 once it is set.

Step 5 : Clear call_relay_proram_flag and Call distance relay sub program, which

computes fundamental components of all relaying signals, ground and phase impedances, detects faults and issue trip signal. If no fault is detected process is repeats from step 4.

Above steps describe complete flow sequence of relay program developed in this work. One more key aspect in implementation of distance relay software is the ability to perform in real time. This imposes restriction on DSC to execute whole program within inter-sample interval of 625 μseconds. The execution time of distance relay algorithm is found to be around 86 μseconds. It is just 14% of inter sampling interval. This indicates, that few more features can be integrated to relay software, without compromising on sampling frequency.

The section that follow, explains the HIL technique, HIL test set-up and also presents results of evaluation tests conducted to assess numerical distance relay real time performance.

5.5 HIL Testing

Traditional software simulation has the disadvantage of being unable to exactly replicate real operational conditions. On the other hand, a lab model of power system is not capable of fully capturing events of large-scale power system dynamics. One way to bridge the gap between simulation and real conditions is to combine real-time simulation and HIL (Vamsidhar and Fernandes, 2004; Wang *et al.*, 2007, 2009). The HIL simulation is a hybrid simulation technique, where a part of the system is constructed with real hardware, and the remainder is simulated on a real-time simulator (Fathy *et al.*, 2006). The two environments are interfaced to each other using an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC), together with suitable signal amplifiers. This type of simulation is used to test low-power control system equipment or protection relays. This technique allows newly designed device to be tested in controlled safety of a simulated environment rather than in field. Different operating and faulted scenarios can be simulated, without causing harm to power system. This section explains HIL technique used to test newly developed distance relay hardware and

results are presented.

5.5.1 Hardware In the Loop Test Set-up Description

The figure 5.18 shows block schematic of HIL set-up developed to evaluate performance of the relay in real time.

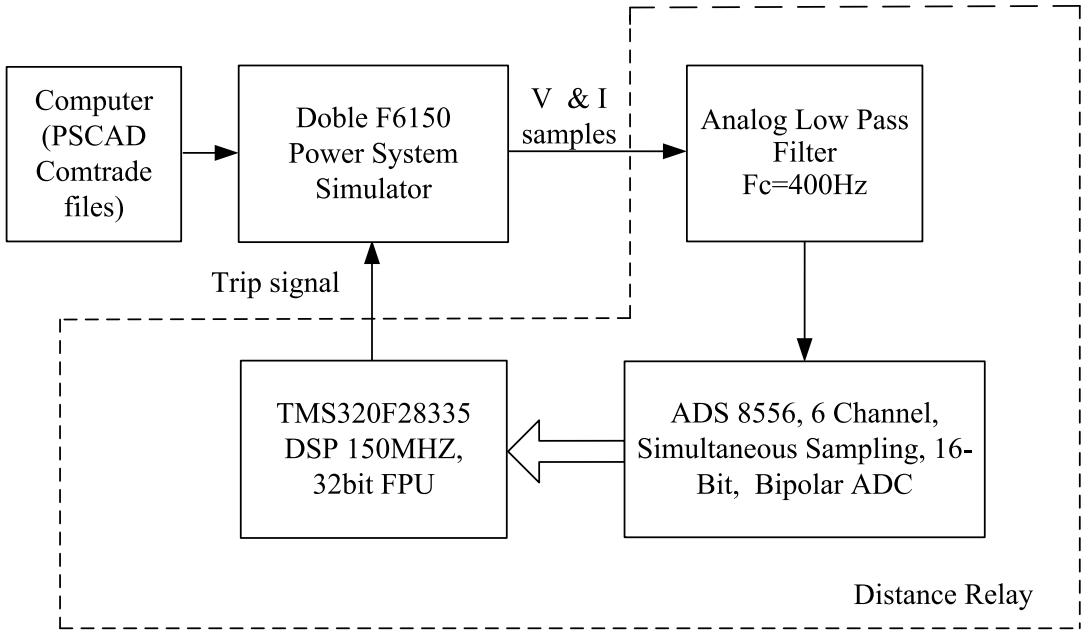


Figure 5.18: Block Diagram of HIL Setup for Real Time Testing of Digital Distance Relay

It consists of a PC supporting EMTDC/ PSCAD software, a power system simulator (Doble make, Model F6150, 150VA, three phase voltage and current signal generator) and a distance relay unit under test, forming a complete digital relay test bench. The model power system has been simulated in PSCAD/EMTDC environment for various fault transient conditions. The results of these cases are stored in respective COMTRADE91 files (Phadke *et al.*, 1992; Kezunovic, 2002; Ryan, 1997), which are useful as relaying signals. All relaying signals are suitably converted and scaled down, to match $\pm$ 12 Volts input range of ADC (ADS8556), before loading on to power system simulator. Also, phase currents have been stored as scaled voltages in COMTRADE

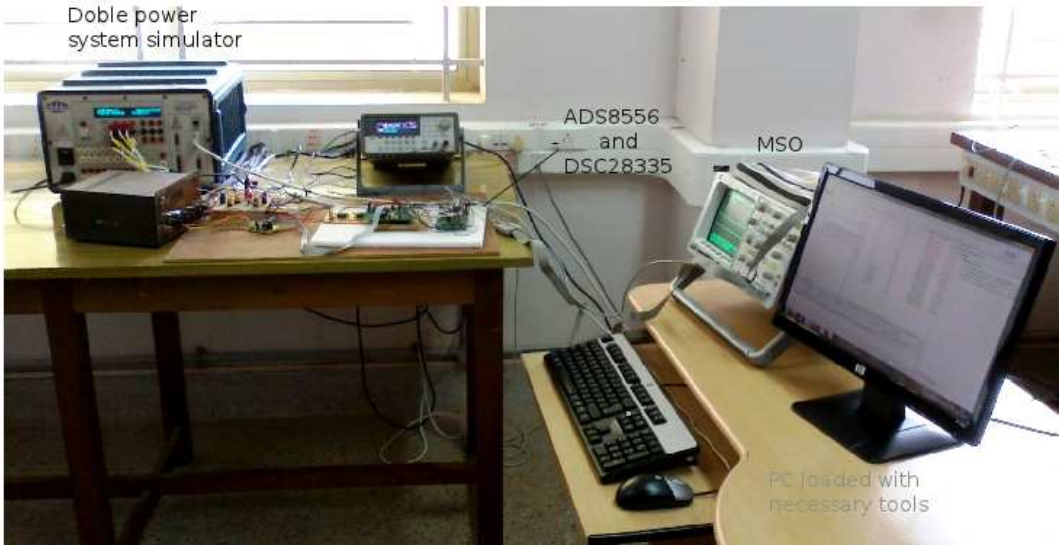


Figure 5.19: Photograph of the HIL test set-up

files, therefore current sources can be replaced by voltage sources in the Doble F6150 power system simulator. This eliminates need for external current to voltage converter circuit in relay test set-up. These conditioned relaying signals are loaded to Doble power system simulator using Transwin3.3® software(TransWin, 2011). Doble power system simulator generates relaying signals in real time, which form equivalent to secondary injection signals to the distance relay unit under test. The trip signal issued by distance relay is used as an input to the digital input port of Doble power system simulator. Simulator stops playing the waveforms immediately after receiving the trip signal. The photograph of complete HIL set-up is shown in 5.19. The figure 5.20 shows enlarged view of ADS8556 interfaced with DSC28335. The following paragraph presents HIL test results.

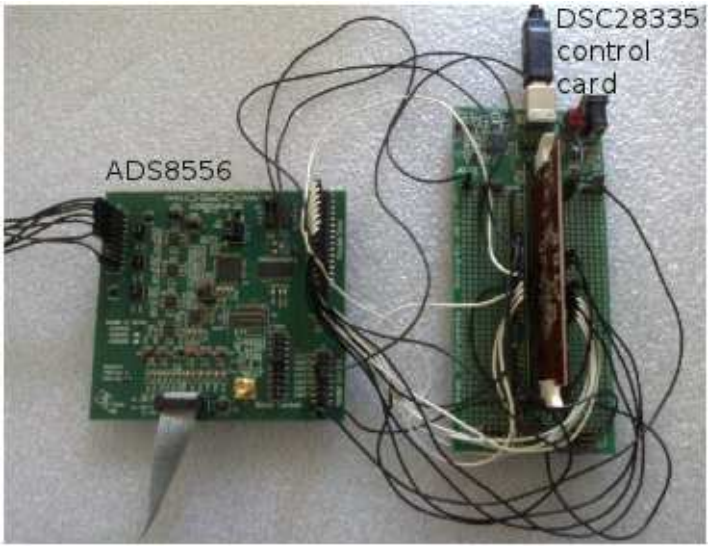


Figure 5.20: Photograph of ADS8556 interfaced with DSC28335

5.5.2 HIL Test Results

About 100 test cases have been considered to verify the performance of DSC based distance relay. The performance of the distance relay has been satisfactory for all the test cases. As a sample, two cases are presented here with oscilloscope screen shots. The relay response for AB fault at 100 kilometers from the relay location is shown in the figure 5.21. The first waveform shows the scaled real time fault current of phase-A produced by the DOBLE power system simulator. The second waveform of the same figure is the trip signal issued by the distance relay. It can be seen that the relay issued trip signal in about 11.2 milliseconds. Similarly relay response for a phase-A to ground (AG) fault at 150 kilometers from the relay location is shown in the figure 5.22. For this zone end fault relay took 19.60 milliseconds to issue the trip signal.

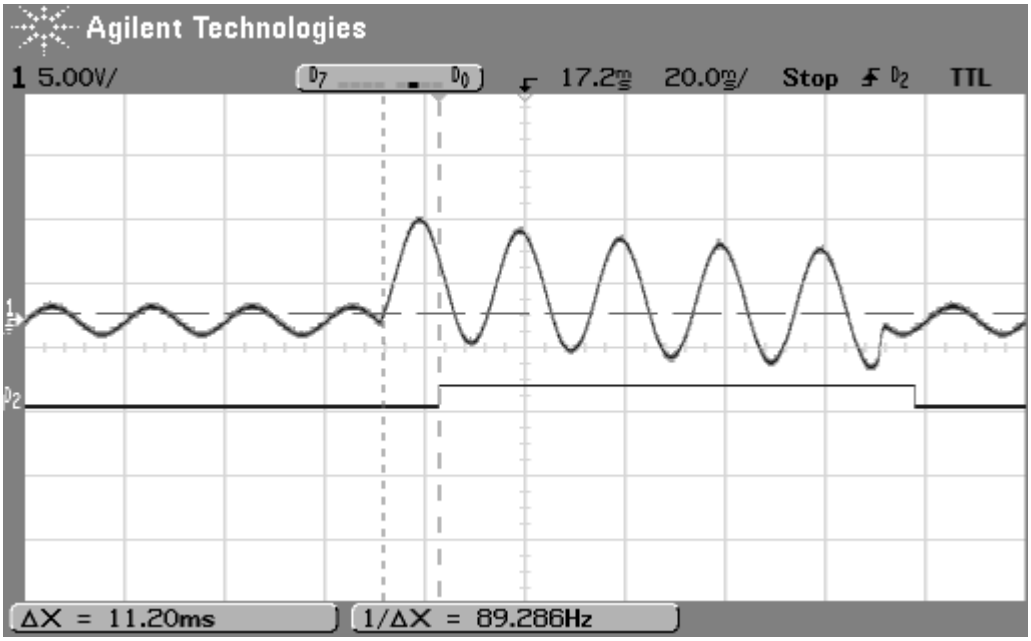


Figure 5.21: Fault current waveform and the trip signal issued by the distance relay for AB fault at 100KM.

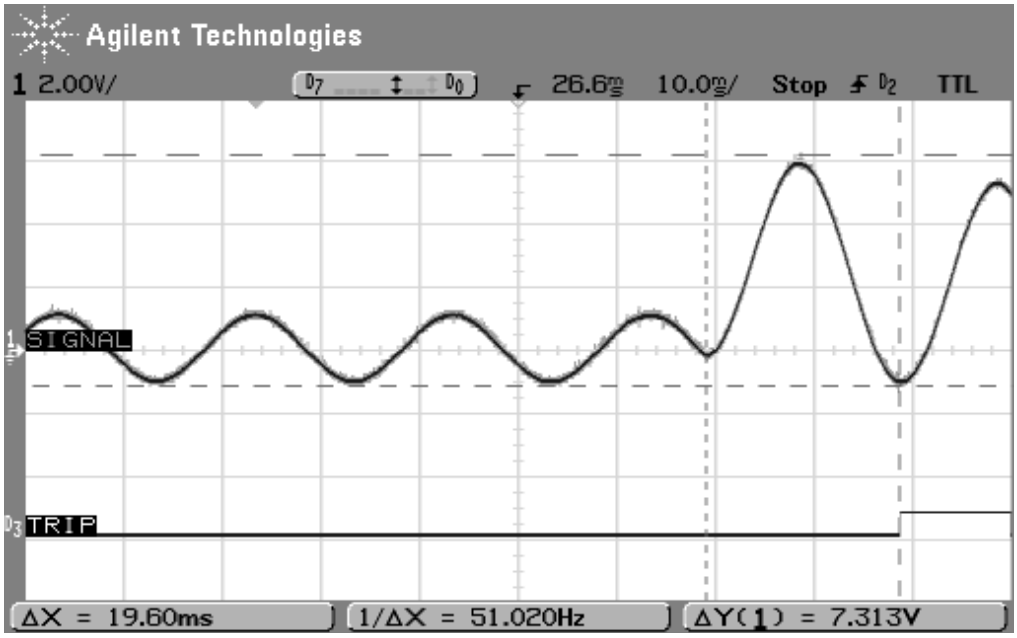


Figure 5.22: Fault current waveform and the trip signal issued by the distance relay for AG fault at 150KM.

The above results proved the functionality of the newly developed conventional distance relay. The distance relay algorithm is executed in about eighty six μseconds. In the second phase, proposed adaptive distance relay has been developed with minor modifications in hardware and software modules of the conventional distance relay.

5.6 Development of Adaptive Distance Relay

The block diagram of the relay hardware designed and configured for implementing proposed adaptive distance relay is as shown in the figure 5.23. The adaptive relay hardware scheme consists of nine analog input channels namely; three phase voltages, three phase currents at the relay location and three phase STATCOM currents. A phase lag compensator is required in practical relaying schemes to compensate channel communication delay. Two numbers of ADS8556 are required for the present application in order to digitize nine channels simultaneously. The SOC signal is applied simultaneously to both ADS8556 modules, with equal trace lengths to minimize skewing in signal events. The 16-bit output of the ADS8556-1 (measuring signals local to relay location) connected to higher 16-bits and output of the second ADS8556-2 (remote STATCOM phase currents) is connected to lower 16-bits of port A as shown in the figure. The SOC and read signals are generated through output port of the DSC and properly coordinated to read all nine analog channels. Samples received are stored in their respective data table. This data is processed by the adaptive relay software. The adaptive relay software has been already discussed and its performance has been evaluated in the simulation mode in section 4.2 of chapter 4. Both mho and quadrilateral relay logic has been implemented here on the DSC, serves as the adaptive relay software.

5.6.1 Performance Evaluation of Adaptive Distance Relay

The HIL procedure described in the section 5.5.1 has been followed for the performance evaluation of adaptive distance relay. The performance of both mho and quadrilateral

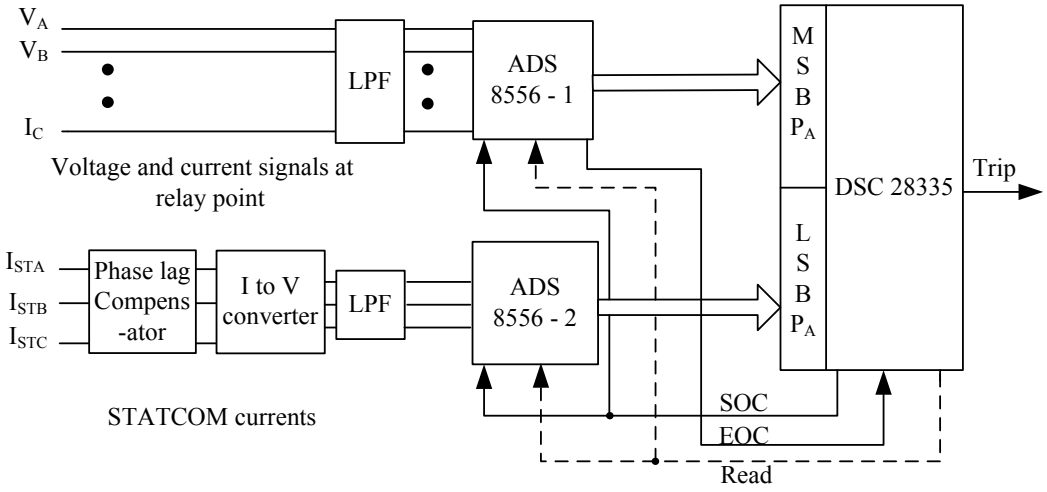


Figure 5.23: Block Diagram of adaptive distance relay hardware

relays have been evaluated in detail. The required COMTRADE fault data files obtained from EMTDC/PSCAD simulations are loaded to Doble power system simulator. The steady state impedance measured by the adaptive relay hardware has been noted for all the cases. Tables 5.2 shows the impedances measured by both adaptive relay model and adaptive relay hardware for solid single line to ground faults, double line faults, double line to ground faults and three phase faults at 60 Km, 100Km and 160 Km of the transmission line respectively. The mho relay logic has been used as a fault detector.

Table 5.2: Impedance measured by adaptive relay for AG faults

Fault distance from relay(KM)	Actual fault impedance R + jX (Ω)	Impedance measured by adaptive relay: Model R + jX (Ω)	Impedance measured by adaptive relay: Hardware R +jX (Ω)
AG Faults			
60.00	2.08 + j25.40	2.15 + j25.39	2.05 + j26.20
100.00	3.47 + j42.34	3.61 + j42.38	3.30 + j42.51
160.00	5.55 + j67.74	5.80 + j68.32	5.75 + j68.04
BC Faults			
60.00	2.08 + j25.40	2.10 + j25.43	2.22 + j25.12
100.00	3.47 + j42.34	3.53 + j42.48	3.42 + j 42.11
160.00	5.55 + j67.74	5.71 + j68.41	5.78 + j68.45
AB-G Faults			
60.00	2.08 + j25.40	2.09 + j25.35	2.01 + j25.40
100.00	3.47 + j42.34	3.51 + j42.39	3.45 + j42.41
160.00	5.55 + j67.74	5.62 + j68.16	5.72 + j68.25
ABC Faults			
60.00	2.08 + j25.40	2.10 + j25.43	2.21 + j25.48
100.00	3.47 + j42.34	3.53 + j42.48	3.48 + j42.40
160.00	5.55 + j67.74	5.72 + j68.58	5.67 + j68.48

It can be seen from these table that the steady state impedance measured by software model implemented in EMTDC / PSCAD and DSC based hardware relay closely match with each other. The adaptive relay program took about 106 μseconds for execution of one complete sequence. This increase in relay cycle time is mainly due to the incorporation of three additional analog channels and computation of fundamental components of these signals using RFCWF algorithm. Also, the computation of adap-

tive relay equations, which are complex in nature have contributed to the increase in the execution time. Total execution time of 106 μseconds is about 17% of the inter sample interval, which is 625 μseconds. Table 5.3 shows status of trip signal of DSC based conventional and adaptive relays for the zone end fault cases. The relay reach is set at 160 Km of the line for all cases, ✓ and X symbols denotes 'Operation' and 'No operation' of the relay respectively in this table. It can be seen that for first case, both conventional and adaptive relays have operated for an AG fault at 50 KM from the relay location. Case numbers 2-5 show the responses of both relays for all types of faults close to reach setting, i.e,. at 150 KM from the relay location. It can be seen that, conventional relay under-reached its zone setting, causing No operation, whereas adaptive relay operated successfully for all the cases. Both relays have shown similar responses for the zone end faults (@160 KM) as indicated by the case numbers 5-9. Table 5.4 gives the values of actual fault impedance and the steady state apparent impedance measured by both relays for the respective fault cases mentioned in table 5.3. It can be seen that the adaptive relay measures the correct fault impedance for all types of faults, hence it successfully mitigates STATCOM's influence on the distance relay performance.

Table 5.3: Operation of the conventional and adaptive relays with STATCOM

Case number	Fault type	Fault distance (KM)	Conventional relay with STATCOM	Adaptive relay with STATCOM
1	AG	50	✓	✓
2	AG	150	X	✓
3	AB	150	X	✓
4	BC-G	150	X	✓
5	ABC	150	X	✓
6	AG	160	X	✓
7	AB	160	X	✓
8	BC-G	160	X	✓
9	ABC	160	X	✓
10	ABC	170	✓	X

Table 5.4: Apparent impedance seen by the conventional and adaptive relays with STATCOM

Fault type	Fault distance (KM)	Actual impedance,(Ω)	Conventional relay Measured impedance,(Ω)	Adaptive relay Measured impedance,(Ω)
AG	50	1.73 + j21.16	1.72 + j21.71	1.72 + j21.71
AG	150	5.20 + j63.50	5.73 + j71.22	5.56 + j64.12
AB	150	-do-	8.07 + j69.17	5.37 + j64.12
BC-G	150	-do-	8.18 + j70.04	5.17+j63.78
ABC	150	-do-	7.14 + j70.51	5.21 + j64.00
AG	160	5.54+j67.73	6.17 + j77.57	5.75 + j68.04
AB	160	-do-	8.38 + j77.87	5.78 + j68.45
BC-G	160	-do-	7.89 + j76.57	5.72 + j68.25
ABC	160	-do-	7.89 + j76.56	5.67 + j68.48
ABC	170	5.89 + j71.97	5.69 + j68.53	5.92 + j72.02

The HIL tests have also been conducted to assess the performance of specifically shaped quadrilateral relay characteristics developed in section 4.2 of chapter 4. The COMTRADE files for various types of faults involving R_f at various levels of reactive component of STATCOM current (I_q) have been generated through simulations. These COMTRADE files are loaded to Doble power system simulator, which in-turn presents real time signals to the relay. The prime objectives of the test is to determine whether the relay automatically attunes to the prevailing value of I_q and to verify the operating time of the relay. The test results have been tabulated in the table 5.5. It can be seen that the relay has operated properly for all values of I_q for various faults with different values of R_f. The maximum operating time of the relay is approximately one fundamental cycle time for zone end faults. The operating time slightly more than 20 ms for high resistance zone end faults in few cases. The minimum operating time of 11.00 ms has been observed for the close end faults without fault resistance.

Table 5.5: Performance of quadrilateral relay

I_q (p.u.)	R_f (Ω)	Fault type	Fault location (in % of relay setting)	operating time(ms)
1.00	50	AG	100	21.00
1.00	25	BC	100	20.62
1.00	0	AG	100	16.15
1.00	50	AG	75	20.00
1.00	25	AB	75	18.75
1.00	0	AG	75	16.50
1.00	50	BCG	50	19.8
1.00	25	ABC	50	13.75
1.00	0	AG	50	12.75
0.50	50	AG	100	20.00
0.50	25	BC	100	20.15
0.50	0	AG	100	18.75
0.50	50	AG	75	19.00
0.50	25	CA	75	18.75
0.50	0	AG	75	17.00
0.50	50	AG	50	13.75
0.50	25	BC	50	13.00
0.50	0	AG	50	12.75
0.50	50	BG	100	20.00
0.50	25	BC	100	19.85
0.50	0	AG	100	18.00
0.50	50	AG	75	20.00
0.50	25	BC	75	20.00
0.50	0	AG	75	18.00
0.50	50	AG	50	19.95
0.50	25	CA	50	20.00
0.50	0	AG	50	13.00
0.00	50	AG	100	20.02
0.00	25	BC	100	20.10
0.00	0	AG	100	19.98
0.00	50	AG	75	18.12
0.00	25	BC	75	17.75
0.00	0	AG	75	17.25
0.00	50	AG	50	13.25
0.00	25	ABG	50	12.25
0.00	0	ABC	50	11.00

Table 5.6 gives the performance of both mho and quadrilateral relays for various fault scenarios. It can be seen by the table that both types of relays have operated properly for solid faults irrespective of the I_q. But the mho relay under-reached first zone setting in the case of faults involving R_f, whereas quadrilateral relay gives accurate trip decision.

Table 5.6: Performance of mho and quadrilateral characteristic relays

SL NO	I_q setting (p.u.)	Fault Type	R_f (Ω)	Mho relay	Shaped Quadrilateral relay
1	1.00	AG	0	✓	✓
2	1.00	AG	30	X	✓
3	1.00	BC	50	X	✓
4	0.50	AG	0	✓	✓
5	0.50	BC	30	X	✓
6	0.50	AG	50	X	✓
7	0.25	AG	0	✓	✓
8	0.25	BC	30	X	✓
9	0.25	AG	50	X	✓
10	0.00	AG	0	✓	✓
11	0.00	BC	30	X	✓
12	0.00	AG	50	X	✓

This Chapter presented the development and real time testing of adaptive distance relay. The chapter begun with development of distance relay hardware, and discussed several important issues such as selection of appropriate devices for the relay implementation and HIL relay test bench. The distance relay implemented using new devices like DSC TMS320F28335 and simultaneous conversion type ADC (ADS8556), eliminates the need of external hardware components such as sample and hold circuits, reference signal generators etc. This provides a convenient platform for developing a high speed and modular numerical protection relays, which are more reliable due to reduced hardware components. Further, the basic conventional relay hardware has been enhanced, to realize the proposed adaptive distance relay. The modifications made in the relay hardware and software modules have been presented.

The adaptive relaying schemes with mho and quadrilateral relays as fault detectors have been developed. Both schemes have been deployed on the DSC based relay hardware. The performance of adaptive relays have been evaluated using HIL test procedure. The HIL results matched closely with the simulation results. The adaptive mho relay operates accurately for all types of solid faults on a STATCOM connected transmission line. But its accuracy is greatly affected by fault resistance. The adaptive relaying scheme, which evokes the appropriate quadrilateral relay characteristics depending upon the prevailing reactive power compensation accurately detects both solid faults and faults with R_f. The time taken for issuing the trip signal is about 20 ms for zone end faults. This shows that the adaptive relaying scheme with shaped relay characteristics successfully abates reach problems of the relay in the STATCOM connected transmission lines. In the next chapter the broad conclusions drawn from the results of analysis carried out in the research work are presented.

CHAPTER 6

Conclusion and Future Scope

The main objective of this research was to study the influence of midpoint connected STATCOM on the distance rely performance and to develop an adaptive relaying scheme to mitigate its adverse impact. The conclusion drawn, major contributions and the scope for further investigations is presented in this chapter.

6.1 Conclusions

The following conclusions are drawn from the research work presented in this thesis,

Transient behavioral model of a 48 pulse, three level inverter based STATCOM model has been built in EMTDC/PSCAD software package. The complete mathematical analysis of multipulse multilevel inverter has been carried out, equations describing the output voltage of the individual stages has been presented with their respective waveforms. This type of inverter produces a premium quality output voltage waveform with 3.81 % harmonic content, which can be directly connected to high voltage applications without filtering. The $\pm 100MVA$ and $\pm 200MVA$ STATCOM models have been developed to cope up with the different levels of power transmission needs and to facilitate the study account for influence of STATCOM rating on the relay performance. A decoupled current controller has been implemented to operate the STATCOM in both voltage control mode and reactive power control mode successfully for a wide range of varying system conditions by considering a realistic study system. The study indicated that installation of STATCOM benefits the power system. It helps to maintain the voltage profile along the transmission line, thereby enhances the power transfer capability of the existing power system.

The influence of STATCOM on distance relay performance for different faults at various locations under varying system conditions have been studied. The mathematical equations pertaining to apparent impedance measurement error for different fault conditions are derived. It is observed that the amount of impedance error varies depending on factors such as,fault type, fault location, reactive current injected by the STATCOM and its operating mode before fault. It has been found that the relay suffers from under-reaching effect during voltage control mode, but over-reaches its first zone setting for certain faults while operating in inductive mode during lightly loaded conditions. It has also noted that the level of reach problem is more pronounced in higher rating STATCOM. The simulation results indicated that stand alone distance relay cannot provide adequate protection to the STATCOM connected transmission lines.

An adaptive distance relaying scheme has been developed to mitigate the reach problems. The adaptive distance relaying scheme developed in this work, requires time stamped three phase STATCOM currents for the calculation of the exact impedance to the fault. Adaptive equations are derived by modeling the STATCOM as in-feed, to correct the measured apparent impedance error. A current ratio factor (C_{ratio}) has been derived for phase to phase and phase to ground relay units separately which have to be substituted in the adaptive equations to combat the error. The efficacy of the scheme is tested in the simulation environment with mho type fault detector. This scheme successfully mitigates the first zone reach problems in the case of solid faults. However it fails to provide protection in the case of resistive faults. Therefore, option of specifically shaped relay characteristics has been explored, which is possible due to distinct feature offered by numerical relays. The relay characteristic has been shaped with various types of faults with R_f at different levels of compensation provided by the STATCOM. The model system exhibited specific characteristics in respect of ground and phase relays. But in both cases the shaped characteristic has been realized using quadrilateral characteristics without the loss of accuracy. The simulations encompassing all types of faults at various levels of reactive power compensation have been carried out to evaluate the performance of shaped relay characteristic. The results show that quadrilateral relay adapts characteristics according to prevailing compensation level. Hence provides

reliable protection for the STATCOM connected transmission lines.

The adaptive distance relay has been implemented, using TMS320F28335 DSC and a six channel high speed simultaneous sampling analog to digital converter ADS8556. The relay software has been developed in embedded C language using code composer studio (CCS IV) platform targeted for TMS320F28335 DSC. The advantage of such a relay is that it is highly compact, modular and reliable because of fewer components. The fundamental component of the relaying quantities were extracted by , RFCWF algorithm to save the computation time. Both mho relay and quadrilateral relay characteristics have been implemented on the relay.

The new adaptive distance relaying schemes have been tested using the hardware in the loop test procedure to ascertain the real time performance. The HIL test set up consists of a computer loaded with EMTDC/PSACD software, a Doble F6150 power system simulator and adaptive distance relay hardware. The real time tests encompassing all power system conditions are conducted, the results were verified with the simulation results and found close to 100 percent match between them. The adaptive relay algorithm executed in about 106 μseconds at CPU clock of 150 MHz. This is about 17% of the inter sample interval, which is 625 μseconds shows that relay hardware used in this work is a feasible option.

6.2 The major contributions of this research work

The major contributions of this research work are listed below.

- Complete mathematical equations describing the operation of a 48 pulse three level inverter has been derived.
- Transient behavioural models of $\pm$ 100 MVA and $\pm$ 200 MVA STATCOM have been built using 48 pulse inverter in EMTDC/PSCAD. The influence of STATCOM on the performance of the distance relay was studied analytically and through simulations.
- Adaptive distance relaying schemes have been developed to mitigate the adverse impact of STATCOM on the distance relay performance.

- Distance relay hardware capable of handling the adaptive relaying schemes has been developed using recently released 32 bit floating point DSC (TMS320F28335) and a 6 channel simultaneous sampling ADC (ADS8556).
- HIL test set up has been configured using the Doble F6150 power system simulator. The performance of the adaptive schemes developed in this research work have been successfully evaluated using HIL procedure.

6.3 Future Scope

- The STATCOM controller developed in this work is based on symmetrical firing pulse generation scheme. The effect of individual phase controller scheme on the distance relay performance can be studied.
- The communication channel has not been modelled in this work. The modelling of communication channel and channel delay effects on the relay performance can be explored.
- The effect of other types of FACTS devices on the performance of the distance relay can be studied and the adaptive schemes can be developed.
- The Wavelet transform based feature extraction techniques can be evaluated to avoid reach problem in STATCOM connected transmission lines. Also, the application of Artificial Neural Network (ANN) based relays can be explored. Such relays, when imparted proper training can accurately detect faults under various operating conditions of the power system.

APPENDIX A

PSCAD/EMTDC Model of the Model Power System and its Parameters

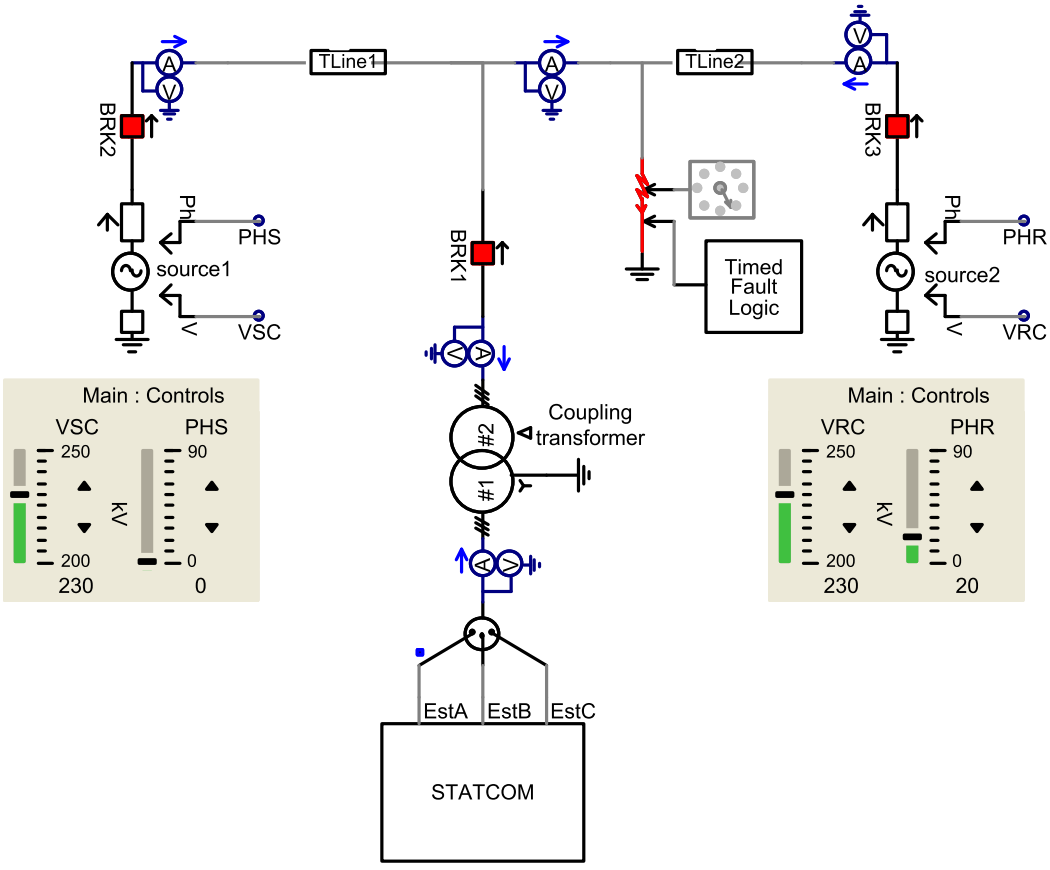


Figure A.1: Study power system model

Table A.1: Equivalent source data

Parameter	Rating
Base Voltage	230 KV
short circuit level	10000 MVA
X/R ratio	8
Frequency	50 Hz

Table A.2: Coupling transformer data

Parameter	Rating
Nominal power	100 MVA
Primary voltage	138 KV
Secondary voltage	230 KV
leakage reactance	0.1 pu

Table A.3: STATCOM data

Parameter	Rating
Rated Power	100 MVA
Rated Voltage	138 KV
Number of Pulses	48
Capacitance	3000 μ F each
Capacitor Voltage	9.650 KV each

Table A.4: Transmission line data

Parameter	Rating/Type
Line length	200 km
Line-line voltage	230 KV
Model	Frequency dependent
Transpose of conductors	Ideally transposed
Number of phase conductors	3
Number of ground wires	2
Shunt conductance	1.00E-10 G/m
Positive sequence resistance	0.03467 Ohms/KM
Positive seuqence reactance	0.42336 Ohms/KM
Zero sequence resistance	0.10401 Ohms/KM
Zero seuqence reactance	1.142641 Ohms/KM

Table A.5: PI controller parameters

Voltage controller	
k_p	12
k_i	0.001
Reactive current controller	
k_p	30
k_i	0.005

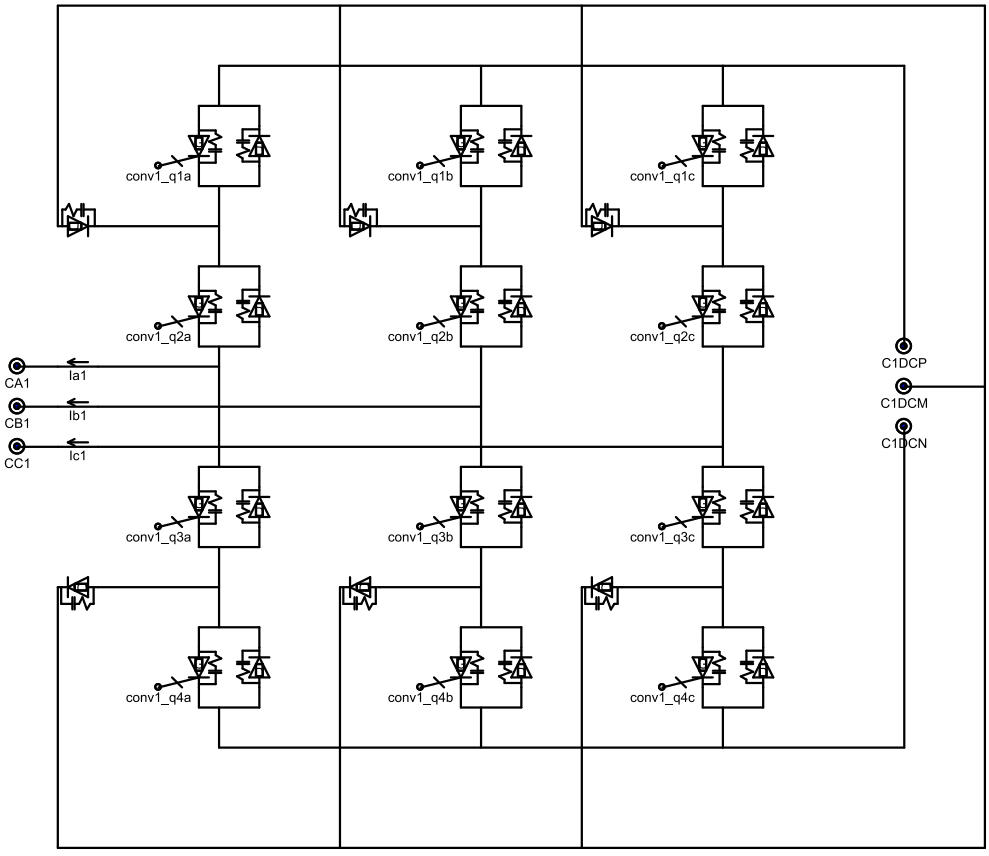


Figure A.2: Three phase three level inverter

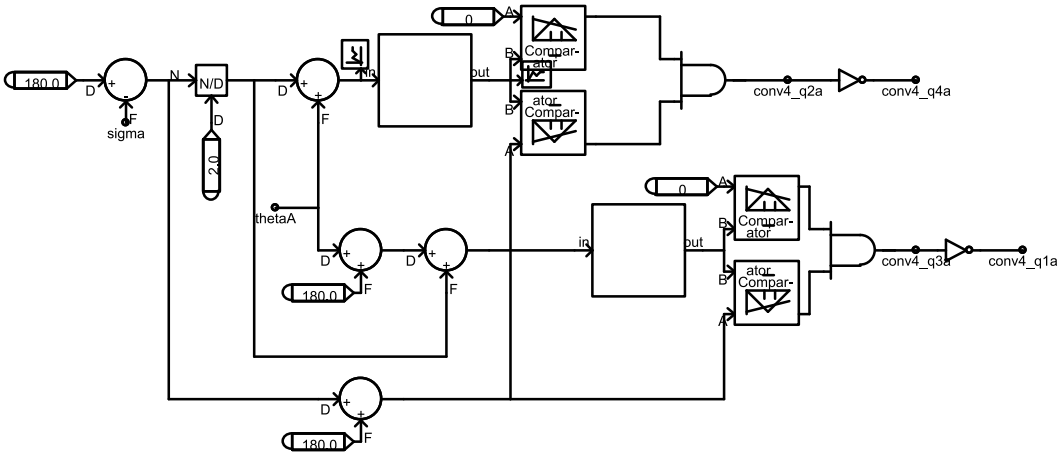


Figure A.3: Firing pulse generator

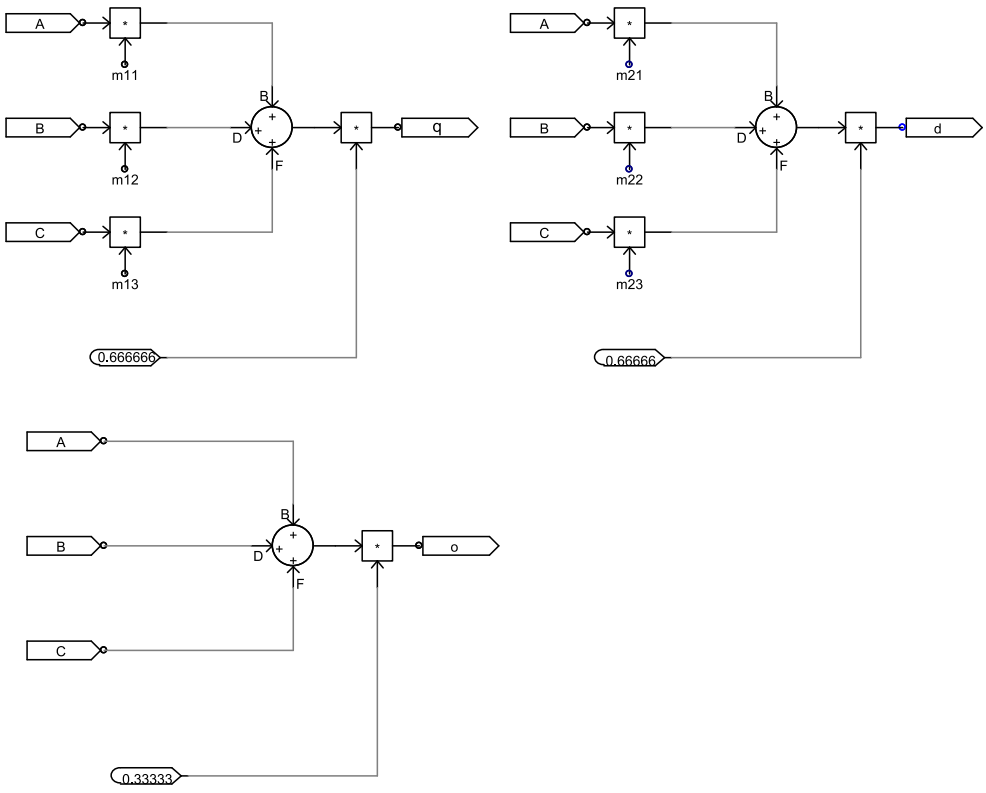


Figure A.4: abc to dq0 transformation implementation

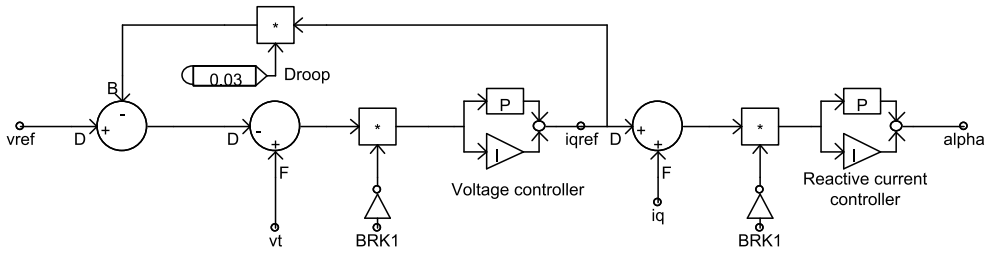


Figure A.5: STATCOM controller

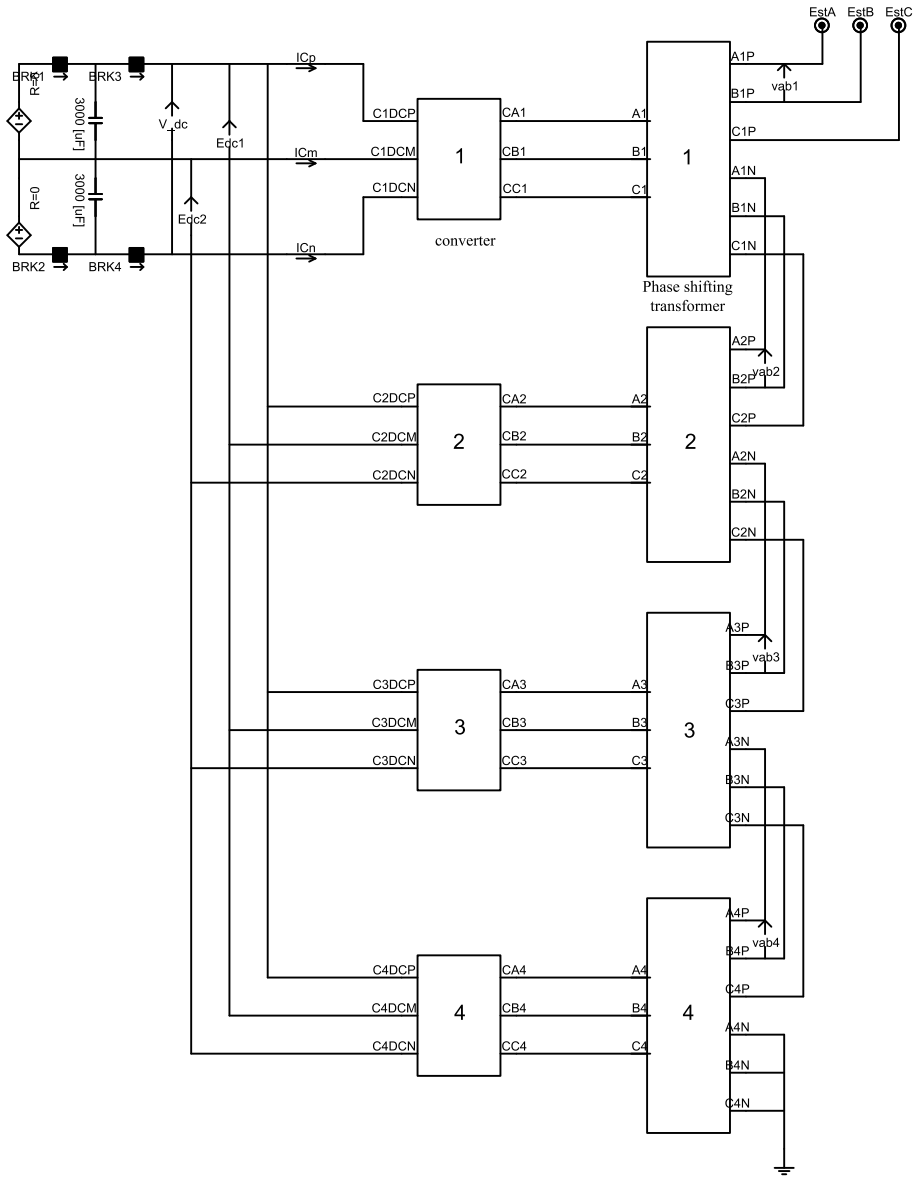


Figure A.6: 48 Pulse STATCOM structure

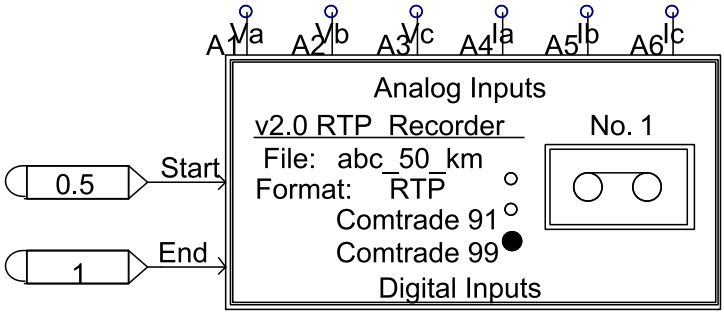


Figure A.7: Real time playback block configured to create to COMTRADE files

APPENDIX B

ADS8556 Parallel Interface Specifications

Figure B.1 shows the timing diagram for parallel read access. The details of timing instants/intervals marked on the diagram are mentioned in the Table B.1.

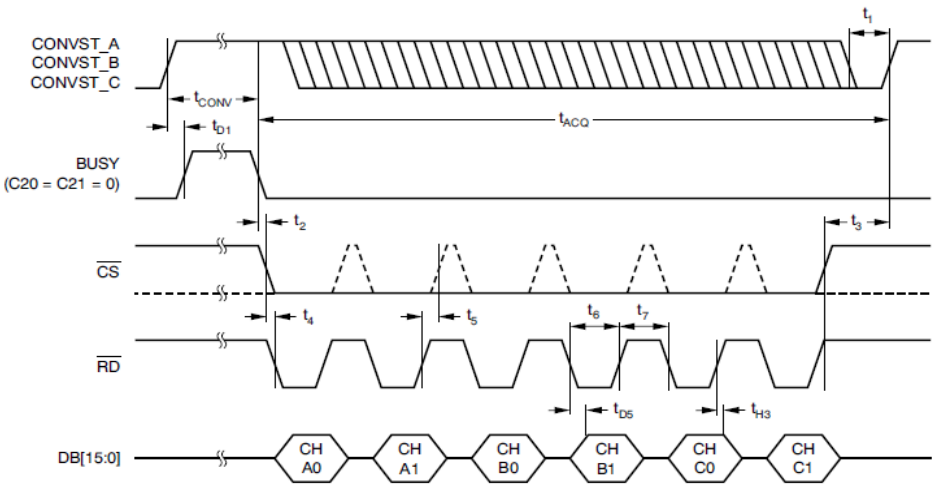


Figure B.1: Timing diagram for parallel read access

Table B.1: Parallel Interface Timing Requirements

Notation	Parameter Name	Min	Max	Units
t_{ACQ}	Acquisition time	280		ns
t_{CONV}	Conversion time		1.26	μs
t_1	CONVST_x low time	20		ns
t_2	BUSY low to $\overline{CS}$ low time	0	0	ns
t_3	Bus access finished to next conversion start time	40		ns
t_4	$\overline{CS}$ low to $\overline{RD}$ low time	0		ns
t_5	$\overline{RD}$ high to $\overline{CS}$ high time	0		ns
t_6	$\overline{RD}$ pulse width	30		ns
t_{D1}	CONVST_x high to BUSY high delay	50	20	ns
t_{D5}	$\overline{RD}$ falling edge to output data valid delay		20	ns
t_{H3}	Output data to $\overline{RD}$ rising edge hold time	5		ns

APPENDIX C

Fourier Recursive Full Cycle Window Algorithm

In the Fourier algorithm, a desired harmonic frequency component is extracted from the relaying signal samples by correlating with the reference sine and cosine wave samples of the desired frequency. This method processes data sample window of one fundamental cycle width and popularly known as Full cycle window Fourier algorithm (FCWF). The Discrete Fourier Transform of X_k contains the fundamental frequency component given by,

$$X_C = \frac{2}{N}\sum_{k=0}^{N-1} x_k \cos\left(\frac{2\pi}{N}k\right) \tag{C.1}$$

$$X_S = \frac{2}{N}\sum_{k=0}^{N-1} x_k \sin\left(\frac{2\pi}{N}k\right) \tag{C.2}$$

Where,

X_c = Real part of fundamental component

X_s = Imaginary part of fundamental component

N = Number of samples per cycle

x_k= k^{th} sampled signal data

The magnitude and the phase of the signal can be computed using equations C.3 and C.4 given below,

$$Magnitude = \sqrt{X_C^2 + X_S^2} \tag{C.3}$$

$$Angle = \tan^{-1}\left(\frac{X_S}{X_C}\right) \tag{C.4}$$

But in practical applications, full cycle window Fourier algorithm will be used in recursive mode for saving computation time by using equations C.5 and C.6 this will

reduce computation from 2N multiply add operation in normal DFT to 4 additions and 2 multiplications per update.

$$X_C^{w+1} = X_C^w + (x_{w+N} - x_w)\cos\left(\frac{2w\pi}{N}\right) \tag{C.5}$$

$$X_S^{w+1} = X_S^w + (x_{w+N} - x_w)\sin\left(\frac{2\pi w}{N}\right) \tag{C.6}$$

w = current window

The computation for X_c^w and X_c^{w+1} can be visualized from the figure C.1. Similar operation will be performed to compute the X_s^w and X_s^{w+1}.

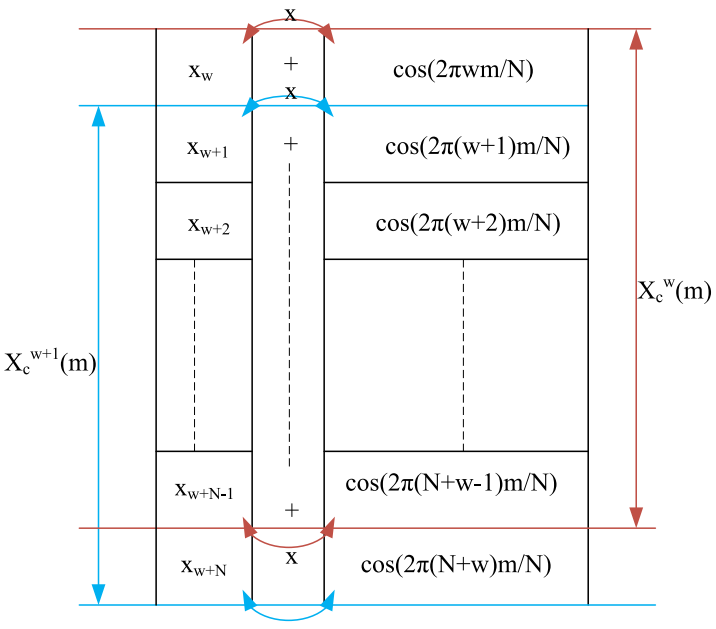


Figure C.1: Mechanism of recursive full cycle window algorithm (Soman, 2010)

APPENDIX D

DOBLE Power System Simulator and its Configuration Using TransWin Software

D.1 Dbole F6150 Power System Simulator

The F6150 is an instrument with the high power, flexibility, and sophisticated software to run full simulation tests on relays and protection schemes. It provides everything required in a single, field-rugged, portable box. It can test everything from a single, high-burden electromechanical earth/ground fault relay to complete, modern, multi-function numerical microprocessor protection schemes, without the need for additional instruments. It can perform steady-state, dynamic-state, and transient simulation tests. The F6150 can even be used for end-to-end protection scheme tests using Global Positioning System technology to synchronize remotely located F6150s. Also the IEC61850 features in F6150 are KEMA TESTED. There are many softwares available to suit the particular test requirements. In this work TranWin software package is used to configure the Doble instrument (PN500, 2007).

D.1.1 Configuration of Doble F6150 Using TransWin software package

A brief explanation of the procedure, followed to configure the Doble instrument for relay testing is presented in the following paragraphs,

1. Upon start up TransWin package prompts three options from the menu as shown in the figure. Transient Playback option must be selected to play the recorded COMTRADE files.

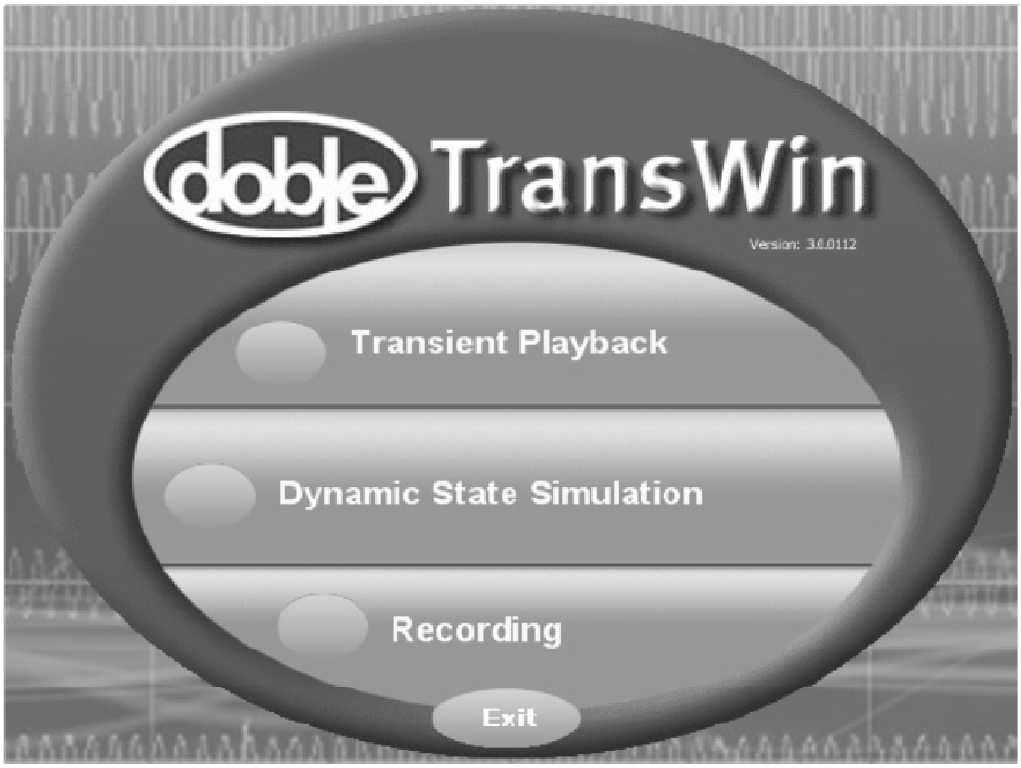


Figure D.1: Main menu of the TransWin program

2. Open the proper *.cfg file which contains the required test waveforms.
3. Establish connection between PC and the Doble F6150 using serial or Ethernet conncetion (TransWin, 2011)
4. Choose the channels required to conduct the test by checking the enable playback box as shown in the figure D.2 . This software displays the minimum and maximum values of the respective waveforms; this is an important feature enables user to check whether the signal amplitude is within the ADS8556 input range or not.

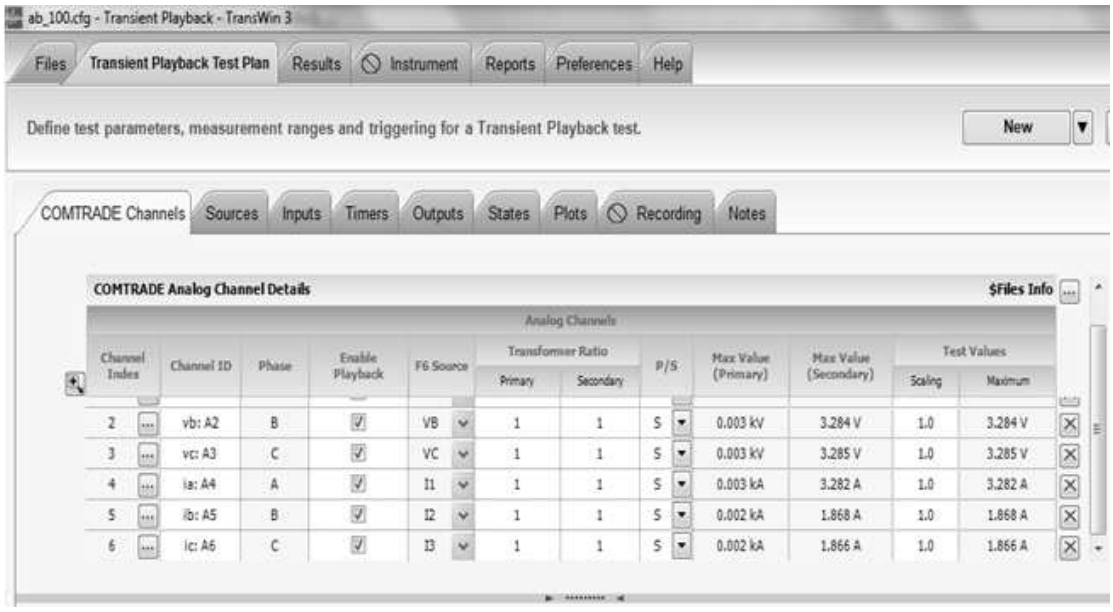


Figure D.2: Output channels configuration menu

5. Configure the Doble F6150 sources as per the test requirements using the menu as shown in the figure D.3. It includes few standard configuration set up available in the configuration menu. If any other configuration is required, then user can choose custom configuration under the configuration menu and configure according to the test requirements.

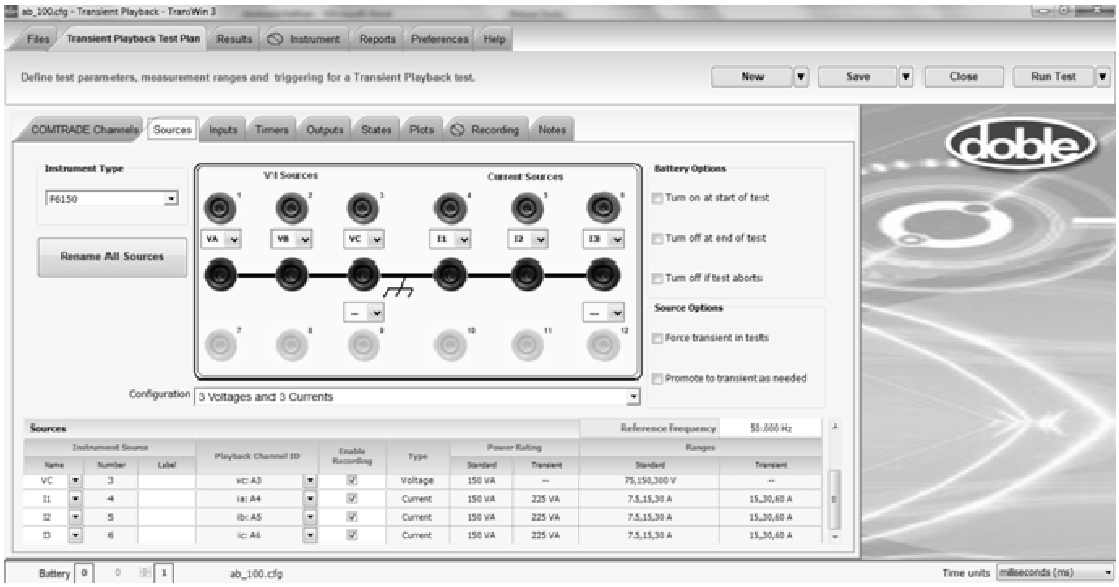


Figure D.3: Source configuration menu

6. Verify the test signal waveforms that will be played by the simulator, by clicking

on the *plot* tab before playing the waveform. To play the waveforms in real time click the on the Run Test tab and choose the appropriate options under the menu as shown in the figure D.4. The signal can be played once or continuously as per the test requirements. These signals will be available on the respective sources for testing.

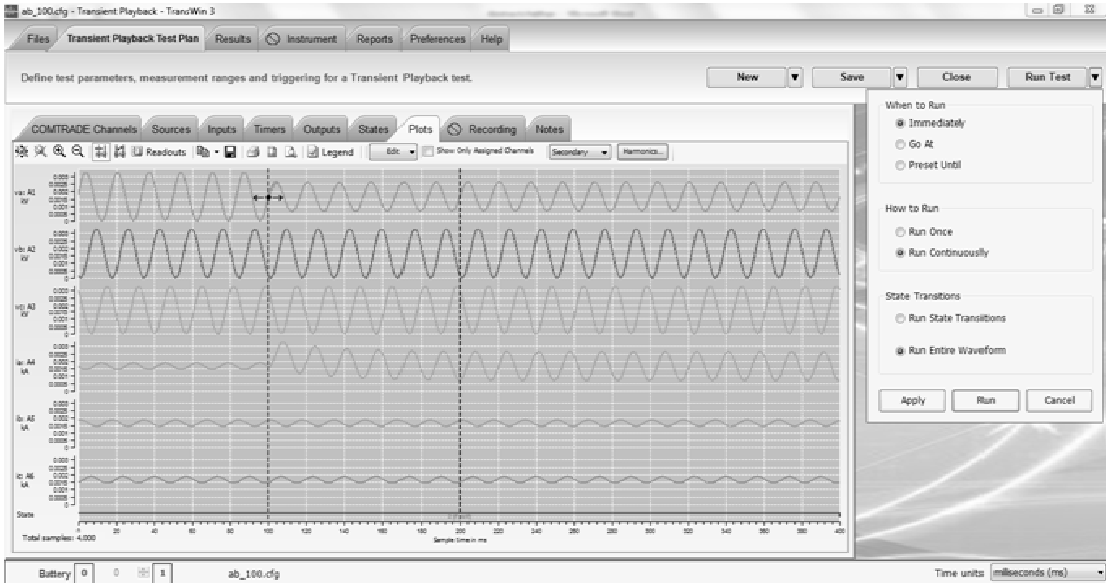


Figure D.4: Real time playback configuration menu

7. The real time signal playback can be suspended either by clicking on the STOP button or by sensing trip signal from the relay under test. Later method is used in this work.

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3. Sham M.V. and Vittal K.P., Development of DSP based high speed numerical distance relay and its evaluation using hardware in loop power system simulator, Innovative Smart Grid Technologies−India (ISGT India), 2011 IEEE PES, 37−42, 2011
4. Sham M.V., Chethan K.S. and Vittal K.P., Development of adaptive distance relay for STATCOM connected transmission line, Innovative Smart Grid Technologies −India (ISGT India), 2011 IEEE PES, 248−253, 2011
5. Sham M.V. and Vittal K.P., STATCOM Connected Transmission Lines - A Case Study, Electrical India, vol. 52 No.9, pp120-126.

Curriculum Vitae

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Educational Qualification

Degree	Specialization	Name of the Insitute	University	Year
B.E.	Electrical and Electronics Engineering	J.N.N.College of Engineering,India	Kuvempu, India	1992-1996
M.Tech	Power and Energy Systems	Karnataka Regional Engineering college	Mangalore, India	1997-1999
Pursuing Ph.D	Electrical Engineering	NITK	Autonomous India	2010-till date

Work Experience

Post	Affiliation	Place	Year
Electrical Engineer	Sujaya Steel Industries	Shimoga, India	1996-1997
Junior Manager	Jindal Vijayanagar Steel Limited	Bellary, India	1999-2000
Lecturer	Government polytechnic college	Bhadravathi, India	2000-2005
Senior Grade Lecturer	-do-	-do-	2005-2010
Selection Grade Lecturer	-do-	-do-	2010-till date

Responsibilities held

- Coordinator for MODROBS implementation under AICTE(All India Council for Technical Education) scheme during 2003-2005.
- EDUSAT (satellite based distance learning) program coordinator during 2008-2010.

Subjects Taught

- Generation, Protection and Switch Gear
- Embedded Systems
- Power Electronics
- C programming

Areas of Research Interest

- FACTS applications to power systems
- Power system protection

Society Memberships

- Member of ISTE (Indian Society For Technical Education)
- Student member of IEEE

Computer Proficiency

- Operating Systems: Windows of all flavors and Linux (Ubuntu and Fedora)
- Programming Languages: FORTRAN, C/C++ and JAVA
- Simulation packages and other tools: MATLAB/SIMULINK, EMTDC/PSCAD, PSIM, Code Composer Studio, Keil and LABVIEW.

Exposure to Microprocessors/Microcontrollers and DSP

- Microprocessors : Intel 8085, Intel 8086.
- Microcontrollers : Motorola M68HC11, Intel 8051.
- DSP : TMS320LF2407A and TMS320F28335.

Interest and Activities

- Reading
- Listening music