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Space vector-based synchronised bus-clamping pulse width modulation algorithms for three-level voltage source inverter in overmodulation region

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Abstract: The main objective of the present work is to develop space vector-based synchronised bus-clamping pulse width modulation algorithms to improve total harmonic distortion and higher DC-bus utilisation of the three-level inverter in overmodulation region. The proposed algorithms can generate synchronised pulse width modulation waveforms with all possible pulse number preserving all the waveform symmetries. The results of the proposed algorithms are evaluated and compared with conventional space vector pulse width modulation algorithm. It is shown that the proposed algorithms give improved results in terms of total harmonic distortion and DC-bus utilisation than that of conventional one in overmodulation region. The proposed method is implemented and verified experimentally on a constant *v/f* drive fed from insulated gate bipolar transistor (IGBT)-based voltage source inverter using Motorola power PC-based embedded controller.

1 Introduction

Recently, multilevel inverters have established their importance in the area of high-power medium-voltage applications in industry [1–6]. The space vector pulse width modulation (SVPWM) is a projected modulation technique for multilevel inverters similar to two-level inverters. SVPWM techniques generally have the following features: good utilisation of DC-bus voltage, low current ripple and relatively easy hardware implementation either by a digital signal processor (DSP) or by an embedded controller. These features make it suitable for high-power applications. However, as the number of levels increases, the implementation of SVPWM is considered complex, owing to complex geometry of the space vector diagram, a large number of switching states, increased device switching lossess and voltage imbalance problems. These deficiencies restrict the number of levels to three in most of the industrial drive applications. Hence, three-level inverter is of interest for the present work. Three-level voltage source inverters (VSIs) [7–11] are being increasingly used in high-power, medium-voltage and high-performance applications in industry. The main reasons for the popularity of three-level inverters are because of improved output voltage performance, voltage level can be doubled using the semiconductor devices of similar voltage rating and can operate at lower switching frequency (f_s) compared to two-level inverters [11, 12]. However, in three-level inverter the increase in number of switching devices switching losses increases because of which overall reliability and efficiency of the inverter reduces [3]. Under such circumstances, the use of low f_s or pulse number P reduces the switching losses [13], but this in turn increases the harmonic distortion of the line voltage and motor current on the other hand [3]. The reduction of harmonic distortion at low f_s is still a challenging job for the researchers.

A new SVPWM method for three-level inverter, with an ability to reduce the switching loss at least by 33%, is presented in [14, 15]. Narayanan proposed three space vector-based bus-clamping PWM (BCPWM) algorithms, basic bus-clamping strategy-1 (BBCS-1) with $P = 7, 11, 15, \ldots$, boundary sampling strategy-1 (BSS-1) and asymmetric zero-changing strategy (AZCS) with $P = 5, 9, 13, \ldots$ have been reported in [16, 17]. Two novel synchronised bus-clamping PWM strategies, namely basic bus-clamping strategy-2 (BBCS-2) with $P = 5, 9, 13, \ldots$ and boundary sampling strategy-2 (BSS-2) with $P = 7, 11, 15, \ldots$ [18] and advanced bus-clamping PWM techniques [19] based on space vector approach for high-power drives for two-level inverter. Although the algorithms proposed in [18, 19] for two-level inverter, extending it to three-level inverter in overmodulation region is not straight forward. This paper proposes three-vector bus-clamping algorithm(TVBCA) and four-vector bus-clamping algorithm (FVBCA) for both odd and even number of samples/sector (N) and studies the effect of switching sequences on the performance of the three-level inverter. The results are compared in terms of fundamental component and total harmonic distortion (THD) of the line voltage and motor current THD with conventional SVPWM (CSVPWM).

2 Space vector approach to bus-clamping algorithm

The space vectors and switching states of three-level inverter in stationary($\alpha - \beta$) reference frame is shown in Fig. 1. The

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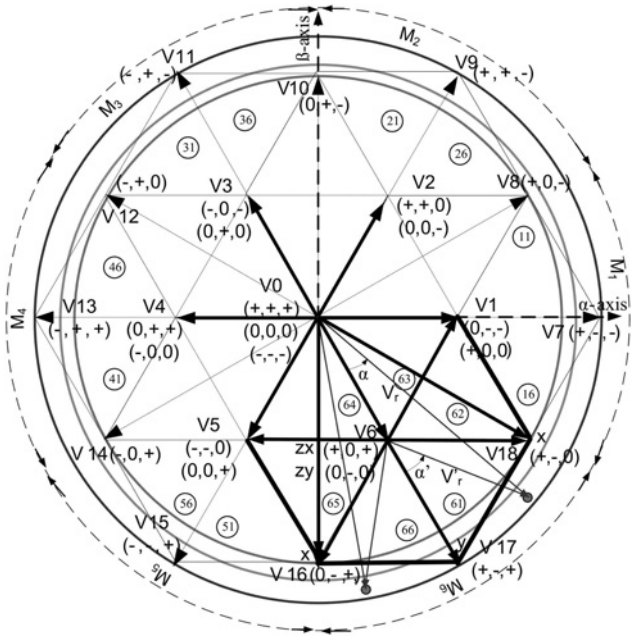

Fig. 1 *Space vector diagram and switching vectors of three-level inverter in stationary reference frame*

vector space is divided into six equal major sectors $M_1 - M_6$ and each major sector is subdivided into six minor sectors 61, 62, 63, 64, 65 and 66 in M_6, for example. In Fig. 1, there are $3^3 = 27$ switching states: three zero-vector states $V_0(+++, 000, ---)$ known as zero-states, 12 small-vector states $V_1(+00,\ 0--)$, $V_2(++0,\ 00-)$, $V_3(0+0, -0-)$, $V_4(0++,\ -00)$, $V_5(00+,\ --0)$, $V_6(+0+,\ 0-0)$, six medium-vector states $V_8(+0-)$, $V_{10}(0+-)$, $V_{12}(-+0)$, $V_{14}(-0+)$, $V_{16}(0-+)$, $V_{18}(+-0)$ and six large-vector states $V_7(+--)$, $V_9(++-)$, $V_{11}(-+-)$, $V_{13}(-++)$, $V_{15}(--+)$, $V_{17}(+-+)$ known as active states.

The space vectors associated with three-level inverter and its two-level transformation in major sector (M_6) is shown in Fig. 1. The reference vector is sampled once in every sample T_s and the position of the sampled reference vector $\boldsymbol{V}_r$ is located by time averaging of the three nearest vectors generated by the inverter using (1).

$$\begin{aligned} \boldsymbol{V}_r T_s &= \boldsymbol{V}_x T_x + \boldsymbol{V}_y T_y + \boldsymbol{V}_z T_z \\ T_s &= T_x + T_y + T_z \end{aligned} \tag{1}$$

where T_x, T_y and T_z are the dwell times of $\boldsymbol{V}_x$, $\boldsymbol{V}_y$ and $\boldsymbol{V}_z$, respectively.

In conventional space vector approach to PWM, an equal division of T_z between two zero states results in lesser ripple current [20, 21]. The vector sequence $V_{6zx}V_{17}V_{18}V_{6zy}$ and $V_{6zy}V_{18}V_{17}V_{6zx}$ in minor sector 66, and $V_{6zy}V_{16}V_{17}V_{6zx}$ and $V_{6zx}V_{17}V_{16}V_{6zy}$ in minor sector 61 are used for equal division of T_z in M_6. The space vector approach to bus-clamping algorithm (BCA) gives flexibility in switching two phases once and clamping one phase or clamping two phases and switching one phase twice [18] or switching phase-1 twice, phase-2 once, and clamping phase-3 in every sample or subcycle. In M_6 depending on the selection of vectors V_{6zx} and V_{6zy} BCA is classified into two basic types: 60° and 30° clampings shown in Fig. 2. In each sample, one zero vector and two active vectors are used in the sequences $V_{6zx}V_{16}V_{17}$ and $V_{17}V_{16}V_{6zx}$ (60° clamping) in 66,

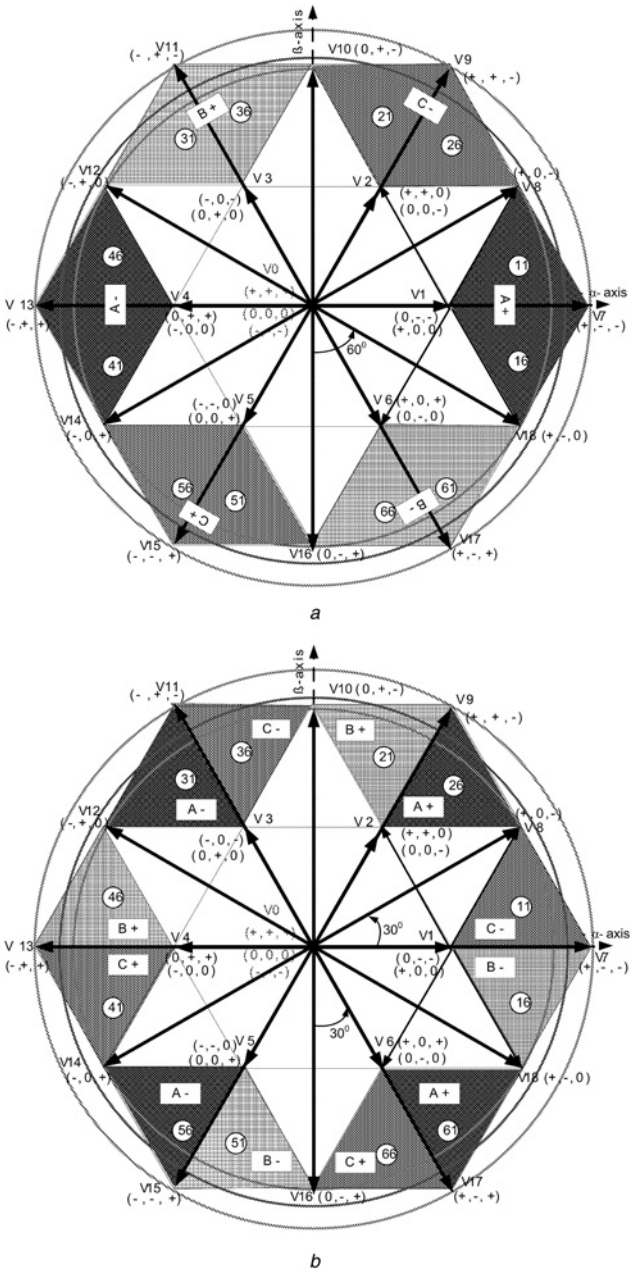

Fig. 2 *Basic types of bus clamping algorithm in three-level inverter*

a 60° clamping
b 30° clamping

and $V_{6zy}V_{18}V_{17}$ and $V_{17}V_{18}V_{6zy}$ (30° clamping) in 61. The sequences like $V_{6zx}V_{16}V_{17}V_{16}$ and $V_{16}V_{17}V_{16}V_{6zx}$ (60° clamping) in 66, $V_{6zy}V_{18}V_{17}V_{18}$ and $V_{18}V_{17}V_{18}V_{6zy}$ (30° clamping) in 61 uses one zero vector with equal division of T_x or T_y between any one of the two active vectors. In M_6 for any given sample out of two clampable phases, either phase-B clamped to the '−' DC-bus or phase-A clamped to the '+' DC-bus and phase-C is unclamped, it can be switched for any transition between two active vectors. If the intial vector state in M_6 is V_{6zx} or V_{6zy}, then each phase must switch an odd number of times within that major sector. If it is an active state V_{16} or V_{17} or V_{18} then only phase-C must switch an odd number of times, while phase-A and phase-B must switch an even number of times and the total number of switchings of all the three phases must be an odd within that major sector [18].

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3 Proposed bus-clamping algorithms

The main objective here is to propose bus-clamping algorithms for three-level inverter to improve THD and higher DC-bus utilisation in overmodulation region. Two new bus-clamping algorithms developed are explained in the Sections 3.1 and 3.2. Based on the placement of N in M_6 four groups have been formed, Group-1, Group-2, Group-3 and Group-4. The pulse number P is the total number of switchings of the three phases in a major sector for one cycle.

3.1 3-Vector bus-clamping algorithm

In this algorithm three nearest vectors are used for the generation of PWM waveforms. The vector switchings are: $V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ leads to 60° clamping or $V_{6zy} \Leftrightarrow V_{18} \Leftrightarrow V_{17}$ leads to 30° clamping in 61 and $V_{6zy} \Leftrightarrow V_{16} \Leftrightarrow V_{17}$ leads to 30° clamping or $V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{6zy}$ leads to 60° clamping in 66.

In Group-1, $N = 2, 6, 10, \ldots$ odd samples ($N/2$) are placed in 66 and 61 of M_6 respectively, $P = 2, 6, 10, \ldots, N$. If V_{6zx} be the initial state of M_6, then the sequences $V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ must be used for the first $N/2$ samples in 61 and sequences $V_{6zy} \Leftrightarrow V_{17} \Leftrightarrow V_{16}$ for the last $N/2$ samples in 66. In this case one of the unclampable phase and the clampable phase must switch an odd number of times, the other must switch an even number of times. The total number of switchings of the three phases must be even within that major sector.

In Group-2, $N = 3, 7, 11, \ldots$ one sample is placed on the boundary of 61 in the middle of M_6, odd samples[$(N-1)/2$] are placed in 66 and 61of M_6, respectively, $P = 4, 10, 16, \ldots, (3N-1)/2$. If V_{6zx} be the initial state of M_6, then the sequences for first $(N-1)/2$ and last $(N-1)/2$ must be similar to Group-1. The sequences for the middle sample must be $V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{17}$ or $V_{17} \Leftrightarrow V_{6zx} \Leftrightarrow V_{17}$. In this group, all the clampable phases must switch an odd number of times, the clampable phase must switch an even number of times and the total number of switchings of the three phases must be even in the major sector.

In Group-3, $N = 4, 8, 12, \ldots$ even samples ($N/2$) are placed in 66 and 61 of M_6, respectively, $P = 5, 11, 17, \ldots, (3N-2)/2$. If V_{6zx} be the initial state of M_6, then the sequences $V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ must be used for the first $N/2$ samples in 61 and sequences $V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{6zx}$ for the last $N/2$ samples in 66. Here, one of the two clampable phase must switch an even number of times, the other must switch an odd number of times and the unclampable phase must switch an odd number of times. The total number of switching of the three phases must be even within the major sector.

In Group-4, $N = 5, 9, 13, \ldots$ one sample is placed on the boundary of 61 in the middle of M_6, even samples [$(N-1)/2$] are placed in 66 and 61 of M_6, respectively, $P = 7, 15, 23, \ldots, (4N-6)/2$. If V_{6zx} be the initial state of M_6, then the sequences for first $(N-1)/2$ and last $(N-1)/2$ must be similar to Group-3. The sequences for the middle sample must be similar to Group-2. In this group the two clampable phase must switch same number of times as that of Group-3, the unclampable phase must switch an odd number of times. The total number of switching of the three phases must be even within the major sector.

The details of vector switching possibilities and dwell times of TVBCA is given in Fig. 3*b*.

3.2 4-Vector bus-clamping algorithm

This algorithm uses one zero vector and two active vectors with equal division of one of the active vector dwell times T_x or T_y for the generation of PWM waveforms. Since one of the active vector appear twice for a given N and hence the name 4-vector bus-clamping algorithm. The vector switching sequences used in this algorithm are: $V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18} \Leftrightarrow V_{17}$ leads to 60° clamping or $V_{6zy} \Leftrightarrow V_{18} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ leads to 30° clamping in 61 and

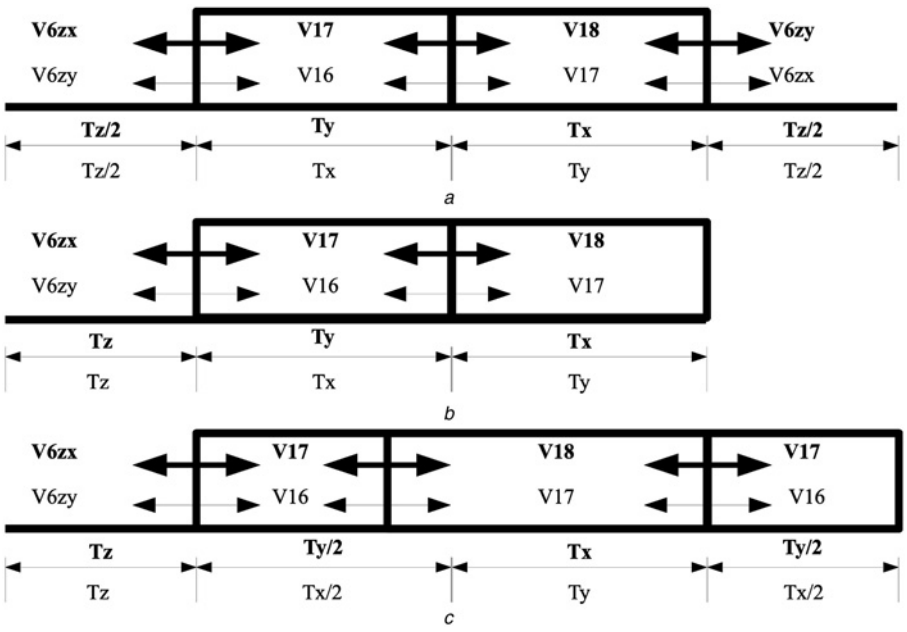

Fig. 3 *Details of switching vector sequences and dwell times in M_6*

a CSVPWM
b TVBCA
c FVBCA

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$V_{6zy} \Leftrightarrow V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{16}$ leads to 30° clamping or $V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{16} \Leftrightarrow V_{6zy}$ leads to 60° clamping in 66.

In Group-1, $N = 2, 6, 10, \ldots$ odd samples ($N/2$) are placed in 66 and 61 of M_6, respectively, $P = 3, 9, 15, \ldots, 3N/2$. If V_{6zy} be the initial state of M_6, then the sequences $V_{6zy} \Leftrightarrow V_{18} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ must be used for the first $N/2$ samples in 61 and sequences $V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{16} \Leftrightarrow V_{6zy}$ for the last $N/2$ samples in 66. In this case two unclampable phases must switch an equal and odd number of times and no switchings in the clampable phase. The total number of switchings of the three phases must be even within that major sector.

In Group-2, $N = 3, 7, 11, \ldots$ one sample is placed on the boundary of 61 in the middle of M_6, odd samples($(N-1)/2$) are placed in 66 and 61 of M_6, respectively, $P = 5, 13, 21, \ldots, (4N-2)/2$. If V_{6zy} be the initial state of M_6, then the sequences $V_{18} \Leftrightarrow V_{17} \Leftrightarrow V_{18} \Leftrightarrow V_{6zy}$ must be used for the first $(N-1)/2$ samples in 61 and the sequences $V_{6zy} \Leftrightarrow V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{16}$ for the last $(N-1)/2$ samples in 66. The sequence for the middle sample must be $V_{17} \Leftrightarrow V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$. In this case one of the clampable phase and the unclampable phase must switch an equal and even number of times and the other clampable phase must switch an even number of times. The total number of switchings of the three phases must be even within that major sector.

In Group-3, $N = 4, 8, 12, \ldots$ even samples($N/2$) are placed in 66 and 61 of M_6, respectively, $P = 7, 15, 23, \ldots, (4N-2)/2$. If V_{6zx} be the initial state of M_6, then the sequences $V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18} \Leftrightarrow V_{17}$ or $V_{6zy} \Leftrightarrow V_{18} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ must be used for the first $N/2$ samples in 61 and the sequences $V_{6zy} \Leftrightarrow V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{16}$ for the last $N/2$ samples in 66. In this case one of the clampable phase and the unclampable phase must switch an equal and even number of times and the other clampable phase must switch an even number of times. The total number of switchings of the three phases must be even within the major sector.

In Group-4, $N = 5, 9, 13, \ldots$ one sample is placed on the boundary of 61 in the middle of M_6, even samples($(N-1)/2$) are placed in 66 and 61 of M_6, respectively, $P = 8, 16, 24, \ldots, 2(N-1)$. If V_{6zy} be the initial state of M_6, then the sequences $V_{17} \Leftrightarrow V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$ must be used for the first $(N-1)/2$ samples in 61 and the sequences $V_{6zy} \Leftrightarrow V_{16} \Leftrightarrow V_{17} \Leftrightarrow V_{16}$ for the last $(N-1)/2$ samples in 66. The sequence for the middle sample must be $V_{17} \Leftrightarrow V_{6zx} \Leftrightarrow V_{17} \Leftrightarrow V_{18}$. In this case one of the clampable phase and the unclampable phase must switch an equal and even number of times and the other clampable phase must switch an even number of times. The total number of switchings of the three phases must be even within that major sector.

The details of vector switching possibilities and dwell times of FVBCA is given in Fig. 3*c*.

3.3 Overmodulation region

The region ($0.866 < M_i \leq 1$) between the inner most circle and outmost circle in Fig. 1 is defined as overmodulation region [22]. In two-level inverter the overmodulation region is divided into two zones, namely overmodulation region-1 ($0.907 < M_i \leq 0.952$) and overmodulation region-2 ($0.952 < M_i \leq 1$) [23], the same region-1 and region-2 definition is extended to three-level inverter in [10]. The boundary between overmodulation region-1 and overmodulation region-2 in [11, 24] is 0.9535 as the medium vectors are not considered. In the present work the medium vectors are also considered and with this approach the boundary between overmodulation region-1 and overmodulation region-2 is different for different N. The boundary between overmodulation region-1 and overmodulation region-2 for $N = 2$ is 0.8965, for $N = 3,4$ and 5 the boundaries are 0.8793, 0.9373 and 0.9105, respectively.

In overmodulation region, only the tip of the $\boldsymbol{V}_r$ belongs to minor sectors 66 and 61 as shown in Fig. 1. Hence only these two minor sectors are of interest for the proposed work. The dwell times for minor sectors 66 and 61 are calculated using (2) and (3), respectively, and because of symmetry these equations are valid for all the other major sectors M_1 to M_5.

$$\begin{aligned} T_x &= 2.309 V'_{r\beta} T_s \\ T_y &= (2V'_{r\alpha} - 1.1547 V'_{r\beta}) T_s \\ T_z &= T_s - (T_x + T_y) \end{aligned} \tag{2}$$

$$\begin{aligned} T_x &= -2.309 V'_{r\beta} T_s \\ T_y &= (2V'_{r\alpha} + 1.1547 V'_{r\beta}) T_s \\ T_z &= T_s - (T_x + T_y) \end{aligned} \tag{3}$$

3.4 Premodulation

At the begining of overmodulation region-1 $V'_r = 0.433$. When V'_r is increased beyond 0.433 the tip of the two premodulated samples adjacent to the middle one as shown in Fig. 4*a* touch the hexagon. In the case of $N =$ odd one sample placed on the middle of any given major sector do not saturate and for $N =$ even no sample placed on the middle of the major sector. In order to reduce the complexity of the diagram $N = 3$ is considred for analysis. In major sector M_1, first sample is placed in minor sector 16 at an angle of $\alpha = -20°$, middle sample and the last sample are placed in minor sector 11 at an angle of $\alpha = 0°$ and 20°, respectively. The magnitude of two premodulated samples do not increase further with increase in V'_r which means saturates. In such case, no zero vector is used in these samples and because of the non-application of zero vector the number of switching reduces and pulse dropping starts. In order to prevent pulse dropping the magnitude of those samples which fall outside the hexagon needs to be corrected using (4).

$$\begin{aligned} V'_{rp} &= V'_r \quad \text{if } V'_r \leq V'_{rm} \\ &= V'_{rm} \quad \text{if } V'_r > V'_{rm} \\ V'_{rm} &= \frac{0.433}{\cos(\pi/6 - \alpha')} \\ \alpha'_p &= \alpha' \end{aligned} \tag{4}$$

In overmodulation region-2 the modulation index is increased by shifting the average vectors generated closer to their nearest subsector boundaries. In Fig. 4*b*, the samples which are closer to V_7 in 11 are moved towards vector V_7 and the samples which are closer to V_8 are pushed towards medium vector V_8. Similarly in 16, the samples which are closer to V_7 are moved towards vector V_7 and those vectors closer to medium vector V_{18} are pushed towards medium vector V_{18}. This is achieved by the amplitude correction as in

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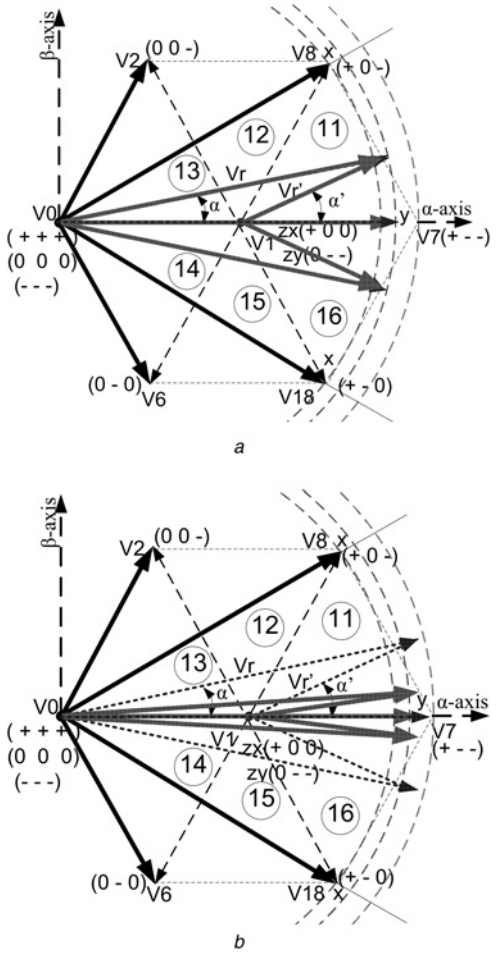

Fig. 4 *Sample placement in major sector (M_1) for $N = 3$ dotted lines (before) and solid lines (after) premodulation*

a Overmodulation region-1
b Overmodulation region-2

overmodulation region-1 and angle correction using (5) with an angle correction factor α_a which decreases from 1 to 0. When $\alpha_a = 0$ all the samples lay on the inner edges of minor sectors 11 and 16, at this point three-level inverter looses its multilevel characteritics and behaves like two-level inverter.

$$\begin{aligned} \alpha'_p &= \alpha_a \alpha' \quad \text{if } 0^0 \le \alpha' < \frac{\pi}{6} \\ &= \frac{\pi}{6} \quad \text{if } \alpha' = \frac{\pi}{6} \\ &= \frac{\pi}{3} - \alpha_a\left(\frac{\pi}{3} - \alpha'\right) \quad \text{if } \frac{\pi}{6} < \alpha' < \frac{\pi}{3} \\ V'_{rm} &= \frac{0.433}{\cos(\pi/6 - \alpha')} \end{aligned} \tag{5}$$

4 Results and discussion

Synchronised bus-clamping PWM algorithms for three-level VSI in overmodulation region are simulated using MATLAB/SIMULINK and applied to a constant *v/f* drive consists of a 400 V, 1.1 kW, 1500 rpm, $3-\Phi$ induction motor powered from a three-level IGBT-based inverter. The complete control system runs on the DS1104 R&D controller board residing in a peripheral component interconnect (PCI) slot of host computer. The board features a floating-point MPC8240 power PC processor and is completed with MATLAB/SIMULINK and real time interface software tools. The proposed algorithm is written in C language using MATLAB editor and is linked to the SIMULINK environment to carry out building process, where the program is compiled using Microtec C compiler, linked with libraries and finally generates .sdf file which will be downloaded on to the board. The drive runs at no load condition at different values of M_i in the overmodulation region. In each case, phase voltage, line voltage and the motor current waveform data are stored using LeCroy make Wave Runner digital storage oscilloscope with 200 MHz bandwidth at a sampling rate of 10 G samples/s. One cycle data are extracted from the data stored for the analysis of the fast fourier transform (FFT) spectrum of the waveforms. The harmonic components are computed using FFT function in MATLAB.

The experimental waveforms of phase voltage (V_{An}), defined as the voltage between output terminal and the neutral point of the inverter, line voltage between two phases (V_{AB}) and no load motor current (i_A) of phase-A are given in Fig. 5*a*(C1–C3). Respectively, for $N = 4$ in

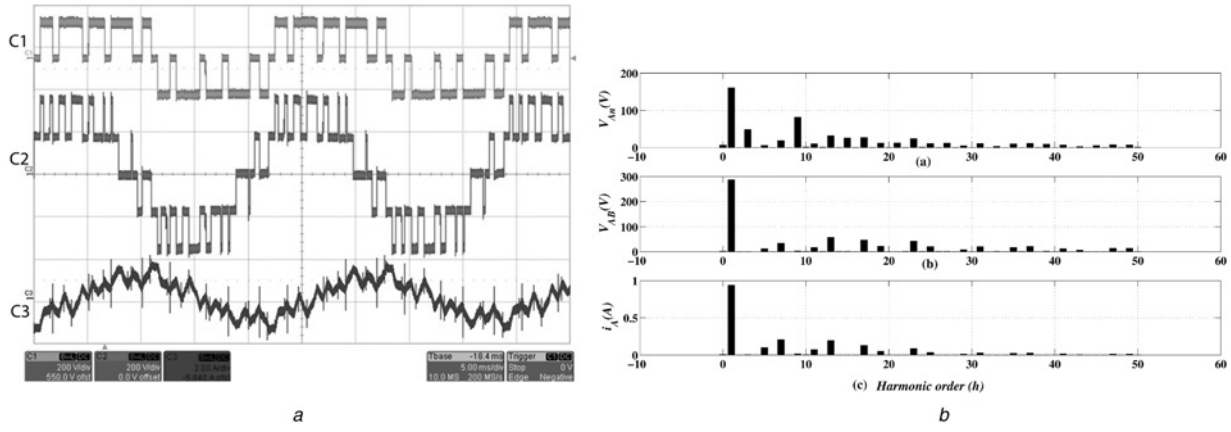

Fig. 5 *Experimental waveforms of phase voltage (V_{An})*

a Experimental waveform of (C1) $V_{An}(V)$ (C2) $V_{AB}(V)$ (C3) $i_A(A)$
b Harmonics spectrum of (a) V_{An}, (b) V_{AB}, (c) i_A for $N = 4$ at $M_i = 0.88$ for FVBCA

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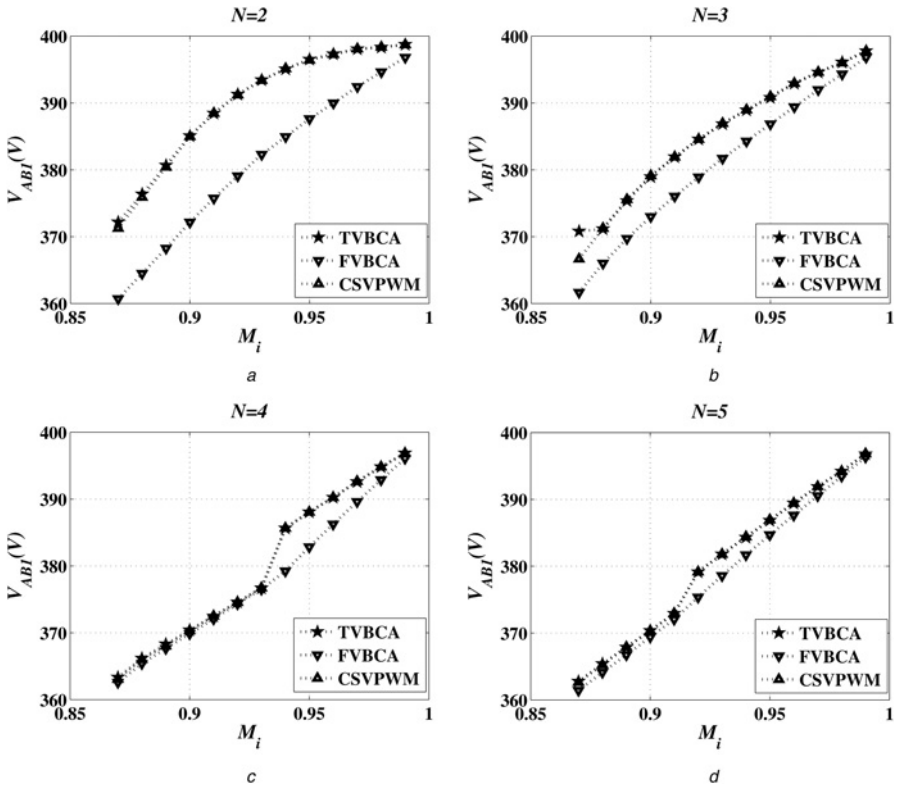

Fig. 6 *Comparison plot of V_{AB1} against M_i for different N*

a V_{ABI} against M_i for $N = 2$
b V_{ABI} against M_i for $N = 3$
c V_{ABI} against M_i for $N = 4$
d V_{ABI} against M_i for $N = 5$

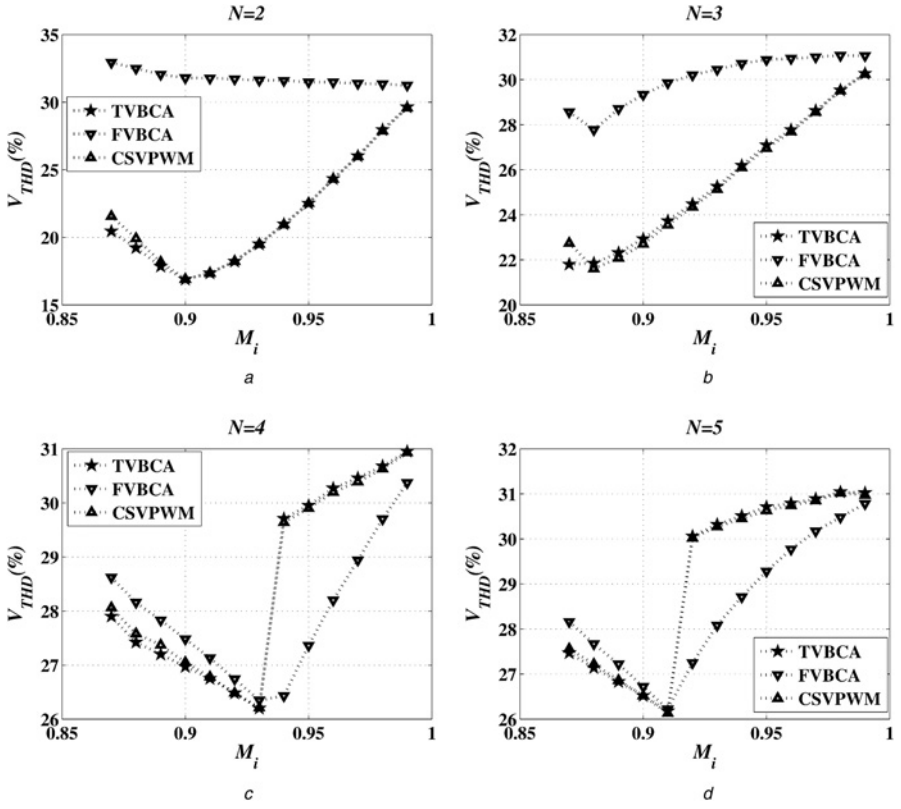

Fig. 7 *Comparison plot of V_{THD} against M_i for different N*

a V_{THD} against M_i for $N = 2$
b V_{THD} against M_i for $N = 3$
c V_{THD} against M_i for $N = 4$
d V_{THD} against M_i for $N = 5$

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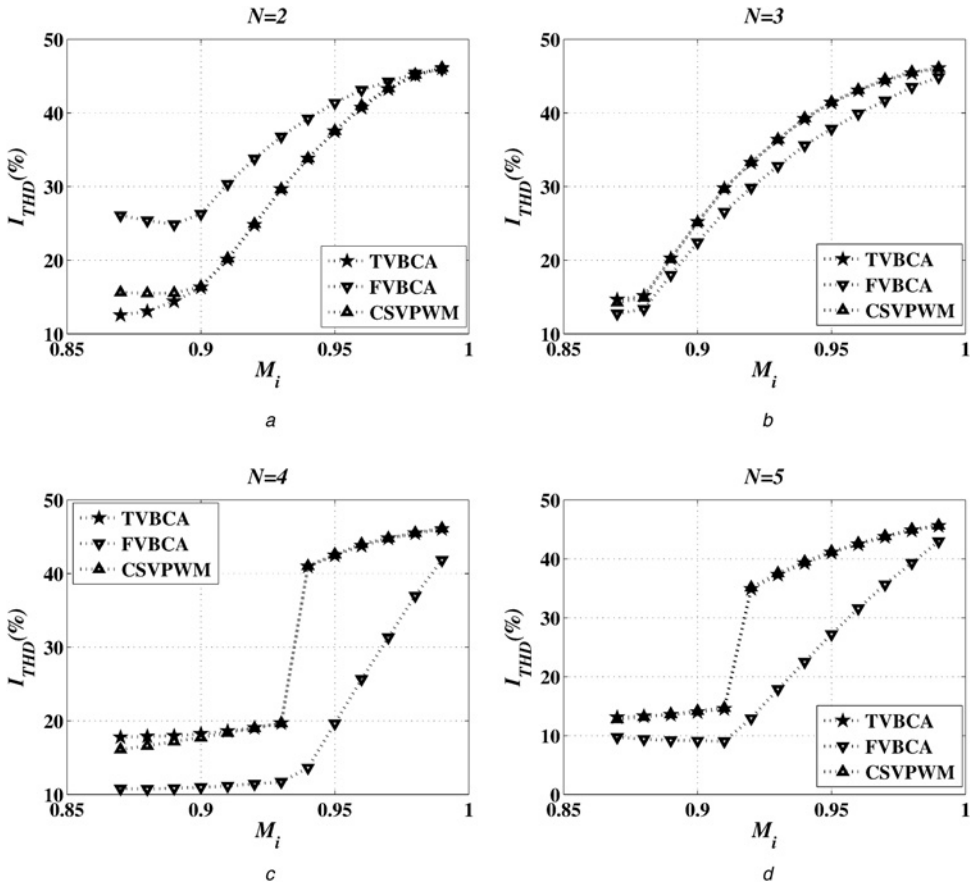

Fig. 8 *Comparison plot of I_{THD} against M_i for different N*

a I_{THD} against M_i for $N = 2$
b I_{THD} against M_i for $N = 3$
c I_{THD} against M_i for $N = 4$
d I_{THD} against M_i for $N = 5$

overmodulation region-1 at $M_i = 0.88$. Their corresponding harmonic spectrums are given in Fig. 5*b*(a)–(c), respectively. The waveforms exhibit synchronisation and symmetry. The FFT plots demonstrate the absence of even harmonics which means half wave symmetry (HWS). The triplen harmonics are present in the phase voltage [plot (a) in Fig. 5*b*], and they are cancelled in line voltage [plot (b) in Fig. 5*b*)] and motor current [plot (c) in Fig. 5*b*], because of three phase symmetry (TPS).

The performance of the inverter is measured in terms of voltage THD (V_{THD}) of V_{AB} and current THD (I_{THD}) of i_{A}. The parameters V_{THD} and I_{THD} against M_i for the proposed algorithms with normal pulse number before pulse dropping (P_{bpd}) are compared with CSVPWM. The proposed algorithms TVBCA with $P_{\mathrm{bpd}} = 2$, 4, 5, 7 and FVBCA with $P_{\mathrm{bpd}} = 3$, 5, 7, 8 are considered for the performance analysis against CSVPWM with $P_{\mathrm{bpd}} = 3$, 4, 6, 7 for $N = 2$, 3, 4 and 5, respectively. The comparative results are given in Figs. 6*a*–*d* fundamental component of the line voltage (V_{AB1}) against M_i, Figs. 7*a*–*d* V_{THD} against M_i and Figs. 8*a*–*d* I_{THD} against M_i for $N = 2$, 3, 4 and 5.

In Figs. 6*a*–*d* V_{AB1} of TVBCA is higher than FVBCA and slighly higher than CSVPWM for the entire overmodulation region. The relation between V_{AB1} and M_i is almost linear, in certain portion of overmodulation region V_{AB1} is equal in TVBCA and CSVPWM for $N = 2$, 3, 4, 5 and equal in all three methods in case of $N = 4$ and 5 upto $M_i = 0.93$ and 0.91, respectively. In Figs. 7*a* and *b* there is an improvement in V_{THD} for lower P_{bpd} which means reduction in switching losses. In Figs. 7*c* and *d* in overmodulation region-1 there is an improvement in lower P_{bpd} and in case of overmodulation region-2 FVBCA gives improved V_{THD}. It can be seen from Fig. 8*a* that TVBCA gives lesser harmonic distortion and I_{THD} is equal in certain portion for TVBCA and CSVPWM. In Figs. 8*b*–*d*, FVBCA result in improved harmonic distortion compared to TVBCA and CSVPWM.

5 Conclusions

Space vector-based synchronised bus-clamping PWM algorithms for three-level VSI in overmodulation region are proposed. The results are compared with conventional space vector PWM. It is shown from the results that the proposed algorithm gives higher fundamental voltage with improved THD. The two algorithms together can generate PWM waveform with odd and even pulse number. In constant *v*/*f* drives where the inverters operate at low switching frequencies the proposed algorithms can be used either to minimise switching losses (using TVBCA) at lower pulse number, or to reduce harmonic distortion (using FVBCA) at higher pulse number.

The harmonic spectrum of the experimental results shows the absence of triplen harmonics in line voltage and motor current, this ensures that synchronisation, quaterwave symmetry, half wave symmetry and three phase symmetries are maintained in the waveform.

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