PERFORMANCE OF A BOOST MULTI-LEVEL INVERTER FOR MINING APPLICATIONS

Thesis

Submitted in partial fulfilment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled **"Performance of a boost multi level inverter for mining applications"** which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy in **Mining Engineering** is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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(N V V Prudhvi Krishna B)

ABSTRACT

In recent, much advancement has been witnessed in the field of drive systems. Electrical variable speed drives (VSDs) are integral to mineral processing and mining. VSDs are widely used in **mining, drilling, traction, air compressors, water pumps, and conveyors**. In fact, drives are back bone for any application, In the field of mining, drilling, traction systems drives are the only important parts of the entire control units. In this regard, the inner structure of drive i.e., inverter is key unit for the same. In the present study a novel inverter structure is designed for different mining, traction and conveyor applications. Although applications are plenty but still the proposed inverter is capable to meet the aforesaid applications.

The back ground of drives system is that, for many years DC motors were used in mining applications. Steadily those motors are being replaced with AC motors due to several advancements in the AC drive technology. In addition to better control, AC motors require less maintenance than DC motors. Thus, controlling AC motors with drive system is a challenging issue. This aspect is key for new research and developments in the field of drives. Although voltage control and current control drives exists, still VSD's have their own functions and features in terms of utilization.

Traditionally VSDs are the part of the drive systems, VSD's are mainly based on the conventional voltage source inverters (VSIs). Nevertheless, the conventional VSIs suffer from the barriers like output voltage limitations, harmonics, and control complexities. Since the loads are variable in the mining applications, continuous and reliable power converters are much needed. Multilevel inverters (MLIs) have become a promising alternative to conventional VSIs due to efficiency, ample power capacity, high-quality injected currents, and less complexity. Most of the available MLIs possess unity or stepped-down voltage feature. In such cases, a front-end boosting stage or step-up transformer at the output is used to meet the voltage requirement. Using MLIs with inherent boosting ability in such a scenario is more logical. Capacitor-based MLIs with boosting ability and self-voltage balancing are termed switched capacitor MLIs (SC-MLIs).

Likewise, MLI topologies presented in this thesis amplify the voltage level using a single dc source. These units can be cascaded to produce higher levels by considering a proper choice of the magnitude of the multiple dc sources.

The motivation of this research work is to emanate a novel switched-capacitor-based boost MLI for mining and drilling applications. In particular, the proposed inverter is designed for

nine-levels by using two capacitors as virtual sources. To support the proposed configurations, detailed operating principles, modulation, and real time results are presented. The Proposed MLIs is capable to generate large number of levels with a single source if it extended further. However, to achieve nine levels only 11 switches and 2 capacitors are used and this enables the proposed topology in compact and efficient manner.

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NOMENCLATURE

MLI	Multi Level Inverter
SSHB	Single Stage Hexad Boost
DB-MLI	Dual Boost Multi Level Inverter
PD-PWM	Phase Disposition Pulse Width Modulation
SCMLI	Switched Capacitor Multi Level Inverter
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
MDPWM	Modified Discontinuous Pulse Width Modulation
THD	Total Harmonic Distortion
CMV	Common Mode Voltage
DMV	Differential Mode Voltages
VSD	Variable Speed Drive
VSI	Voltage Source Inverter
EMI	Electro Magnetic Interference
DCI	Diode Clamped Inverter
IGBT	Insulated Gate Bipolar junction Transistor
GTO	Gate Turnoff Thyristors
NPC	Neutral Point Clamped

CHAPTER 1
INTRODUCTION

Introduction

Chapter one provides an overview, features, topological aspects, and common issues encountered when applying electric drives to underground mines. Additionally, the advantages of different drive systems are discussed as well as challenges in the present scenario with a critical review of emerging inverter topologies. Finally, the thesis research objectives and organization are discussed.

1.1 Overview of High-Power Converters

In the mid-1980s, gate turn-off (GTO) thyristors with 4500V gate voltage became commercially available,(Rizzo and Zargari 2004) which led to the evolution of medium-voltage (MV) and high-power converter drives. By replacing two-level voltage source inverters with MLIs, conventional inverters are generally displaced by two-level inverters. During the last two decades, high-power semiconductors (Brunner et al. 1997, Steimer et al. 1999) have made MLIs more popular. A wide range of industrial applications are powered by several high-power converters that have been developed and commercialized in the past. MV drives can have power ratings ranging from 0.4 to 40 MW at medium voltage levels between 2.3 and 13.8 kV. When load-commutated inverters are used with synchronous motor drives, this power rating can be increased to 100 MW (Bhatia et al.1998). Despite this, most MV drives installed today have voltage ratings between 3.3 and 6.6 kV and are rated for 1-4 MW (W.C et al.1998) According to a market study, fans, pumps, conveyors, and compressors account for 85% of MV drives. (Menz et al.2002,B.P et al.2001).In most cases, standard MV drives will meet the technical requirements for these drives, As shown in Table 1.1, commercially available semiconductors have voltage and current ratings. Other semiconductors included in this table are the static induction thyristor (SIT), the emitter turn-off thyristor (ETO), and the MOS-controlled thyristor (MCT). The fact remains that high-power applications have not benefited greatly from them. MV semiconductor switches cannot operate at higher voltages individually because they are available in the MV range. The operating voltage of power converters can be

increased by connecting MV semiconductors in series. It is possible that semiconductors connected in series and their gate drivers will not perform in the same way statically and dynamically. When blocking modes and transients occur, the inverse voltage may not be shared equally between these series-connected devices.

Table 1.1 An overview of the semiconductor market

Rating	Power diode	Thyristor	GTO	GCT/IGCT/ SGCT	IGBT
Maximum voltage	8.5 kV at 1.2 kA	12 kV at 1.5 kA	6 kV at 6 kA	10 kV at 1.7 kA	6.5 kV at 0.75 kA
Maximum current	9.6 kA at 1.8 kV	5 kA at 0.4 kV	6 kA at 6 kV	5 kA at 4.5 kV	2.4 kA at 1.7 kV

If blocking modes are to be achieved with equal voltage sharing, a separate equalization circuit is required. As a result of the additional voltage equalization circuit, (Rodriguez et al., 2009b). The converter experiences power losses. As well as being standard products, medium voltage inverters in the megawatt range belong to drive systems and energy conversion systems in conjunction with other components. Drive systems (K.H et al., 2004) and power converters must provide different performance features based on the applications in various industry sectors. Additionally, converter circuits have to be adapted to different types of motors, such as DC motors, induction motors, and synchronous motors - with permanent magnets or separately excited. In order to meet economic requirements, different circuit topologies have been developed, such as cyclo converters, matrix inverters, voltage source inverters, cellular inverters, current source inverters, and load-commutated inverters. This is achieved by examining the available power semiconductors, their maximum voltages and currents, as well as their turn-off capabilities. By continuously improving semiconductor elements, gating circuits, cooling methods, insulation materials, or cooling methods, drive converters may be improved. Due to this, certain circuit topologies are permanently displaced from one another.

There are many applications for variable speed drives in the megawatt range in different sectors, such as basic material industry, energy, and ship propulsion. An overview of converter applications by industry branch and power range is shown in

Table 1.2. For power grid energy conversion applications, this table includes non-rotating converters, but not traction converters.

1.2 Traditional Drive systems and applications

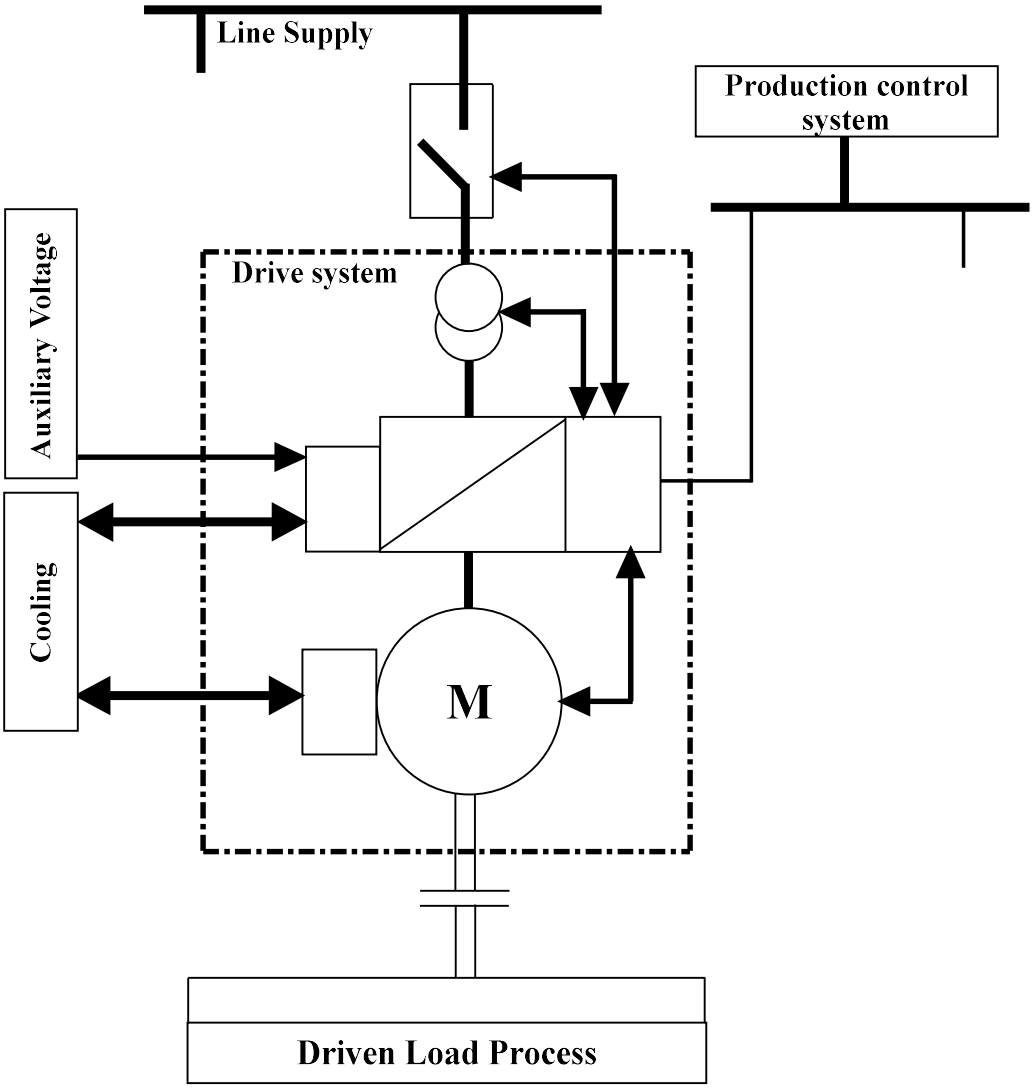


Figure 1.1 Components of Megawatt Drive Systems

1.2.1 Motors used in Mining

Figure1.2 Few Motors used in mining.

Table 1.1(a) Different motors Speed and Horse Power

S.No.	Horse Power(HP)	Speed(RPM)
1	5 HP	1750rpm
2	5.4 HP	1430rpm
3	6 HP	1500rpm
4	7.5 HP	1440rpm
5	10 HP	1760rpm

Motors designed for the demanding environment of mining operations i.e., drilling conveyors and traction. (B.P et al., 2001). These motors having different number of specifications depending upon the place of usage and are given below

1.2.2 Drives in conveyor belts

Figure 1.3 Drives in conveyor belts

1.2.3 Drilling machine

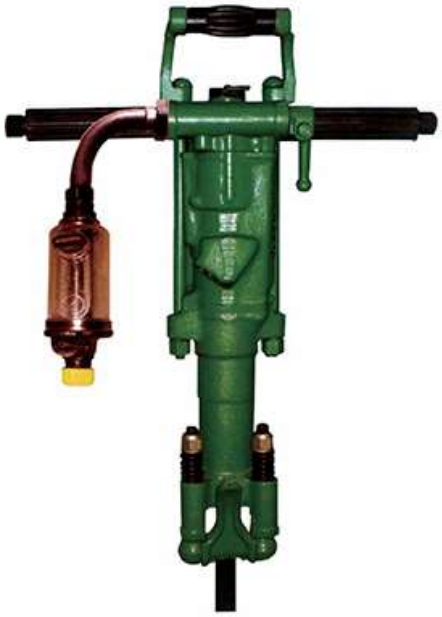


Figure 1.4 Drilling machine

Figures 1.3 and 1.4 shows the induction machines for the mining applications. In Figure 1.3 the induction motor acts as conveyor belt and the rating of the machines are given in table 1(a). From Table 1.(a) different motor speeds are presented. However, in reality, such motor operates at different frequencies. Further, in Figure 1.4 shows the drilling machine for rock drilling operations. Details of the rock drill machines are given below and it is given as an frequency of operations should be is greater than 34 Hz. Weight of the same is given as 18 kg. In reality 18 kg machine is quite bulky for regular works. Moreover it has poor efficiency and thereby huge burden on cost of the system. Later, to operate such low-frequency system we need sophisticated drive addition to that voltage and current ratings are very high for the same.

Table 1.1 (b) Drilling machine Parameters

Weight (Kg)	18
Total Length (mm)	605
Working Pressure (Mpa)	0.4
Impact Frequency (Hz)	≥34
Air Consumption (L/s)	≤25

Drive inverters are typically purchased by system integrators, plant constructors, or machinery OEMs from the operating company, rather than through direct procurement. At present, there are no companies capable of producing the complete equipment entirely on their own. The decision to utilize a specific drive technology is made by system integrators, rather than being determined by the customers. Medium voltage drives are a project business because of the small quantities and complex decision process because of the small quantities.

a) Basic requirements for all medium voltage drives are:

1. The system demonstrates robustness, exceptional reliability, and high availability.
2. Line harmonics exhibit low levels.
3. The line does not generate reactive power.
4. Integration, use and maintenance are easy.

Table 1.2 Overview of converter applications

Industry Sector	Application	Power
Oil & Gas	Turbo compressors (Export gas, LNG gas, Pipelines, Gas storage, Air separation), Reciprocating Compressors, Centrifugal pumps	1-100 MW
Metals	Hot rolling mill drives (Rougher, Plate mill, CSP mill, Finishing mill), Cold rolling mill (Single stand reversing mill, Cold tandem mill, skin pass mill), Sectional steel mill (Beam line), Blast furnace converter	2-25 MW
Power	Pumps (Boiler feed pump, Cooling medium pumps), Coal mills, Conveyor belts, Blowers, Fans, Startup converters for Gas turbo generators and storage pump generators, static var comp., HVDC, static freq. changers, Wind turbines	1 -40 MW
Mining	Ore mills, Mine hoists, Conveyor belts, Pumps, Crushers, Blowers, Compressors, Bucket wheel excavators	2-15 MW
Water	Pumps, blowers	0.5 - 40 MW
Marine	Propulsion drives, Booster-generators, Thrusters, Winders	2-20 MW
Chemical, Cement, Pulp & Paper	Extruders, Pumps, Compressors, Blowers, Cement mills, Fans, Mixers, Presses	0.5 - 4 MW

Additionally, the following requirements are necessary:

- Low noise level
- Energy losses are minimal, and the efficiency is high.
- Sufficient space must be available
- Responsive service and efficient logistics for spare parts.
- Competence in supporting the sales and integration processes is essential.

In Table below 1.3 you will find a list of the key-requirements for the main applications in each of the industries listed in the table. In order to meet these requirements, the different circuit topologies that are used in the different application fields have to satisfy the different requirements of those circuit topologies.

1.3 Drive system challenges

MV drives (Akagi., 2001, Zargari et al.,2004) present a number of technical challenges that differ from low-voltage (≤ 600 V) ac drives. It may not even be

Table 1.3 Key requirements of the applications

Sector	Key requirements
Oil & Gas	2-quadrant operation, for existing motors, high standardization, steady state operation at rated power, high speed gearless drives
Metals, Mining	4-quadrant operation, high currents down to standstill, coordinated drives, high control performance, low torque ripple, stabilizing mechanical oscillations, high field weakening range
Power, Water	2-quadrant operation, for existing motors, high standardization, steady state operation at rated power, energy saving, start up converter

Marine	2-quadrant operation, 4-quadrant operation for booster-generators, marine certification, low dimensions, low weight, high efficiency
Chemical, Cement, Pulp+Pap	2-quadrant operation, start-up converters, high standardization, coordinated drives

Necessary to dress them for the low-voltage drives that must be dressed for the MV drives. In general, these requirements and challenges can be grouped into four categories: the power quality requirements associated with line-side converters, the challenges associated with motor-side converters, the constraints associated with switching devices, and the requirements associated with the drive system.

1.4 Drive System Requirements

MV drive systems must meet the following general requirements i.e., High efficiency, low manufacturing cost, small physical size, high reliability, effective fault protection, easy installation, self-commissioning, and low downtime for repairs. As a result, high dynamic performance, the ability to regeneratively brake and the capability to operate in four quadrants are some of the application-specific requirements. (Zargari et al., 2004)

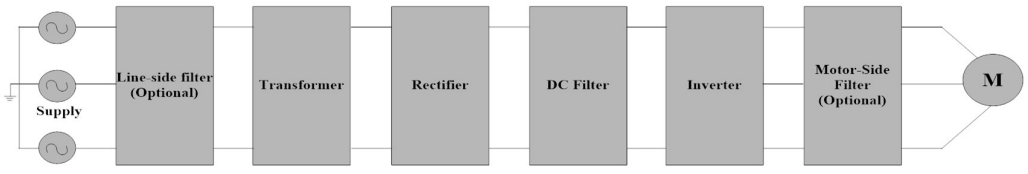


Figure 1.5 Details of medium votlage drive system

1.5 Advanced Power Converters

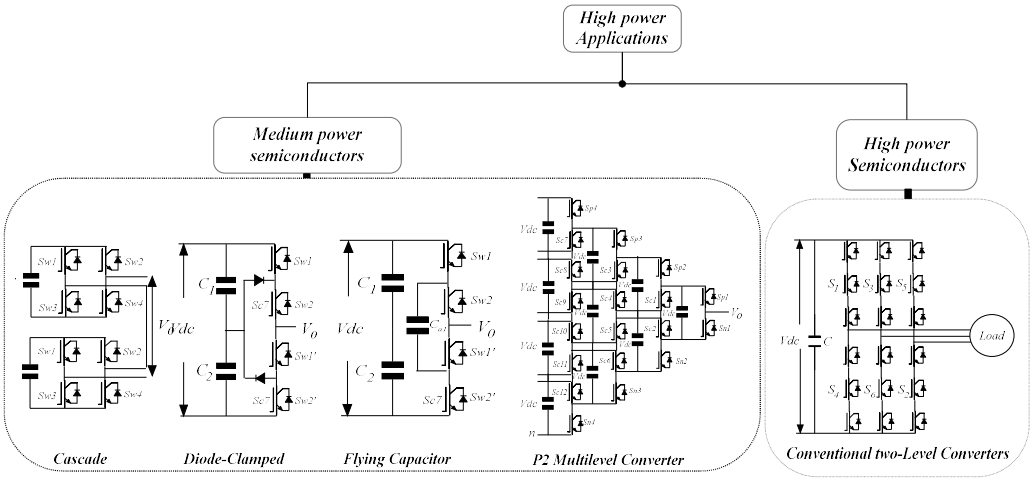


Figure.1.6 Traditional and advanced power coverters

Although Numerous Inverter designs are available in the industry but there exists a variety of topologies and control strategies when it comes to power converters. Depending on how the converter is going to be used, there are different design approaches that address different issues. One of the important concerns is waveform quality, which can be addressed in a number of ways. Waveforms can be filtered using capacitors and inductors. A transformer can be filtered on either its primary or secondary side or both sides if there is a transformer involved. A low-pass filter limits the passage of harmonic components while allowing the fundamental component to pass. This can adjust waveform quality. It should be noted that conventional inverters always produce waveforms of very low quality.

LC filters are often used in circuits to improve the quality of the output waveform. It is therefore also reasonable to assume that readers may have a question as to why the quality of the converter output is currently low at this point in time? What are the reasons for adding low pass filters to circuits? Also, how can the quality of the output waveform be increased without compromising the efficiency of the output waveform? These are all open issues associated with inverters of the present day. On the right side of Figure 1.6 is a conventional two-level inverter and it has several semiconductor devices connected in series. As a result, the converter's voltage rating

increases. However, the output level only offers two levels despite devices connected so as to meet load requirements. A bulk LC filter is used to run the motor in this high harmonic waveform. Several different power levels of multilevel inverters are proposed and designed to address this issue.

1.6 Traditional multilevel Inverters

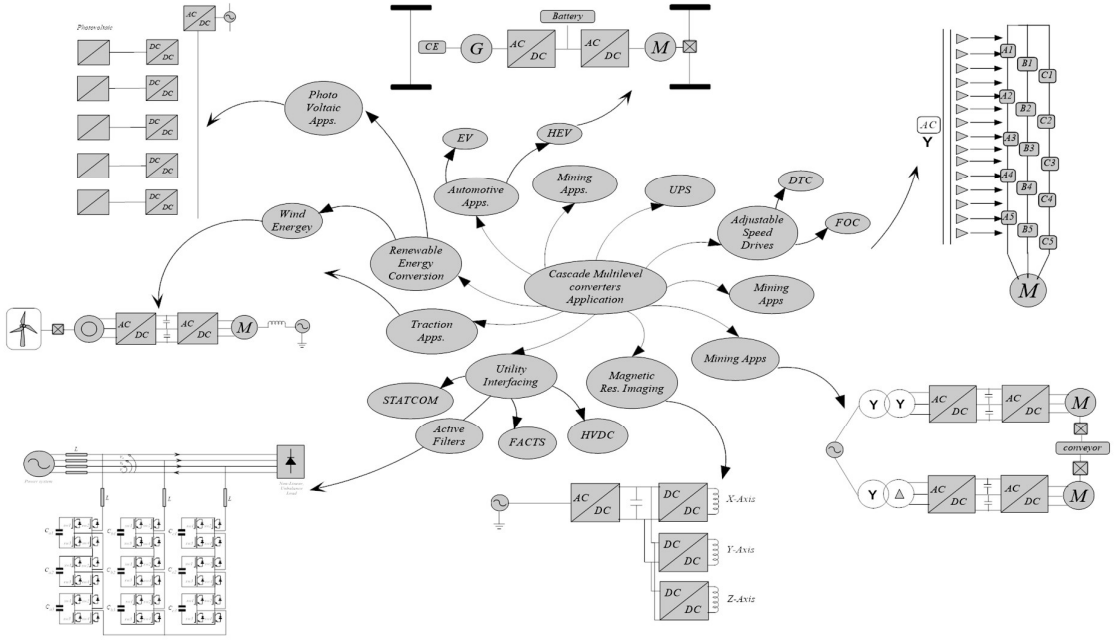


Figure 1.7 Details of multilevel inverter and its applications.

Here Figure 1.7 shows the major view and applications of multilevel inverter in different domains. It is quite evident that Multi-Level Inverter (MLI) has been introduced as an alternative to the conventional inverter for (Stemmler.,1994) high-power and medium voltage applications. As far as the MLI is concerned, the main concept is that in order to perform the power conversion, a staircase voltage waveform is synthesized by using a power semiconductor switch along with several lower voltage dc levels. Multiple input dc levels can be provided by capacitors, batteries, and renewable energy sources. Due to their advantages over conventional power electronic inverter topologies, MLIs are gaining interest in high voltage and

high power applications. In addition to generating high quality voltages and power for loads, the MLIs (Narimani et al.,2014) also have the ability to produce high voltages, low stress on the power switches, low THD in the output voltage and current waveforms, as well as low reactive components in the output filter, resulting in a higher power density as well as lower common-mode voltage when used with the output filter.

As opposed to conventional two-level inverters which are very well known, multilevel inverters have a lot of advantages. Essentially, these advantages are related to improving the quality of the output signal and increasing the nominal output power of the inverter. With the increasing number of levels in the power inverter, the output voltage of the power inverter improves its quality and the total harmonic distortion (THD) of the waveforms at the output is Minimised. These properties make multilevel inverters very attractive to the industry and, now a days, researchers from around the world are putting great effort into improving the performance of multilevel inverters. This includes simplification of control, optimization algorithms, and optimization of the output signals so that the THD of the output signals is reduced, the DC capacitor voltages are balanced, and the current ripples are reduced. The multilevel inverter is regarded today as a very attractive solution for applications requiring high power at medium voltages. Multilevel inverters are commercially available from several major manufacturers with a wide variety of control methods, each suited to different applications. In many industries, including oil and gas, metals, power, mining, water, marine, and chemistry, multilevel inverters have found an important market in high-power ac motor drive applications such as conveyors, pumps, fans, and mills.

Many advantages are offered by multilevel DC-AC conversions, including:

1. In addition to enhancing the harmonic profile, the staircase waveform helps mitigate the dv/dt stresses. This results in a substantial reduction in filter requirements (or even elimination), as well as a reduction in electromagnetic compatibility issues.
2. As compared to the overall operating voltage, semiconductor devices are subjected to much lower voltage stresses. It is therefore feasible to obtain a high-voltage waveform using switches rated at relatively low voltage levels.

3. By using MLIs, a motor connected to a multilevel motor drive can produce a much smaller common mode voltage, thus reducing bearing stress.

4. It is common for multilevel topologies to offer the possibility of obtaining a specific voltage level using a combination of switching strategies. In this way, fault tolerance can be programmed by utilizing these redundant states.

5. Input current can be drawn by MLIs with low distortion.

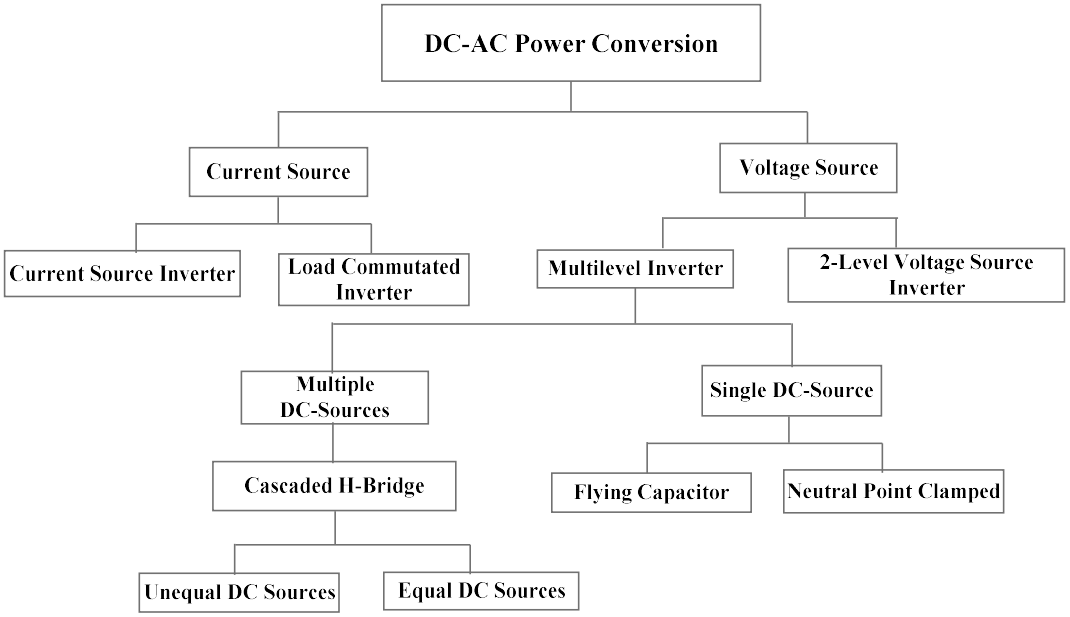


Figure 1.8 Multilevel converters classification

6. A multilevel inverter system can incorporate renewable energy sources such as photovoltaic, wind, and fuel cells and share the load equally among the sources. MLIs have gained wide attention in the research community over the last few decades.

It has been reported that several different topologies for multilevel inverters have been developed over the years. Based on the number of independent DC sources in their structure, they can be classified into two main groups. As far as topologies are concerned, there are three most common and commonly used ones: The Neutral Point Clamped (NPC) or Diode Clamped, the Flying Capacitor (FC) or Capacitor Clamped, and the cascaded H-bridge (CHB). Later, these topologies are redesigned and used in hybrid topologies. However, traditional MLIs are double stage MLIs. Because they

use DC to DC converter for boosting low voltage to high voltage then it is converted to AC in the second stage. Such a difficult conversion is not a viable solution for drive systems. Multi-level inverters (MLIs) with boost configurations have been developed to fulfil these requirements. Thus the current research involves the design of a single-stage boost Multi-Level Inverter (MLI) for the purpose of driving motors used in mining applications. The following is an outline for the thesis.

1.7 Thesis outline

Based on the literature review aim of the above objective, the thesis is structured as under.

1.7.1 Thesis organization

Abstract There is a need for Novel inverter for Drive system in Mining.

Chapter 1 Presents a brief introduction to Traditional inverters, Motivation, Different Electric Drives used in Mining.

Chapter 2 Literature Review, Research Objectives and Research Methodology.

Chapter 3 Proposes a High Reliable H7 & H8 Inverter Drive Systems, Principle of Operation, Merits and Demerits, THD analysis, Simulation studies.

Chapter 4 Proposes a novel single phase and three phase boost multi-level inverter, Design, Simulation studies, experimental studies, Comparison with existing topologies, reduced number of switches.

Chapter 5 Presented real time verifications of single and three phase boost multi-level inverter and their comparison with benchmark topologies in Mining systems.

Chapter 6 Summarizes the discussions on possible future research and conclusions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

There are several products available on the market today that are associated with MV drives. Various power converter topologies and control schemes are used in the design of these drives. There are some unique features that can be found in each design, but there are also some limitations as well. Diversification of offerings encourages innovation in drive technology as well as market competition. Here are a few examples of industrial drives within the medium voltage product range that could pique your interest.

Figure 1.2 Illustrates the picture of an MV drive rated at 4.16 kV and 1.2 MW. The drive is composed of a 12-pulse diode rectifier as a front end and a three-level power converter with LC filter and motor. It is evident when one takes a closer look at the system that there is an LC low pass filter at every stage of conversion, which is quite bulky due to the fact that it is designed to eliminate harmonics in the out voltages. Depending on how the power converter is designed, this filter size will vary. MLI configurations significantly reduce LC design when power converters are designed for various applications. With MLI, harmonics are minimized through pure voltage and current waveforms, resulting in a higher power factor.

2.2 Challenges in classical Converter Topologies

Aforementioned, MV drives are designed with different switching components and configurations use several LC filters and transformers to meet the load. However, apart from configuration there are few parameters that need to be considered for designing. The following are parameters and challenges that must be addressed during the design of a power converter.

2.2.1 Line Current Distortion

Normal rectifiers draw distorted utility line current, and they also create peaks and valleys in voltage waveforms. There are several problems that can be caused by the

distortion of voltage and current waveforms, including nuisance tripping of computer-controlled industrial processes, overheating of transformers, equipment failure, computer data loss, and malfunctions of communication equipment. When an assembly line is tripped by a nuisance, it often results in expensive downtimes and damaged products as a result. (The IEEE Standard 519-1992) This is one of the regulatory guidelines concerning harmonics, which outlines specific requirements. Compliance with this guideline is necessary when selecting the rectifier for the MV drive.

2.2.2 Input Power Factor

All electric equipment must have a high input power factor. A power factor of 0.9 or higher is required by most electric utilities so that customers are not penalized if their power factor falls below that. Since the MV drive has a high rating when it comes to power consumption, this requirement is especially important for it.

2.2.3 LC Resonance Suppression

MV drives that utilize line-side capacitors for power factor compensation or Current THD reduction form LC resonant circuits with their line inductance. By using the utility supply harmonic voltages or rectifier harmonic currents, LC resonant modes can be excited. Lightly damped LC resonances may cause severe oscillations or over voltages that can destroy rectifier components due to the low line resistance of medium voltage supplies. When designing the drive system, it is important to take into account the LC resonance issue.

2.3 Motor-Side Challenges

2.3.1 The DV/DT and Wave Reflections

During rising and falling edges of the inverter output voltage waveform, high dv/dt occurs due to the fast switching speed of semiconductor devices. It's possible for the dv/dt to exceed 10,000 V/µs depending on the inverter dc bus voltage and switching device speed. Motor winding insulation is likely to fail early due to partial discharge from high dv/dt (Steinke,1999) inverter output voltages. By stray capacitances

between the stator and the rotor, a voltage is induced on the rotor shaft because it drives a rotor rotation. Shaft voltage causes current to flow into shaft bearings, causing early bearing failure. The high dv/dt in the inverter can lead to electromagnetic emissions from the motor cables that may impact nearby sensitive electronic equipment. Due to wave reflections in long cables, the high dv/dt (Steinke, 1999) may cause a voltage doubling effect at the rising and falling edges of the motor voltage waveform. If the cable's length exceeds a certain limit, reflections can double the voltage on the motor terminals at each switching transient due to a mismatch between the cable's wave impedance and the inverter's and motor's impedances. For 500 V/μs, the critical cable length is 100 m, for 1000 V/μs, 50 m, and for 10,000 V/μs, 5 m is the critical cable length.

2.3.2 Common-Mode Voltage Stress

Common-mode voltages are normally generated by rectifiers and inverters switching. This is essentially a zero-sequence voltage superimposed on the switching noise, resulting in the common-mode voltages.(Wei et al., 2004) Without mitigation, they'll show up on the neutral of the stator winding, which should be zero when powered by a three-phase balanced utility supply.

A common-mode voltage can also lead to the motor line-to-ground voltage becoming substantially higher than the motor line-to-neutral (phase) voltage, causing premature motor winding insulation failure. Consequently, the motor's life expectancy gets shortened.

During the rectification and inversion process of the converters, common-mode voltages are generated. The switching transients of the high-speed switches can result in a high dv/dt, but this phenomenon differs from it. Furthermore, low-voltage drives often ignore the issue of common-mode voltage.

Low-voltage motors have a conservative insulation system, which is partly responsible for this. There should be no common-mode voltage applied to motors in MV drives. Moreover, the loss of production would make the replacement of the damaged motor very expensive.

2.3.3 Motor Derating

It is possible for high-power inverters to generate a large amount of harmonic currents and voltages. In motor windings and magnetic cores, these harmonics result in additional power losses. Consequently, the motor doesn't run at its maximum capacity because it's derated.

2.3.4 LC Resonances

An LC resonant circuit forms between the motor inductances and the capacitor on the motor side of MV drives. A harmonic voltage or current produced by the inverter may excite the LC circuit's resonant mode. During the design stage of the drive, the motor winding resistance can provide some damping.

2.3.5 Torsional Vibration

Motor inertias and mechanical loads can cause torsional vibrations in the MV drive. Drive systems include simple systems such as motors and loads with two inertias, as well as very complex systems (such as steel rolling mills with 20 inertias**)**. When torque pulsations caused by distorted motor currents coincide with the natural frequency of a mechanical system, torsional vibrations may be created. Broken shafts and couplings can be caused by excessive torsional vibrations, as well as damage to other mechanical components.

2.4 Switching Device Constraints

2.4.1 Device Switching Frequency

MV drives suffer from significant power loss due to device switching losses. In addition to reducing switching loss, the drive can reduce operating costs when it is in operation. The reduced cooling requirements for the switching devices can also reduce the drive's physical size and manufacturing cost. Secondly, limiting the switching frequency can prevent heat from being transferred efficiently from the device to its heat sink due to the thermal resistance of the device. For GTOs, the switching frequency is normally around 200 Hz, while for IGBTs and GCTs, it is usually around 500 Hz. When switching frequency is reduced, line- and motor-side

waveforms are generally more harmonically distorted. When switching frequencies are limited, it is important to make efforts to minimize the distortion of the waveform as much as possible

2.4.2 Series Connection

In the case of MV drives, switching devices are often connected in series for the purpose of operating at medium voltages. Due to the differences between static and dynamic characteristics of series connected devices and their gate drivers, they may not equally share the total voltage during blocking or switching transients. Protecting switching devices and enhancing system reliability requires a reliable voltage equalization scheme.

2.5 Study of traditional Multilevel Inverters

2.5.1 Neutral-point-clamped (NPC) inverters

NPC inverters are popular in high-power applications because they have a neutral-point clamping topology. First introduced by Baker and Bannister in 1980, the neutral point clamped MLI (NPCMLI) is also known as a diode clamped MLI (DCMLI). There are two clamping diodes, two DC link capacitors, and four switches in the per phase inverter circuit of a generalized three-level NPC inverter. A voltage clamping diode is an essential component of the NPCMLI topology.

With a neutral point in the middle of a common DC-bus, there are even numbers of bulk capacitors in series with a neutral point depending on the number of voltage levels in the inverter. A clamping diode is connected to a number of valve pairs connected to this DC-bus, where m is the number of voltage levels in the inverter.

Two new power semiconductors per phase were added to the classic two-level inverter topology. When comparing the two level cases with the same DC-link voltage, this new topology has each power device standing at half voltage. In this case, the voltage can be doubled if the semiconductors have the same characteristics. An NPCMLI with three levels and four switches is shown in Figure 2.1.

A single DC source can apply to any number of voltage levels with such MLIs, especially in three-phase applications. Despite this, NPCMLI has a lot of drawbacks, such as lack of modularity and difficulty balancing DC link voltage for more than three output voltage levels, which limits it for higher voltages and ac motor drives.

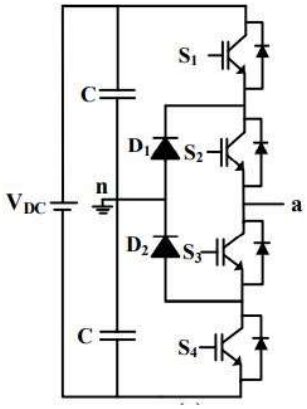


Figure 2.1 NPC MLI for Three-level.

Due to the fact that they use a single DC source for any number of voltage levels, MLIs are very useful, especially in three-phase applications. The major disadvantages of the NPCMLI are its lack of modularity, inability to balance the DC link voltage equally among the DC link capacitors, and its inability to drive high voltage or ac motors. It is necessary to use more capacitors in the DC-link if there are more stepped output voltage levels. In theory, it should be possible to distribute the DC voltage source evenly among the number of capacitors on the DC-link.

2.5.2 Flying capacitor MLI (FCMLI)

Multilevel inverters based on a capacitor clamped topology, also known as flying capacitors, are similar to NPCMLI topologies. Flying capacitor MLIs (FCMLIs), also known as clamping capacitor MLIs (CCMLIs), were introduced for the first time in 1992 by Menard and Foch as a form of high-speed MLI. To hold the voltage at the desired value, it uses capacitors instead of clamping diodes to hold the voltage in the desired range. As for the NPCMLI, m−1 number of capacitors on a shared DC-bus and 2(m−1) switch-diode valve pairs are used. To create output

voltages on the CCMLI, one or more capacitors are used instead of clamping diodes (depending on the inverter level and position).

In addition to DC bus capacitors, clamping capacitors, and switches, the m-level FCMLI also requires DC bus capacitors. In Figure 2.2, we can see a three-level FCMLI that consists of four IGBT switches and one DC bus capacitor (C). On each side of the midpoint between two valve pairs, they are connected to the midpoints of the valve pairs.

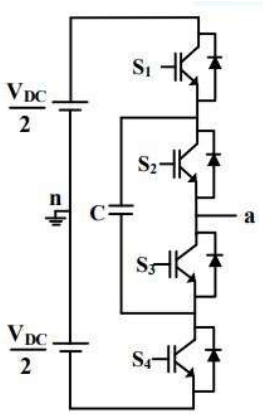


Figure 2.2 FCMLI for Three-level.

As compared to the NPCMLI, the FCMLI provides many advantages, including modularity, a design that can be easily extended, as well as capacitor voltage balancing at higher voltage levels. FCMLI, however, has several disadvantages, including its high cost (as a result of its large number of capacitors) and complex control circuitry. It is unlikely that the FCI will experience the same difficulties as the NPC

Increasing the number of output phase voltage levels raises the challenge of unbalanced dc-link capacitor voltages. For multilevel FCIs with higher voltage levels, however, there is a need for more capacitors. As a result of the start-up of a capacitor, a large amount of current is delivered.

To avoid damaging the power ratings of semiconductor devices during transient periods, pre-charge circuits are required. The DC source is connected to the

DC-link capacitor by a resistor in any inverter in order to minimize the current overstretching the switches during initial operation.

2.5.3 Cascaded H-Bridge Multilevel Inverter (CHBMLI)

MV drives with high power levels commonly use cascaded H-bridge (CHB) multilevel inverters. H-bridge power cells are used in multiple units. It is normal for H-bridge cells to be connected in cascade on their ac side in order to achieve low harmonic distortion at medium voltages. An inverter's operating voltage and manufacturing costs determine the number of power cells it contains. It is possible to reduce costs by using identical power cells, which results in a modular structure.

An isolated DC source is connected to several single-phase inverters in a cascaded H-bridge MLI topology (CHBMLI). In order to obtain five levels of output voltage, the device consists of eight power switches and two DC voltage sources. In Figure 2.3, an eight-IGBT CHB inverter with two DC sources and five levels of CHB is shown. It is possible to generate three voltage levels at each H-bridge of magnitudes +VDC, 0VDC, and −VDC. This system is flexible enough to work with almost all renewable energy sources by combining the output voltages generated by two of these H-bridges.

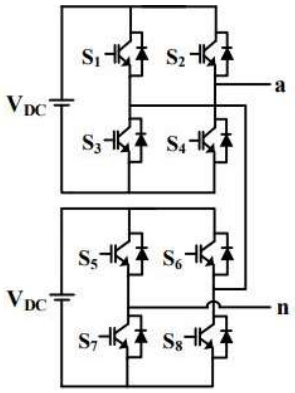


Figure 2.3 CHBMLI for five-level.

There are no clamping diodes or bulky capacitors in the CHB topology, unlike in FC or NPC topologies. By comparing the DC voltage sources of cascaded MLIs, we can further classify them as symmetric or asymmetric.

In contrast to the NPC converter, which has the problem of unbalanced capacitor voltages, the CHB converter does not have this problem. In addition, it does not need excessive flying capacitors to accomplish multilevel conversion, as do the FCIs. Nevertheless, because of the way the CHBI is configured, each cell of the CHBI experiences a high circulating current. As well as isolated dc sources, the CHBI is also required to supply dc voltage across each cell's dc capacitors.

In order to meet the requirements, the output voltage is boosted. Aside from that, the development of MLIs has led to a reduction in the number of parts, particularly for DC sources. The voltages are stepped up using transformers, which in turn increases the size of the system (Marusarz, 1989). In (Liang et al., 2002), (Abdullah et al., 2014), secondary circuits such as boosting converters are incorporated into the inverter topologies. However, this method is not only complex, costly, and unnecessary, but it also increases the overall size, complexity, and cost of the converter. An alternative to transformers, SC-MLI converters have emerged as another promising converter variant. In addition, SCs balance capacitor voltages without the need for a supplement circuit or complicated algorithm.

Renewable energy and electric vehicles are among the fields where SC-based inverters find application. An inverter circuit must incorporate a voltage boost when designing for such applications. There has been a development of new SC structures consisting of boost capability (Marusarz, 1989) in 1989, and another one in 1998 (Mak and Ioinovici, 1998). In order to enhance the voltage boost of SC structures, several structures have been designed based on these features. A study by Mak and Ioinovici (1998) and a study by Hinago and Koizumi (2012) were presented on SCs, in which the phase and voltage of the bipolar output signal is generated by end-side H-bridges, and the magnitude of the output signal has to be tolerated by the end side H-bridges.

In some applications, including those involving high power, this component may limit the converter's usability. Additionally, these circuits require a greater number of capacitors in order to achieve higher levels. SC converters with self-voltage balancing

have been developed by (Axelrod et al., 2005) and (Peng et al., 2019); however, higher levels require a significant amount of components.

(Liu et al., 2018b) introduces a seven-level module with a single dc source split into two equal halves by two capacitors. Semiconductors are most stressed at Vdc. For the higher-level extension, however, more isolated dc sources are needed due to the boosting factor of 0.5. In the paper (Liu et al., 2013) a cascaded MLI SC converter is proposed for high-frequency applications. SC consists of H-bridge units in each basic cell.

In order to extend the topology to higher levels, isolated DC sources must be used. Using the topology of (Liu et al., 2013), (Ye et al. 2014) developed an SC-MLI requiring only one DC source, reducing the number of required semiconductors. The conversion's blocking voltage is increased by the H-bridge at the second end, which boosts the boosting factor per capacitor.

Based on the topology presented in (Barzegarkhoo et al., 2016), asymmetric configurations can be produced with a reduced number of components and higher levels can be produced. It is important to note that the boosting factor is unity per capacitor, and the structure takes advantage of the higher standing voltages across the devices. Asymmetrical circuits with binary boosting factors have been developed by the authors (Saeedian et al., 2018a), and (Liu et al., 2018a) for high voltage boosting gains. The levels, however, are produced with more capacitors, and semiconductor devices are subjected to greater stress across the H-bridge, which generates polarity.

There are merits and demerits to power converters, as mentioned earlier. In our applications, however, the overall size of the system is bulky, so reducing the converter size and cost is important. The traditional topologies of energy conversion include two stages and three stages, and there is a need for DC to AC conversion with particular gain and minimum components.

2.6 Problem statement

In practice, it is challenging to assess various MLI topologies for drive systems as they are diverse and represent a vast family. Further, converters that are presently utilized for mining, traction, and conveyor systems need to be readdressed with compact and efficient designs. Although MLI-based structures meet the demand conversion of DC to AC is an essential component to be researched further. **As a matter of fact, the conversion process from low voltage to high voltage levels and the criterion affects the system to be compact and reliable**. In this regard, some of the key points are mentioned below for the convertor design:

1. Number of semiconductors used

2. Total blocking voltage of the converter

3. Optimal controllability of the topology, i.e., the degree of freedom on modulation and capacitor voltages.

4. Possibility of employing asymmetric sources/capacitor voltage ratios in the topology

5. Number of passive components

Parameters 1 and 2 affect the reliability, cost of the inverter. At the same time, the efficiency is influenced by parameters 1, 2, 3, and 5. A number of redundant states and fault-tolerant operations are directly influenced by 1 and 4. Parameter 5 influences the dynamic response of the inverter. Several efforts are made to generate higher voltage levels with less part count in the recent past. In that process, capacitors as intermediate voltage level generating devices have gained more attention. On this line, the research work in this thesis aims to investigate the hybrid MLIs and synthesize possible topological variations for enhancing the structural and operational behaviour of the selected emerging converter families. Besides, it also aims at developing suitable control strategies for the developed structures for their reliable operation. For this study, two converter families, flying-switched-capacitor is considered. Having outlined the variants and limitations of the available hybrid

topologies, this research is oriented toward developing novel Inverter (MLI) configurations and control strategies to enhance their operational performance in medium and high-power applications. Considering the optimization of converter topologies and generating a higher number of voltage levels, the thesis aims at developing a level inverter topology found to exhibit global compliance on the whole standard imposed range. (Chaudhuri, 2008)

2.7 Thesis objectives

The main objective of this work is to study and develop novel models of MLI in simulation software and implement them for passive loads as a prototype hardware module. The following are the objectives of present research:

1. Design and verification of a novel **Boost Multilevel Inverter** with fewer components.

2. To evaluate the performance of the proposed inverter for different load conditions.

3. To systematically compare and evaluate the proposed topology in **real-time simulator** in terms of performance, and component count.

2.8 Methodology

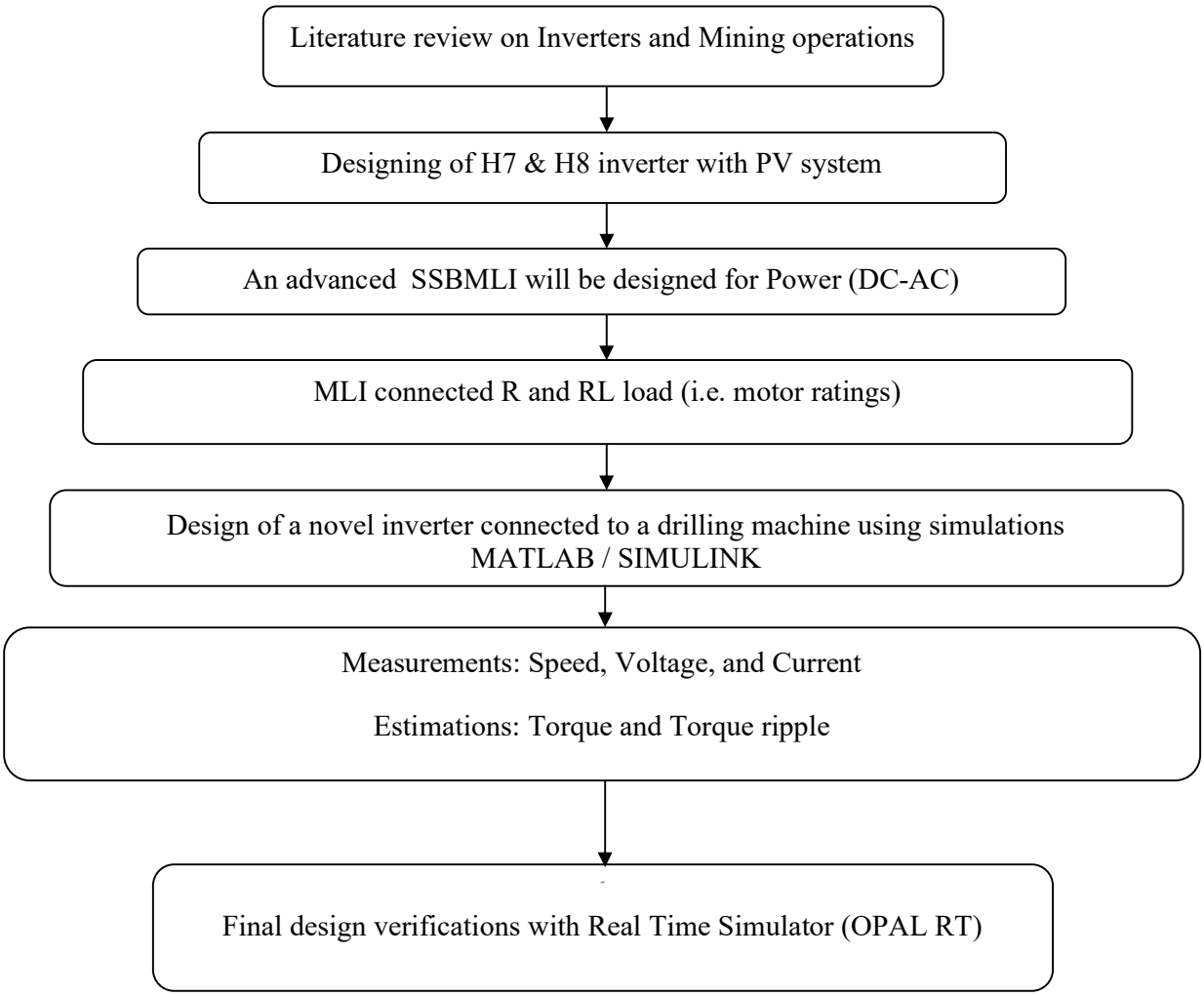
To achieve the above objectives following methodology will be adopted.

1. A detailed literature review will be carried out on photo-voltaic panels, inverters, and Mining operations in mines currently used.
2. Design and modeling of H7& H8 inverter with the photovoltaic system.
3. An advanced Single Stage Boost Multi Level Inverter will be designed for power conversion (DC-AC).
4. The Proposed Multi-level inverter connected to R load and R-L Load will be modeled in MATAB/Simulink and verified by using a real-time simulator (OPAL-RT)
5. Different control techniques namely Modified discontinuous sinusoidal pulse-width-modulation (MDSPWM), and Space vector pulse-width-modulation

(SVPWM) are developed to control the inverter and compare the same systems.

6. Measure the voltage, current, and speed with different torque conditions.
7. Comparing the traditional inverter torque ripple with the proposed one.
8. Studied the influence of the System parameters like THD, Voltage, Current, Torque, and Speed (RPM).
9. Observed the output with different modulation index values.

2.8.1 Flow Chart for the Methodology



CHAPTER 3
H7 AND H8 INVERTERS

Introduction

In the previous chapter, an introduction to drives, respective configurations, functions, and features is furnished. However, in the applications of mining system traction, Conyers and drilling an important aspect. To address these aspects a novel three-phase inverter is designed and the same is utilized for the above-mentioned applications. To showcase the performance of the proposed inverter RL load is considered. Moreover, the proposed inverter will compare with the traditional B6 inverter in terms of efficiency.

3.1 Designing of Novel H7 & H8 Inverter

Traditional inverters i.e., B6 inverters use only 6 switches to drive the system (i.e., to meet the demand of a certain load). Regarding, B6 inverters (i.e., inverters with six power electronic devices) are more popularly used in the early days for PV applications with a transformer for isolation purposes, which adds more cost and weight to the system. It also has many power stages that affect the efficiency of the system. Further, a notable issue in the drive systems when connected with renewable energy source are Common mode leakage current. This aspect is the main constraint to the elimination of transformers in the PV inverter systems but it reduces the complexity, size, and cost. However, balancing capacitance and fictitious capacitance arising across the PV panel causes the leakage current. Thus, leakage current has an impact on the efficiency of the PV system introduces unwanted signals at the output, and increases the harmonic distortion. It also induces spurious signals through electromagnetic interference. It demands a mechanism to minimize the leakage charge per time in PV inverter systems. To address the aforementioned problems H7 & H8 are introduced. Several topologies and control techniques were proposed recently to overcome the difficulty of leakage current. Particularly, H5 and H6 topologies are proposed originally for single-phase PV inverters (E.un et al., 2009) and the same is extended for H7 and H8 topologies respectively for three-phase PV systems. Herein, PV systems are used as the case is very much apt for mining applications. In the

recent past, inverters with renewables have been quite popular in remote locations. The proposed H7 & H8 Inverters are targeted to address similar issues like conveyors, tractions, drilling, and mining systems.

3.1.1 PWM techniques for H7 & H8 Inverter operation

Various traditional PWM techniques are available for the control of the inverter, targeting the reduced leakage current and THD. Namely, C-PWM, SV-PWM, and D-PWM are not suitable for reducing leakage charge per time in transformer-less PV inverters (T. Kerekes et al., 2011). The use of additional switches with zero state switching or control of fluctuations in PV panel voltage is a key point to reducing leakage current (L. Zhang et al.,2014).

The major mining applications include lighting, hand-held mining apparatus, mine water pumps, ventilation systems, and drilling jumbos, which should facilitate with a power supply, having less harmonics. In surface mines, power supply problems are solved to a greater extent with latest power electronic converters and renewable energy systems. As an example a drilling machine with transformer-less PV inverter is easy to carry and handle in surface mines, where technicians are required to cover wide area in a day. In section, H8 PV system with RL load was analyzed for mining equipment applications. Leakage current is reduced to less than 350 mA which is very less when compared to traditional B6 type inverter. The results are reviewed and compared among various possible loads in the mining applications.

3.1.2 Significations of the leakage current

Leakage current problems are popularly minimized using transformer less PV inverters. This topology gives galvanic isolation (i.e.isolation of load and source by DC/ AC coupling) between PV system and the load (R.vinod et al. 2018). The equivalent circuit for leakage current due to common mode voltage (V_{CM}) and PV capacitance (C_{PV}) is shown in Figure 3.1. This leakage current discharges the PV Panel and reduces the efficiency of the system. Figure 3.2 shows the circuit for modelling the leakage current for B6 PV system. The leakage current can be derived from equivalent circuit and can be extracted from Kirchhoff's law given in Equation (1)

$$I_{leakage} = C_{PV} \frac{dV_{CM}(t)}{dt} \qquad (3.1)$$

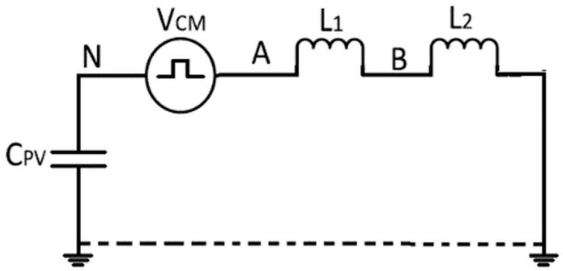


Figure 3.1 Equivalent circuit to analyze leakage current

3.2 Proposed H7 and H8 topology for Mining Equipment Realized with RL Load

The proposed H7 and H8 confutations are shown in Figure 3.3 and 3.4 respectively. With devices from S_1 to S_6 forms the basic B6 inverter. Addition of switch S_7 results in H7 configuration and addition of S_7 & S_8 results in H8 configuration. With the removal of transformer only, the leakage current problem arises. Galvanic isolation is obtained by these additional devices S_7 and S_8. Leakage current can be made zero during freewheeling periods in case of RL or RLE loads with DC/ AC decoupling. Various PWM techniques are tried by the researchers in the earlier. These PWM techniques mostly differed based on production of zero vector and reference vector. Two opposing active vectors are used to produce zero vector in AZS-PWM and three triangular vectors are used to produce zero vector in NS-PWM. Group of odd/even vectors are used to produce desired voltage vector, in RS-PWM. RS-PWM only focuses on leakage current but neglects the overall performance of the PV inverter. RCMV-PWM technique is used to reduce minimize common mode voltage and leakages charge per time without using zero vectors. But the elimination of zero vectors introduces the issue of voltage linearity, and harmonic distortion. Conventional SV-PWM and D-PWM provides good performance, simplicity, reduced switching losses and harmonics. And the voltage vector are shown in Figure 3.5

The common mode voltage of a three-phase inverter is expressed as (3.2)

$$V_{CM} = \frac{V_{an} + V_{bn} + V_{cn}}{3} \tag{3.2}$$

The common mode voltage for different switching states are mentioned in Table 3.1. Pulse patterns for various PV inverter systems PWM techniques are clearly mention in (Freddy et al. 2015).

In this study, the inverter was controlled by MD-PWM technique (a pulse patterns is a combination of NS-PWM and RS-PWM/ AZS-PWM). This technique is applied to reduce the leakage current, without sacrificing the overall performance. Basic D-PWM proved to be best for voltage linearity, harmonics reduction and switching losses. But it causes the leakage charge per time and ripples in the output current. Although galvanic isolation is possible both with DC & AC decoupling. AC decoupling results better performance with reduction in switching losses (E.un et al., 2009). Galvanic isolation reduces leakage current up to some extent only and further reduction can be obtained by common mode voltage clamping. Optimal clamping performance is obtained by zero state rectifier voltage switching not shown in the structure for simplicity.

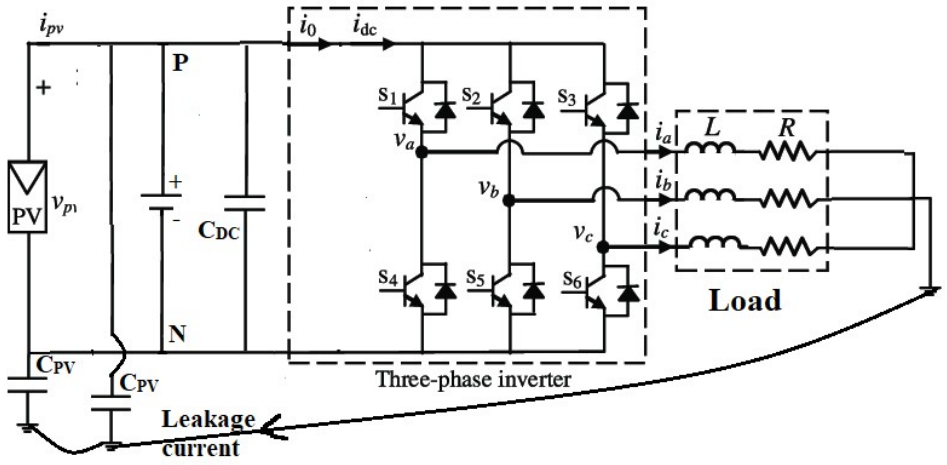


Figure 3.2 Transformer-less B6 photovoltaic inverter with RL load

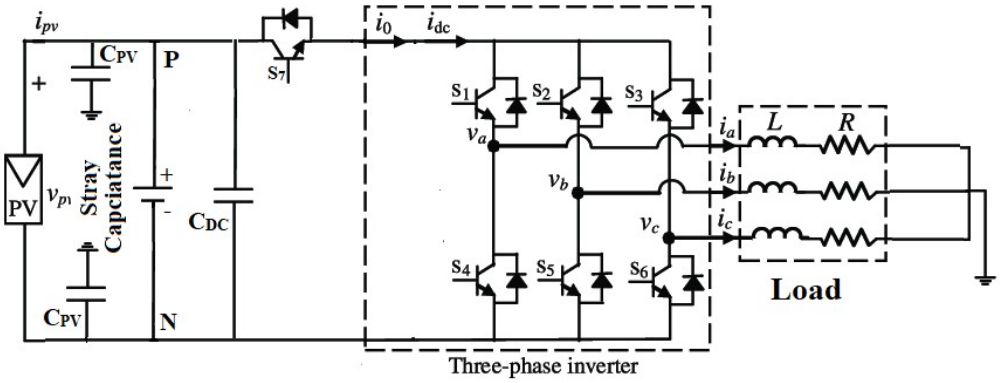


Figure 3.3 Transformer-less H7 photovoltaic inverter with RL load

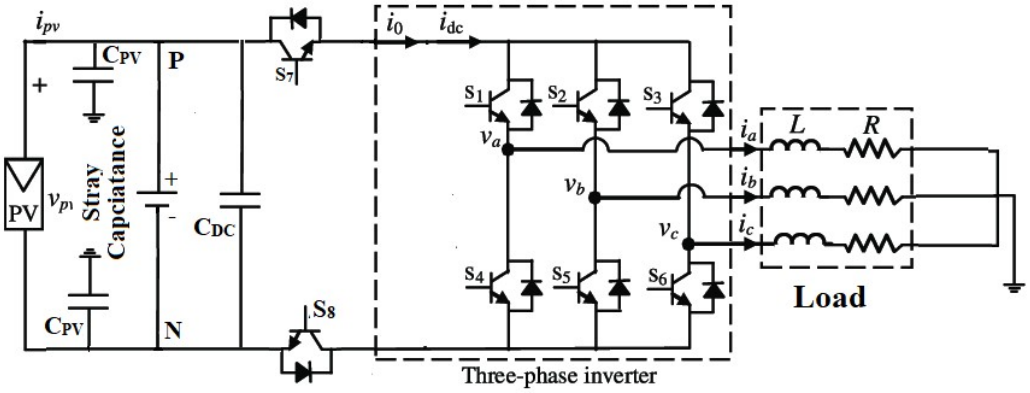


Figure 3.4 Transformer-less H8 photovoltaic inverter with RL load

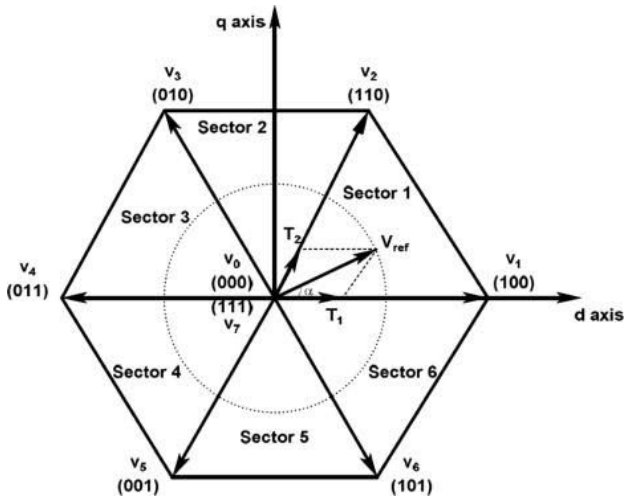


Figure 3.5 State space representation of voltage vectors [6]

Table 3.1 Common mode voltages for inverter switching states

Switching state ($S_1S_2S_3$)	Voltage vector	Common mode voltage
100	V_1	$\frac{V_{dc}}{3}$
110	V_2	$\frac{2V_{dc}}{3}$
010	V_3	$\frac{V_{dc}}{3}$
011	V_4	$\frac{2V_{dc}}{3}$
001	V_5	$\frac{V_{dc}}{3}$
101	V_6	$\frac{2V_{dc}}{3}$
111	V_7	$\frac{V_{dc}}{3}$

D-PWM performs well with transformer type PV applications in view of losses and THD, but it yields high leakage current and voltage ripples. MD-PWM is used to overcome such problems. Inverter switching states are controlled like normal inverter for the desired voltage. S_7 and/or S_8 are controlled to reduce leakage current. It uses all active and null state vectors to produce desired output voltage as listed in Table 3.1. Null state vector can be obtained V_7 state. If V_1, V_2…V_7 states are indicated by 1, 2….7 then sector switching pattern for the Figure3.5 is tabulated in Table 3.2.

Pulse pattern of D-PWM and MD-PWM only differs in null vector implementation in regions 2, 4 & 6. D-PWM locks the common mode voltage between $\frac{V_{dc}}{3} \& V_{dc}$ in sectors 1, 3 & 5. Where as in sectors 2, 4, & 6 it locked between $\frac{V_{dc}}{3} \& \frac{2V_{dc}}{3}$. Null vector of V_0 influence the output voltage profile and reduces current ripples.

Table 3.2 Inverter switching pattern for each switching state

Sector Number	Switching pattern
1	72127
2	23732
3	74347
4	45754
5	76567
6	61716

3.3 Simulation of MD-PWM solar PV system

Simulation was implemented according the circuit diagrams shown in Figure 3.3 and 3.4. The simulation was carried out using MATLAB simulation software. Inclusion of S_7 forms H7 configuration. Leakage current flows during freewheeling period between load and PV panel during null state of 0 & 7. To stop this leakage current between load and PV panel, S_7 is included in conventional basic B6 inverter. Proper

control of this additional switch with the proposed MD-PWM can reduce the leakage current.

Using the equivalent circuit of Figure 3.1, the common mode voltage is given by

$$V_{CM} = \frac{V_{an} + V_{bn} + V_{cn}}{3} = \frac{V_{dc}}{3} \qquad (3.3)$$

Equation (3) shows that common mode voltage is reduced by three times in H7 and H8 topology when compared to B6 inverter.

3.3.1 Simulation results

Figure3.6 and 3.7 shows that the simulation waveforms output voltage, current and it's THD. From the Figure 3.6 and 3.7, it is clear that the load current is fairly sinusoidal with reduced harmonic content. They also shows that, the common mode voltage is found to be $\frac{V_{dc}}{3}$ for switching states 1,3 & 5. And it is $\frac{2V_{dc}}{3}$ for the switching states 2, 4 & 6. Null state is obtained by switching ON all the upper group of switches

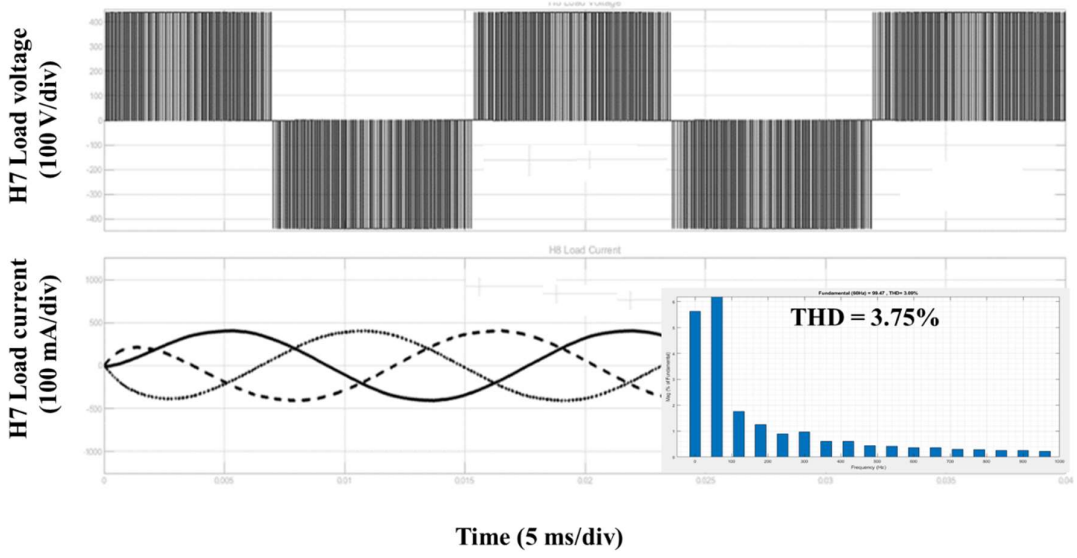


Figure 3.6 Load voltage, current and THD with H7 photo voltaic inverter

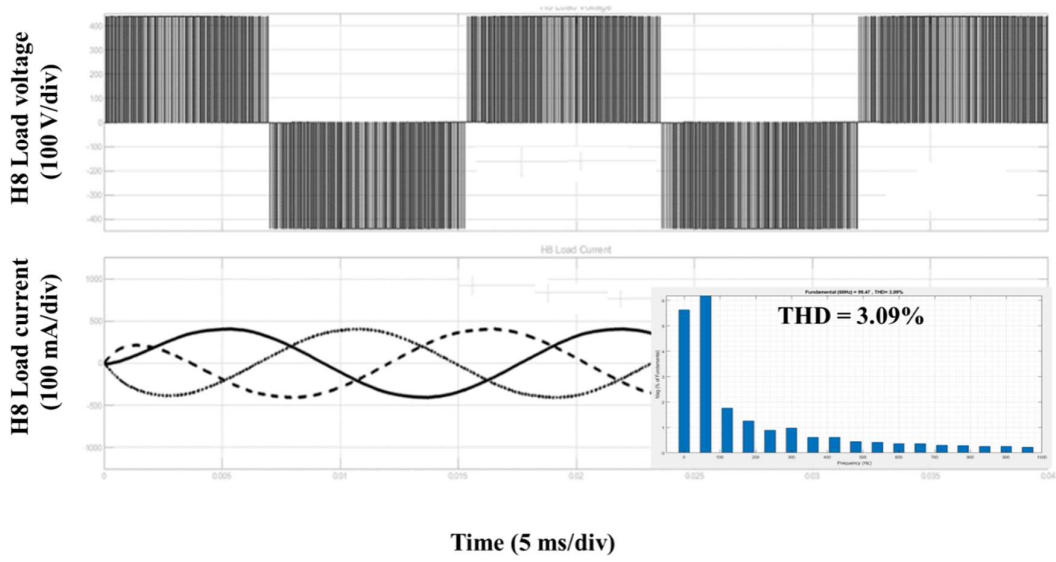


Figure 3.7 Load voltage, current and THD with H8 photo voltaic inverter

The corresponding common mode voltage is $\frac{V_{dc}}{2}$. Zero switching state is avoided to reduce the leakage current as mentioned earlier. Also the leakage current in both configurations are found to be less than 350 mA. The performance is improved in terms of quality of the load current. The load current THD is found to be 3.75 % with H7 configuration and it is 3.09 % with H8 configuration. This THD is around 6 % in conventional photovoltaic inverter systems. The Harmonic analysis is depicted in Figure 3.6 & 3.7. The basic comparison of these topologies are compared with conventional photovoltaic inverter is shown in Table 3.3.

Table 3.3 Comparative results of B6, H7 and H8

Parameter	B6	H7	H8
Leakage current	600 mA	350 mA	318 mA
THD	6.8%	3.75%	3.09%
Efficiency	94.5 %	94.14 %	94.05 %

3.3.2 Experimental results

The proposed topology was implemented experimentally. The design data is given in Table 3.4.

Table 3.4 Design data

Parameters	Rating
Power rating	1000 W
PV Module	500 V, 2 A
Switching frequency	20 kHz
Stray capacitance	0.05 µF
DC link capacitance	5 µF
Inverter Voltage	100 V
Load Inductance	0.8 mH
Load resistance	0.25 Ω

The experimental setup is shown in Figure 3.8. It includes PV module, DC to DC step up converter, stray capacitance, DC link inductance and capacitance, three phase inverter and switching module with a D-space kit. The MD-PWM gating pulses are generated using D-space interface with an adaptive model in the MATLAB.

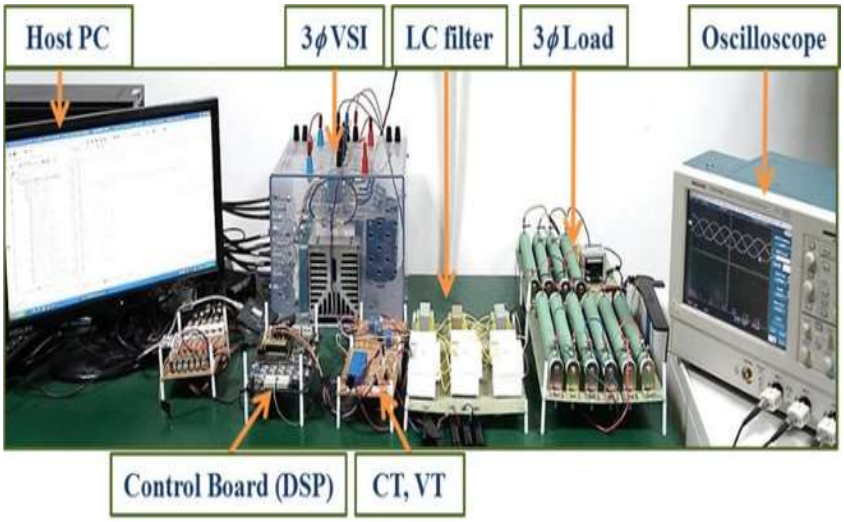


Figure 3.8 Experimental setup

The leakage current is measured both for H7 and H8 inverters, found to be 350 mA and 320 mA respectively for the H7 and H8 inverter topologies. These values are almost matching with analyzed leakage currents through simulation. The leakage current patterns are shown in Figure 3.9 for H7 and H8 topologies.

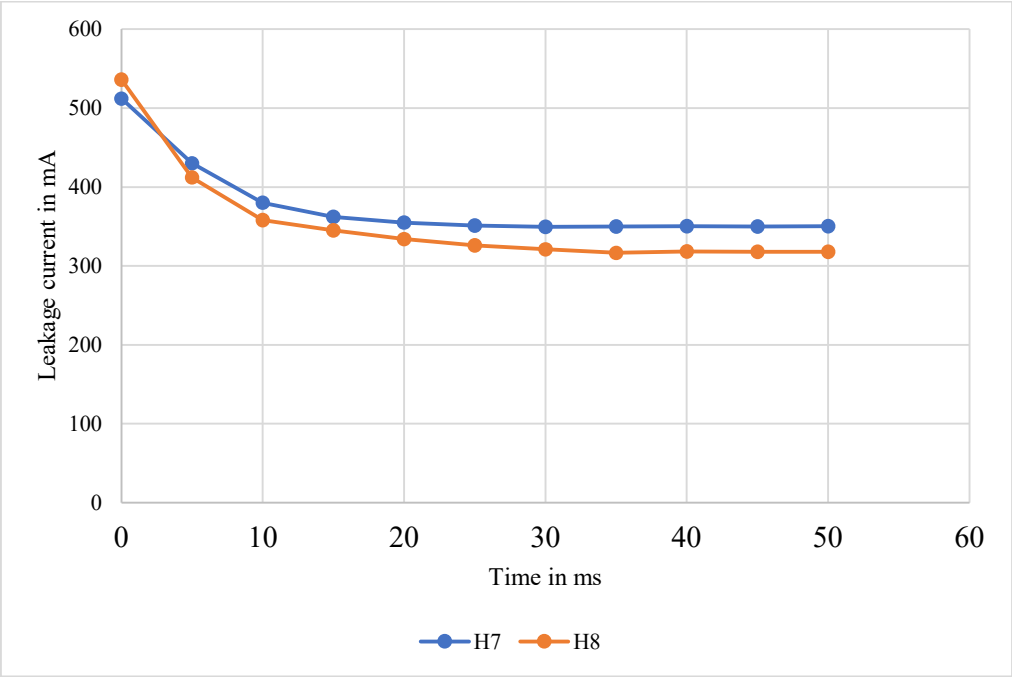


Figure 3.9 Experimental leakage current patterns

The efficiency also calculated from the experimental set up. The efficiency is found to be around to be 94% in both cases without much difference between the two topologies.

3.4 Summary

In this chapter, H7 & H8 photovoltaic transformer-less inverter with MD-PWM technique with RL load (i.e. equivalent to motor specifications') is shown. The same can be extended to portable equipment for mining industry. The difficulty of leakage current problem with conventional type PV inverters is solved to fair extent. Common mode voltage is clamped with zero state voltage switching. THD is found to be 3.75% and 3.09 % respectively in H7 and H8 configurations. The improved performance of the inverters can applicable to greater extent in mining applications.

CHAPTER-4

BOOST MULTI-LEVEL INVERTER

Introduction

A dual boost nine-level inverter for mining applications is proposed in this work. Capacitors are used as virtual sources to boost the voltage magnitude and increase the levels. Additionally, the proposed MLI circuit inherits benefits such as self-balancing capacitors, less blocking voltage, and fewer components. A simple PD-PWM scheme is used to generate gating signals. Circuit portrayal, operating principle, modulation, and capacitor voltage ripples are studied. MATLAB software is used to carry out simulations, and the obtained outcomes prove the boosting ability under different loading circumstances. A detailed comparative review is conducted with other recent SCMLIs to illustrate the superiorities of the proposed circuit.

4.1 Proposed topology

4.1.1 Circuit description

Figure 4.1 depicts the proposed dual boost Multi Level Inverter (DB-MLI) circuit. As the name implies, DB-MLI produces two times boosted output with the magnitude of $0.5V_{dc}$ for each level and provides nine-levels in output voltage. The DB-MLI generates levels from $2V_{dc}$ to $-2V_{dc}$ with 11 power electronic switches, two capacitors. Capacitors C_1, C_2, are charged- discharged several times with series-parallel technique to generate levels. The equivalent switching circuitry for all nine voltage-levels/modes is portrayed in Figure 4.2. The grey, red, and green capacitors indicate the unaffect, discharge, and charge states, respectively. Another significant advantage of the proposed DB-MLI is that it forms zero and negative levels without a back-end H-bridge. The blocking voltage of the semiconductors does not exceed source voltage even for higher levels. All switches except switch S_7 have to block supply voltage V_{dc}, whereas S_7 has to block $0.5V_{dc}$. Therefore, lower-voltage rated semiconductor switches can be used in the inverter.

Table 4.1 shows the switching-pattern and the effect on the capacitor for the respective voltage level. Here C, D, - , 1, and 0 stands for a charge, discharge, idol, ON, and OFF, respectively. Capacitors C1, C_2 charge, discharge several times, as shown in Table 4.1. Capacitor C_1, C_2 charge to the half of the source voltage $0.5V_{dc}$ through S_3, S_5, S_6, and S_8. Load impedance does not affect the charging loop's time constant, and capacitor voltages instantly reach their final value because semiconductors' parasitic resistance is meager. However, load impedance increases the discharging loop's time constant while discharging the capacitors. since the load resistance is high compared to the semiconductor parasitic resistance. As a result, capacitor voltages are balanced at reference value even with fewer charging states. It is worthy of mentioning that the capacitor voltages are kept at $0.5V_{dc}$ without any auxiliary balancing circuit, thus, reducing control- complexity.

Further, it is comprehended that ripple across the capacitor is inversely proportional to the capacitance. The equation to size the minimum capacitance (C_{min}) with x% ripple, amount of charge during highest time interval (ΔQ_{Cn}) can be given as,

$$c_{n\,min} = \frac{\Delta Q C_n}{x\% X v_{cn}}; n = 1,2 \qquad (4.1)$$

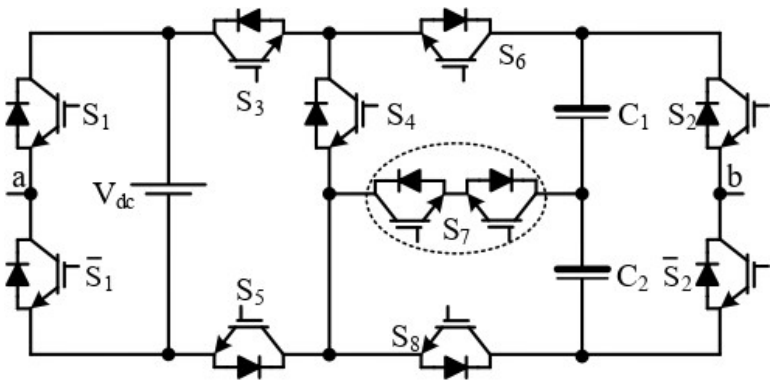


Figure 4.1 Proposed DB-MLI circuit

4.1.2 Modes of Operation

Output voltage levels are produced by adding voltage across DC link and boost capacitors. Switching table for the voltage levels of proposed DB-MLI is listed in Table 4.1. Figure 4.2 illustrates the operation of various modes with the current path

and active switches for the output voltage, V_o. Operating modes for the positive half cycle are elucidated as follows:

- $2V_{dc}$ level: Semiconductors S_1, $\bar{S}_2$, S_4, S_5, and S_6 are ON, connecting capacitors and source in additive. The resulting voltage at terminals a-b is $2V_{dc}$ ($1V_{dc}$ + $0.5V_{dc}$ + 0.5Vdc).
- $1.5V_{dc}$ level: Semiconductors S_1, S_2, S_5, and S_7 are ON, connecting C_2 and source in additive. The resulting voltage at terminals a-b is $1.5V_{dc}$ ($1V_{dc}$ + $0.5V_{dc}$).
  $1V_{dc}$ level: Semiconductors S_1,$\bar{S}_2$ S_5, and S_8 are ON, source to terminals a-b. The resulting voltage at terminals

Table 4.1 Switching Table of Proposed Switches

SWITCHING TABLE OF PROPOSED										
$V_0=V_{ab}$	SWITCHES								CAPACITOR	
	S1	S2	S3	S4	S5	S6	S7	S8	C1	C2
$2V_{dc}$	1	0	0	1	1	1	0	0	D	D
1.5 V_{dc}	1	0	0	0	1	0	1	0	-	D
1 V_{dc}	1	0	1	0	1	1	0	1	C	C
0.5 V_{dc}	1	0	1	1	0	0	1	0	-	D
0	1	1	1	0	1	1	0	1	C	C
0	0	0	1	0	1	1	0	1	C	C
-0.5 V_{dc}	0	1	0	0	1	0	1	0	D	-
-1 V_{dc}	0	1	1	0	1	1	0	1	C	C
-1.5 V_{dc}	0	1	1	1	0	0	1	0	D	-
-2 V_{dc}	0	1	1	1	0	0	0	1	D	D

a-b is $1V_{dc}$. Both capacitors charge through S_3, S_5, and S_6, and S_8 in this mode.

- $0.5V_{dc}$ level: Semiconductors S_1, S_2, S_3, S_4, and S_7 are ON, connecting C_1 to terminals a-b. The resulting voltage at terminals a-b is 0.5Vdc.

- $0V_{dc}$ level: Semiconductors S_1, S_2, S_3, and S_6 are ON, shorting the terminals a-b. The resulting voltage at terminals a-b is $0V_{dc}$.

  The PD-PWM approach is utilized to produce gating signals. The rationale behind the selection of the fundamental switching frequency PWM method is to formulate the energy balance expressions straightforwardly. Besides that, harmonics decrease significantly, therefore, improving the quality of the output waveforms. In this regard, The amplitude modulation index in terms of peak magnitude reference (Vm), carrier waveforms ($\hat{v}_{car}$) is presented as

$$m_a = \frac{V_m}{4 \times \hat{v}_{car}} \tag{4.2}$$

Nonetheless, other PWM techniques like the round-control method, selective harmonic minimization methods, other (Yellasiri et al. 2019), and (M.saeedian et al. 2018) are also equally applicable.

For the proposed nine-level inverter, four triangular carrier waves are compared with a rectified sine wave (Vref = |Vmsin(ωt)|) to generate firing pulses of the semiconductor switches. The outputs of comparators are designated as P1 - P4 and a cycle selector as C. Further, the gating signals for each of the switches are derived using the switching combination listed in Table 4.1

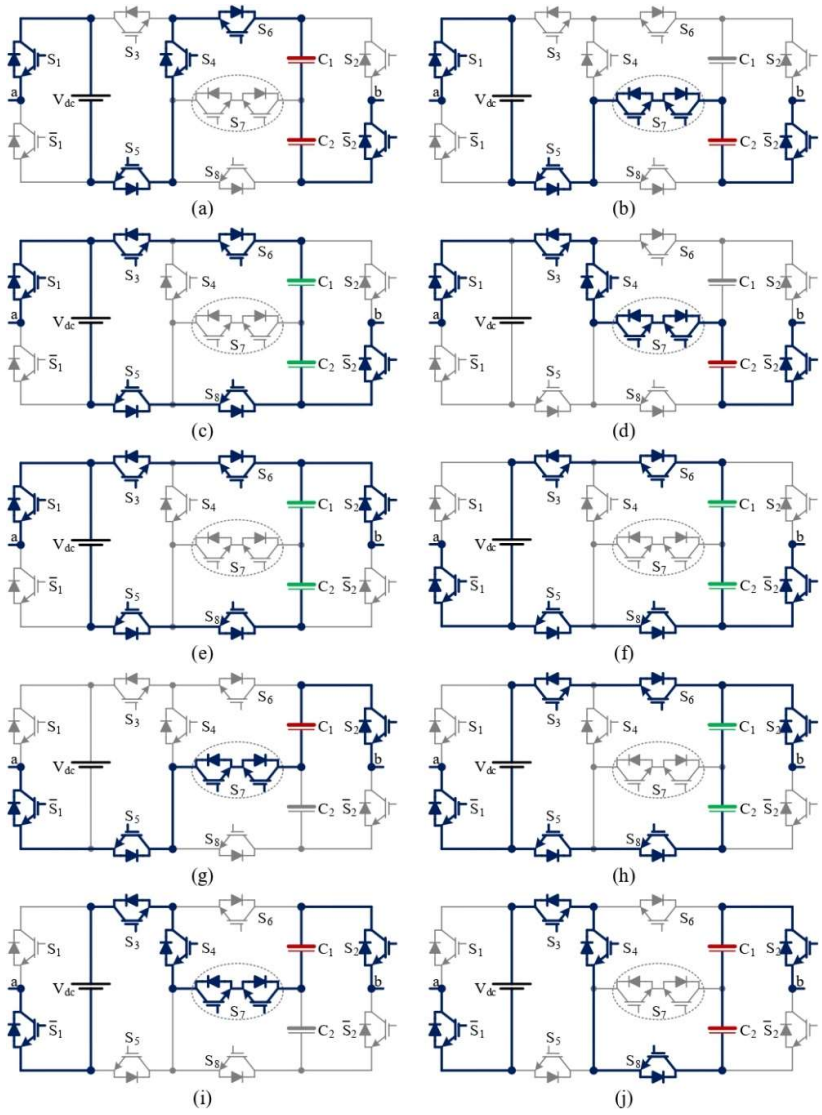


Figure 4.2 Modes of operation: (a) 2Vdc, (b) 1.5Vdc, (c) 1Vdc, (d) 0.5Vdc, (e) 0Vdc, (f) 0Vdc, (g) -0.5Vdc, (h) -1Vdc, (i) -1.5Vdc, (j) -2Vdc.

Therefore, the switching equations are given as,

$$S1 = S3 = C \tag{4.3}$$

$$S2 = \bar{P}_2 \cdot C + P2 \cdot \bar{c} \tag{4.4}$$

$$S4 = S7 = \bar{P}_1 + P2 \cdot \bar{P}_3 + P4 \cdot \bar{c} \tag{4.5}$$

$$S5 = S6 = P4 \cdot C + \bar{P} + P2 \cdot \bar{P}_3 \tag{4.6}$$

S8 = P1 · $\bar{P}_2$ + P3 · $\bar{P}_4$ (4.7)

S9 = P4 (4.8)

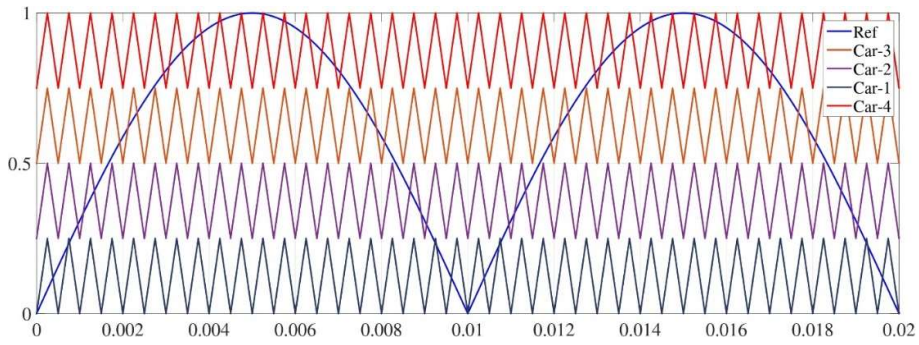
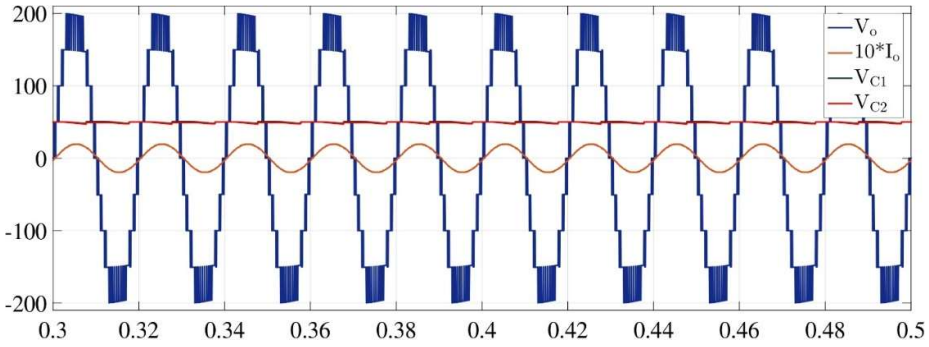
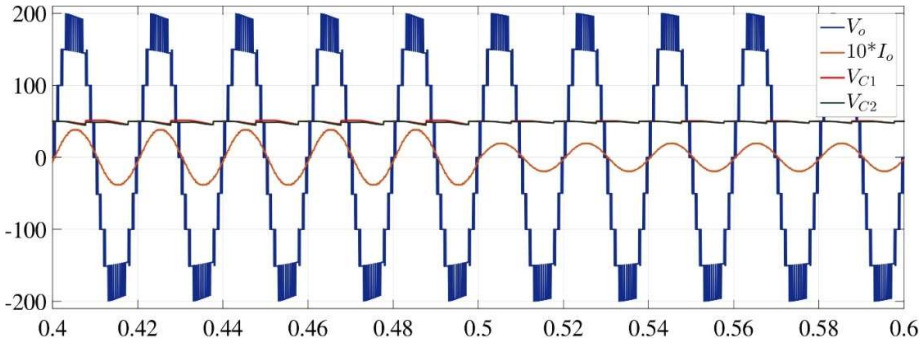


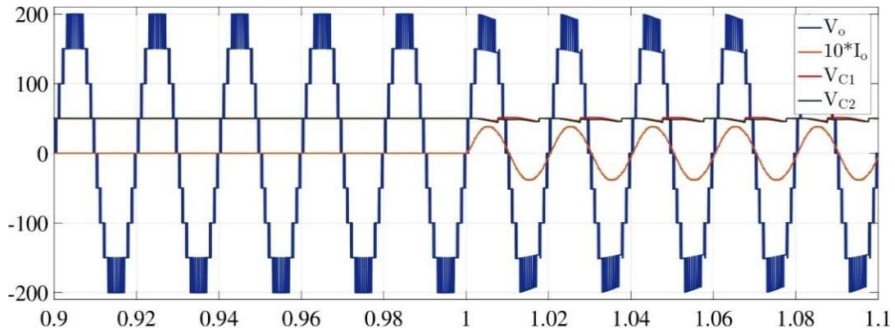
Figure 4.3 Reduced carrier PD-PWM technique



(a)



(b)



(c)

Figure 4.4 Simulation results at: (a) 30 Ω - 20 mH load, (b) transient change in load from 30 Ω - 20 mH to 60 Ω - 40 mH, (c) No to full load condition.

4.2 Simulation Results

The performance and working principle of the proposed DB-MLI topology are shown with the MATLAB simulation platform. Capacitors C1, C2 have the same value of 1.2 mF. Reference, switching frequency of 50 Hz 2.5 kHz, and the dc input supply voltage of 100 V are considered. Figure 4.4 illustrates the simulation outcomes of the suggested DB-MLI topology under different resistive, inductive loads at complete modulation index. The unfiltered output waveforms at 30 - 20 mH is pictured in Figure4. 4 (a). The unfiltered output voltage waveform of the proposed circuit has nine steps with a magnitude of 200 V and peak of the load current is around 6 A. C1, C2 balanced at its reference voltage magnitude of50 V each. Figure 4.4 (b), 4.4 (c) show the portrays at different load transients.

It is observed in the capacitors that the ripple has reduced when the load is increased. This ripple reduction is because of the increased time constant of the discharging interval. Output voltage waveform is unaffected in both the transient conditions and capacitors maintained their reference value. The THD value of the load voltage at 30 - 20 mH is 13.51 %. Since the 2 kHz switching frequency, predominant harmonics are pushed to (mf ± 1) order, i.e., 39th and 41st. The obtained THD spectrum is depicted in Figure 4.5.

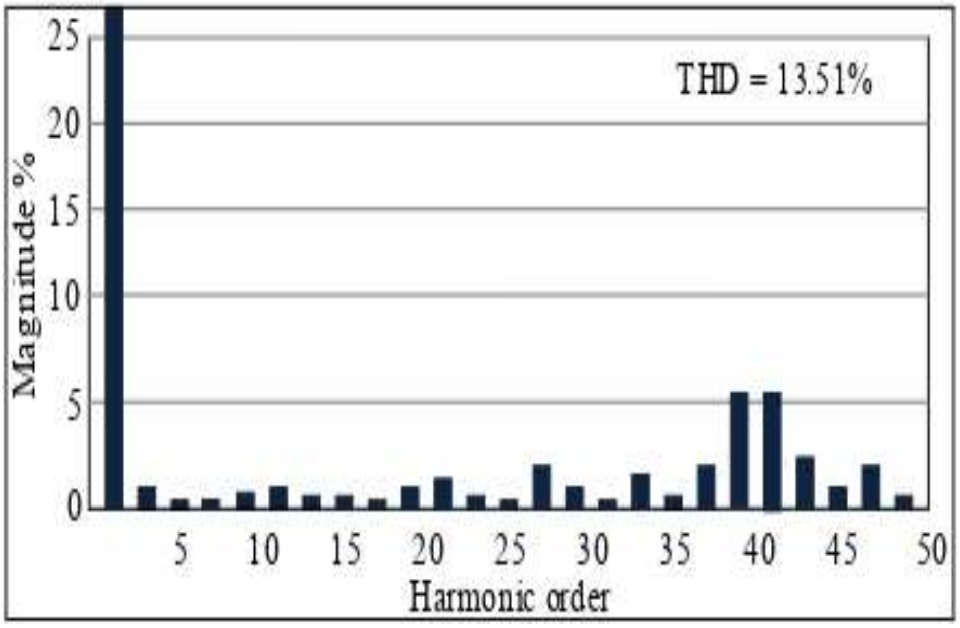


Figure 4.5 Fourier spectra of unfiltered output voltage

To furnish a comparative analysis on the proposed inverter circuit with established boost-based MLIs, the numbers of switching elements Nsw, capacitors NCap, and blocking voltages are incorporated in Table 4.2.

As witnessed, compared circuits have their component count larger than the proposed circuit except (Y.Ye et al.2014). The circuit in (Y.Ye et al.2014). needs fewer switches, but six diodes and H-bridge at the back-end produces high blocking voltage. Hence, the proposed circuit is a good preference for mining and industrial applications

Table 4.2 Comparison with recent topologies with proposed DB-MLI

Parameter	Topology								
	[5] (2018)	[3] (2014)	[9] (2018)	[8] (2018)	[7] (2019)	[13] (2018)	[4] (2016)	[10] (2019	Proposed
Nsw	14	8	17	19	17	12	13	19	11
Ndiode	2	6	-	-	5	4	-	-	-

Ncap	4	3	4	3	4	4	3	3	2
H-Bridge stress	2.5	4	-	-	-	-	4	-	-
PIV*Vdc	2.5	4	4	1	1	4	4	1	1
TSV	20	20	26	19	17	26	29	19	10

Nsw: no. of switches, Ncap: no. of capacitors, Ndiode: no. of diodes, TSV: total standing voltage, PIV: peak inverse voltage

4.3 The Proposed MLI - Three phase configuration for drive system

From the above, the proposed single-phase boost MLI design has been verified with RL load. Herein, the same has been extended to three phase with induction motor drive. Figure 4.6 show case the three-phase design with a switching configuration.

In similar to single phase system total of ten switches and two capacitors per phase are utilized. Herein, three set of single phase system with three DC sources are used and All though output voltages remain same but the MLI is connected to an induction motor drive. So here only the motor performance and its related parameters are estimated and verified with appropriate standard outcomes.

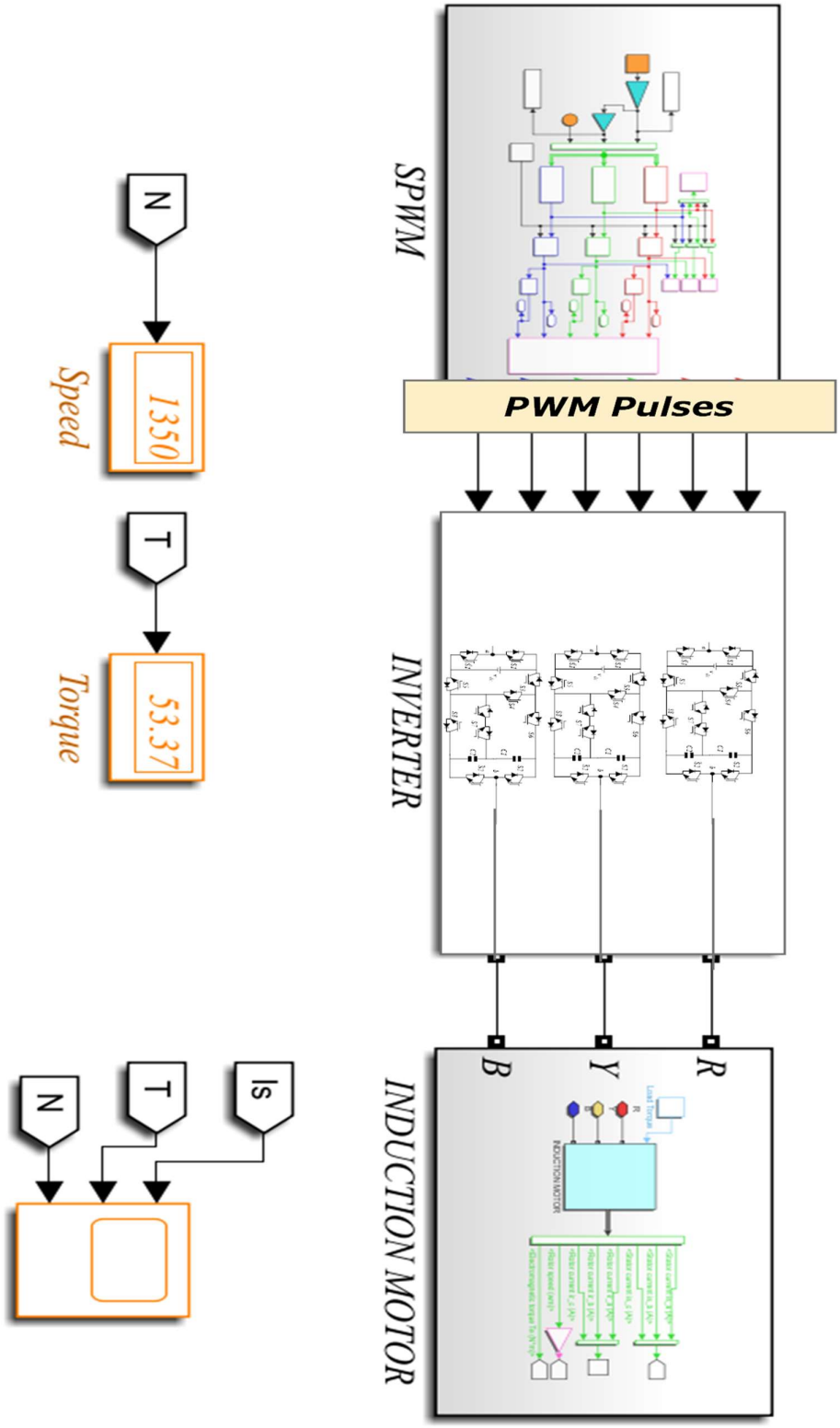


Figure 4.6 The proposed three-phase boost MLI with induction motor drive.

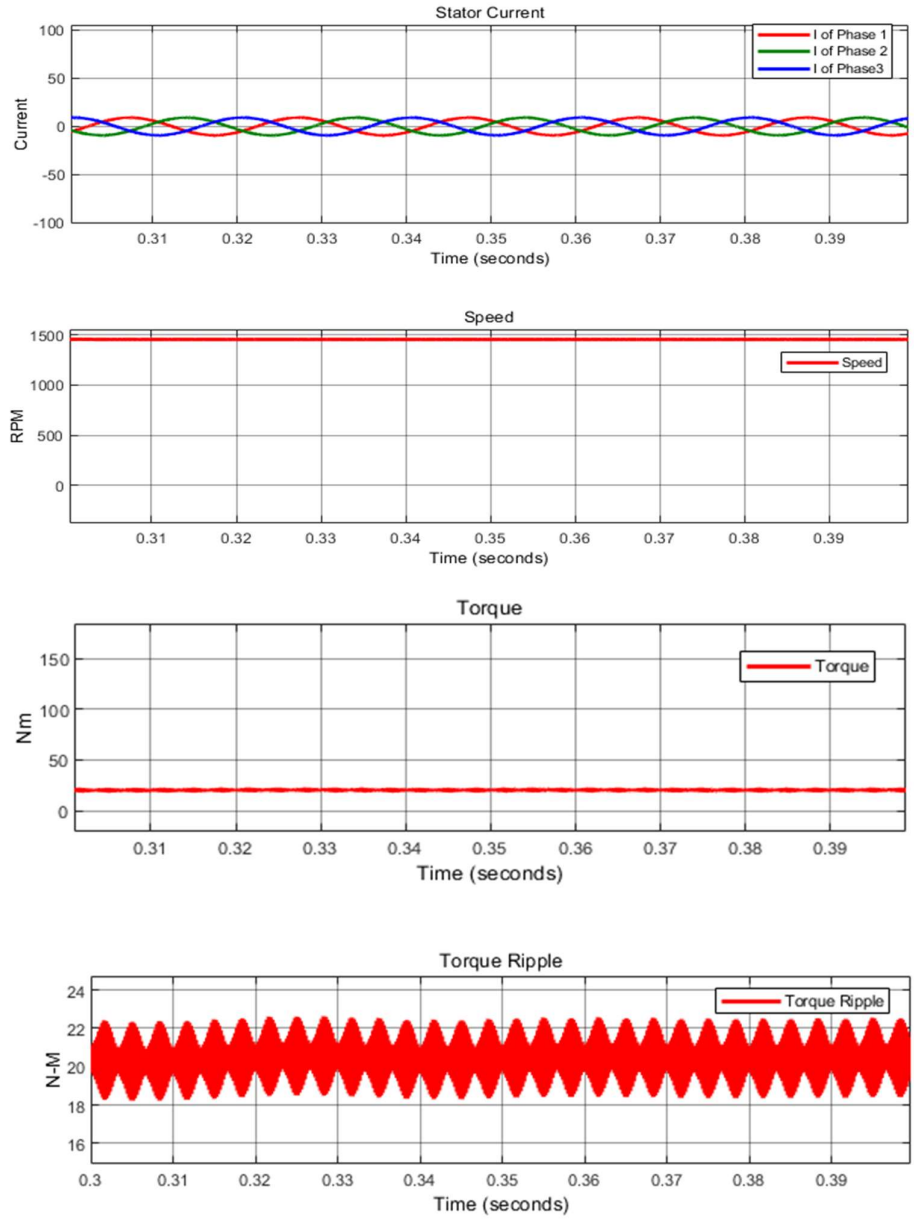


Figure 4.6.1 Details of stator currents, speed, torque and torque ripple (from top to bottom) TL =20 N/m

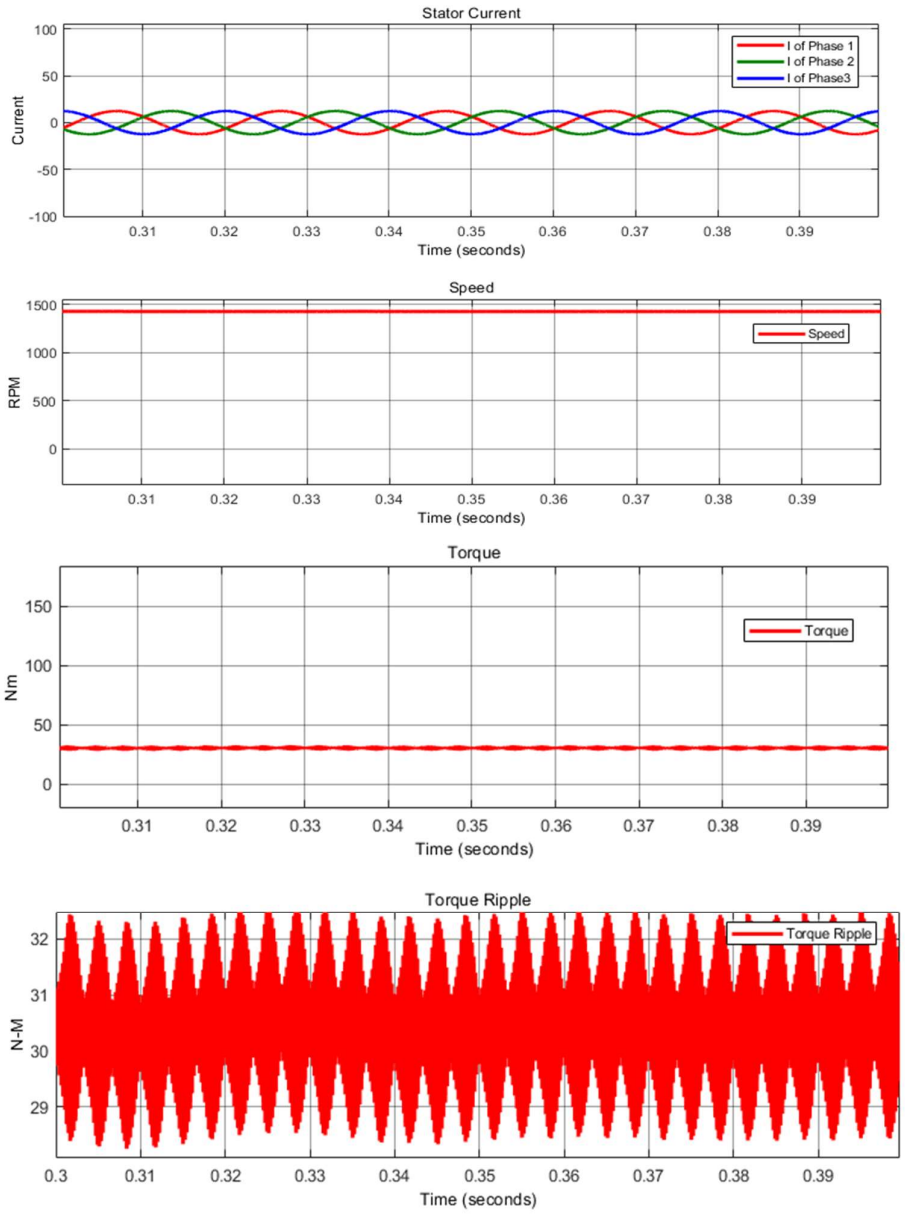


Figure 4.6.2 Details of stator currents, speed, torque and torque ripple (from top to bottom) at TL =30 N/m

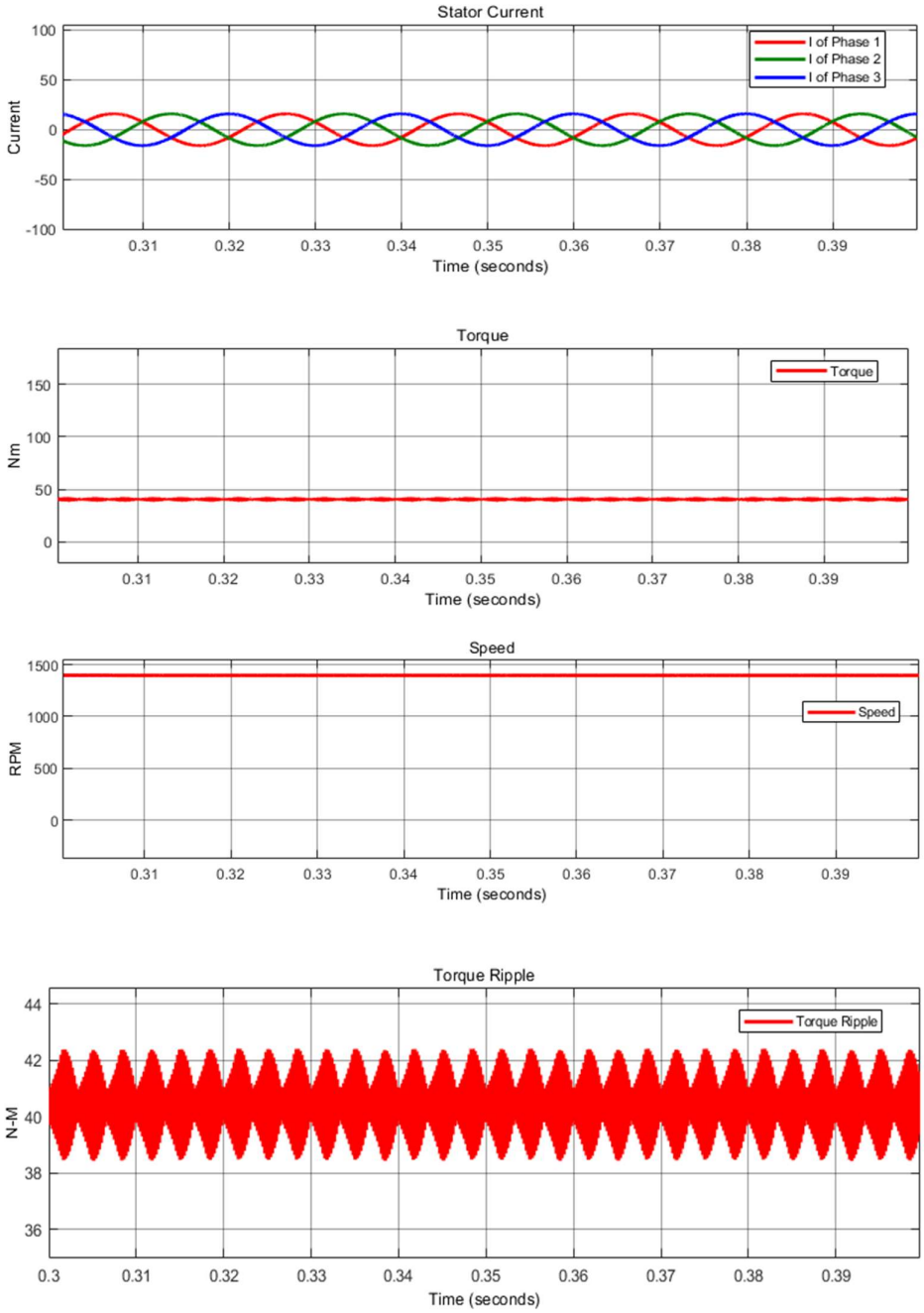


Figure 4.6.3 Details of stator currents, speed, torque and torque ripple (from top to bottom) TL =40 N/m

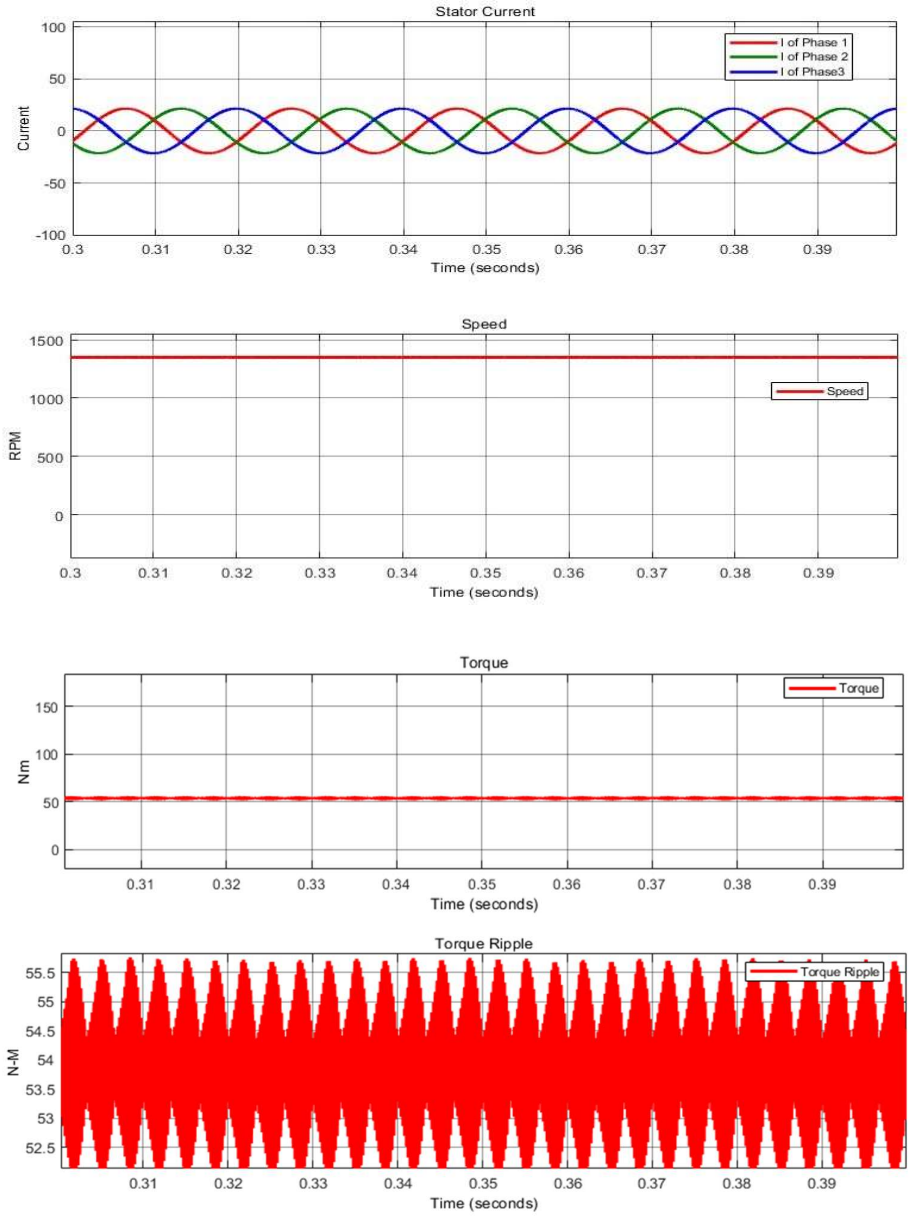


Figure 4.6.4 Details of stator currents, speed, torque and torque ripple (from top to bottom) TL =53.3 N/m

Figure 4.6.1, the drive outcomes like, auxiliary winding currents, torque ripple and rotor speed are portrayed. In terms of performance, torque ripple, output current and speed are important to estimate. As these three parameters signify the drive efficiency and thereby cost.

Coming to Figure 4.6.1, first parameter is winding current and it is around 0.573 A. Regarding, torque and speed are at 0.8 N-m & 1491 rpm respectively. In these particular details if we observe the torque ripple it is very minimal because of boost multi level inverter. Although traditional drive system operates with normal inverter configurations, but they showcase very high amount of torque ripples. In fact, torque ripples quite large in mining and Conveyers systems. These inherent issues may lead to failure of drive and labelled as one of the primary reasons for failures.

Further, Huge LC filter are used in the inverter drive for traditional systems where as in the proposed drive it is very minimum i.e.. in terms of Pico farads. This small filter is sufficient to eliminate high order harmonics. Further, the same verifications are extended for different load torques. in Figure 4.6.1 it is TL = 20 N/m, in Figure 4.6.2, 4.6.3 and 4.6.4 T_L is varied in the ranges of 30, 40 and 53.3 N/m. The key for the variation is, to estimate the drive performance at different speeds and the ripple associated at these conditions.

In all the cases the zoom version of torque ripple is presented in the bottom of the figures. If we observe the ripple at $T_L = 30$, it is varied in the range of 28.5 to 32.5 N/m. such variations are quite minimum for drilling operations. Further, at $T_L = 40$, it is varied in the range of 39 to 42. Even in this case variation is only 3 N/m. later, at $T_L = 53.3$, it varied in the range of 52 to 55.5 and this variation is around 3.5 N/m. thus, torque ripple is quite a minimal at different ranges of TL. This inherent benefit is retrieved from the MLI.

Table 4.3 Comparison of Traditional and proposed Inverter Drive Systems

Parameters	**Traditional Inverter**	**Proposed Inverter**
Torque ripple	Very high at higher torques	Very low
Current ripple and amplitude	Ripples are visible with higher magnitudes.	Ripples are visible with higher magnitudes.
LC filter	LC filter is a must for the traditional inverter	A very small value of LC filter is required (in terms of pf)
Output voltages and its waveform nature	Two level voltages are generated with common mode voltages and harmonics are very high and particularly lower order.	More than two level voltages are generated (without common mode voltages)
Stages for energy conversion	It is a two-stage conversion i.e. DC to DC and DC to AC. (DC link voltage needs 400 V for driving the induction machine so they use DC-DC boost)	The proposed MLI has an inherent boost so it is single-stage conversion equipment.
Voltage and current rating of switch	Voltage and current rating are very high as dv/dt stress is high over switches.	Very small ratings of switches are adequate for driving the MLI.
Complexity and flexibility	Simple in structure and flexible in design.	Simple in structure but complex in switching. However, they are flexible in nature
Standing voltage	Very high	Very low

Regarding drive, traction and mining-oriented loads, above parameters are key to evaluate the performance. Additionally, a comparative table is presented with traditional drive system by including same kind of analysis. From the table it can be concluded that proposed drive system far advanced for mining applications.

4.4 Summary

A dual boost nine-level inverter for mining applications is proposed in this work. Capacitors are used as virtual sources to boost the voltage magnitude and increase the levels. Additionally, the proposed MLI circuit inherits benefits such as self-balancing capacitors, less blocking voltage, and fewer components. A simple PD-PWM scheme is used to generate gating signals. Circuit portrayal, operating principle, modulation, and capacitor voltage ripples are studied. MATLAB software is used to carry out simulations, and the obtained outcomes prove the boosting ability under different loading circumstances. A detailed comparative review is conducted with other recent SCMLIs to illustrate the superiorities of the proposed circuit. Finally, the proposed design is extended for three-phase systems and the configuration of the three-phase boost MLI design is presented and verified with induction motor drive at different load torques.

CHAPTER-5

REAL-TIME VERIFICATIONS

Introduction

Boost MLIs for single-phase and three-phase systems have been verified in the previous chapter. Afterwards, a comparison between the proposed version and the traditional version is performed. Here, a real-time Hardware in Loop simulations is performed to validate the proposed MLI. As a matter of fact, HIL is a sophisticated validation setup to the Product developments of a new kind. The final designs of the companies, like ABB, Siemens, Rockwell Automation. etc., are validated using HIL. Design verification can be accomplished through HIL at an affordable price. An overview of HIL and the proposed boost MLI with induction drive is presented in the present chapter. In addition, a table of comparative results is included for benchmarking the proposed design in mining applications.

5.1 Details of HIL Simulator

In the context of hardware-in-the-loop simulations (HIL), FPGA devices are being used increasingly for real-time simulations. In various applications (C.Dufour et al.2012), HIL techniques are used in order to keep the budget impact to a manageable level during the development phase while running realistic tests on the actual hardware in a safe environment. These applications are best suited to FPGAs because of their high computational speed and fast I/O coupling capabilities. The HIL loop latency of the FPGA-based models in eFPGAsim in particular is taken very seriously, often considered a critical aspect in testing high-end motor controllers.

Models can be executed on FPGA and CPU using the RT-LAB real-time simulator. Most Simulink models and toolboxes, including Sim Power Systems, are supported on the CPU. OPAL-RT created eFPGAsim, a tailored collection of models and solvers for the FPGA.

The set of FPGA motor drive models that are now accessible in eFPGAsim as of Q2-2014 are:

FEA-based Permanent Magnet Synchronous Motor (PMSM, IPM) (Y.Inaba et al., 2011)

Switched Reluctance Motor (SRM) (S.Cense et al., 2011)

An induction motor or induction generator (IM/DFIM)

The model for the various machines is made to allow for online changes to all of the settings. Electric Hardware Solver, called a variable topology FPGA solver, is used to customise the power electronic component (eHS)

By enabling circuit and parameter modification with a single bit stream, the system is built for quick design iteration processes that reduce the time between design iterations to a few seconds. Machines and eHS are both created using floating-point math.

The system allows control engineers to validate prototype and production controllers in real-time using a virtual drive along with the connected power electronics.

The time step of the solver varies from 150 nanoseconds to one microsecond and the total latency between the IGBT firing signals and the voltages and currents outputs at the analogue outputs varies between 1 to 1.5 ps, user can implement himself any type of converter circuits with the eHS FPGA generic solver and the schematic editor of SimPower- System, PLECS and PSIM. Simple 2-level inverters for induction motor drives, buck, boost, H-bridge and SRM uni-directional converters for different mining applications or more complex power electronic circuits with high power converter such a matrix converters, 3-level NPC or flying-capacitor topologies for motor drives in traction system can easily be simulated with time step between 200 nanoseconds and 1 microsecond. The circuit topology and parameters can be modified on-the-fly in a few seconds without regenerating the FPGA bitstream, which save a lot of time.

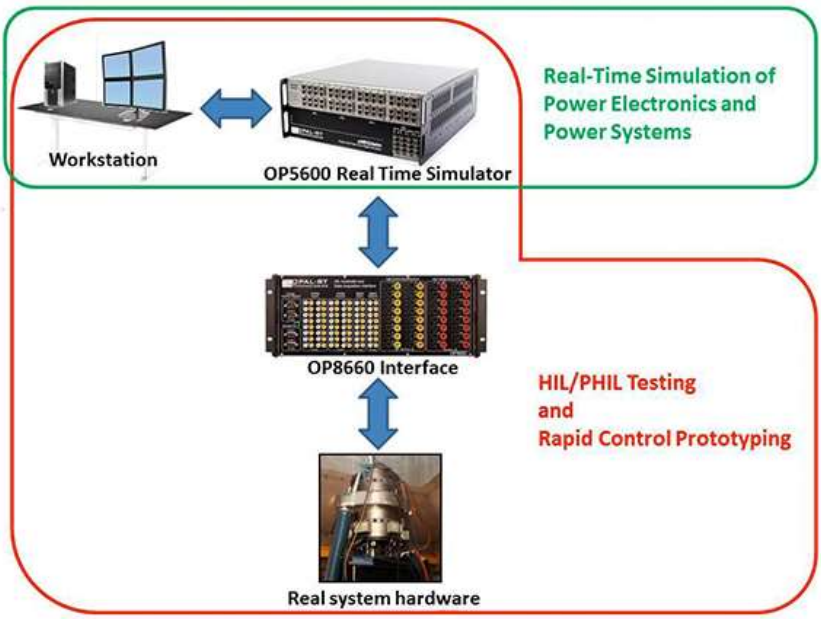


Figure 5.1 Details of HIL Simulator

5.2 Hardware verifications of the proposed single-phase boost MLI

In chapter 3, the proposed single phase MLI is verified through MATLAB Simulink. Herein, same is verified with Real Time Simulator (OPAL-RT -OP4200). Figure 5.2 shows the single phase proposed MLI setup for Real-time simulation. Total 10 switches and 2 capacitors are used. Entire network is drive with single supply. This is one of the finest merits in the proposed version.

As in advanced drive systems traditional MLI uses many dc sources. To accommodate separate dc supply additional rectifiers utilized. These arrangements are bulky and not recommendable to the drive operations which are in mining applications.

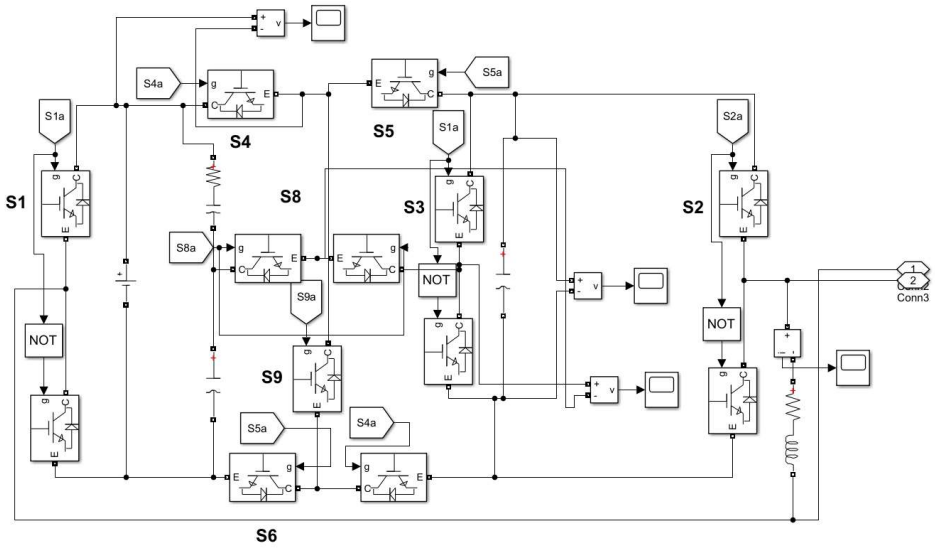
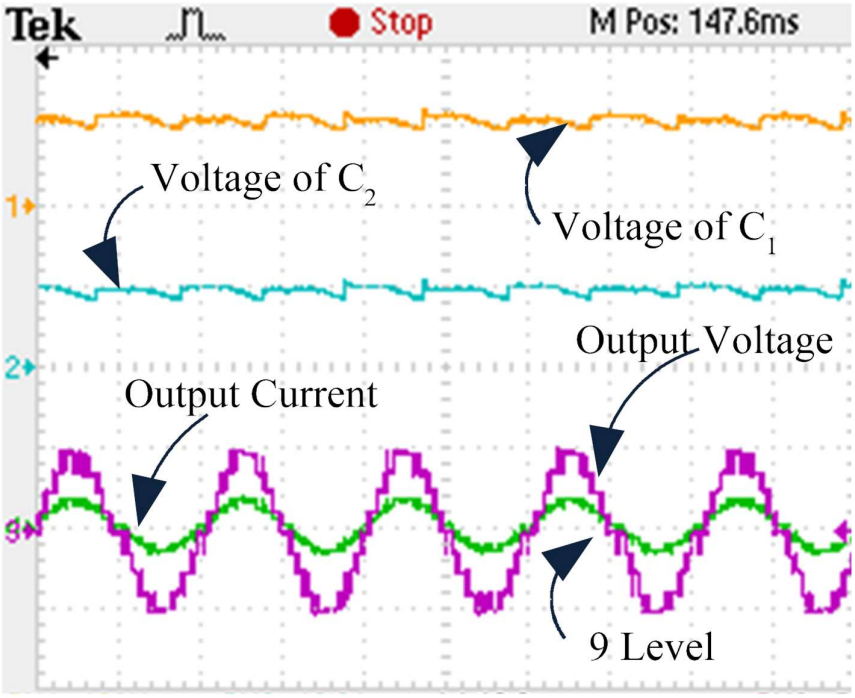


Figure 5.2 The proposed single-phase Boost – MLI.

Coming to the proposed version, dc supply of 100V is given as input, and operated at 2.5 kHz switching frequency. Output frequency is retrieved at RL load. The output is varied with modulation index range from zero to one. In this range nature of the waveform and magnitude is controlled. In other terms, controlling the speed of the drive is done through modulation index. At many instants, at lower modulation index drive strives hard to run because of insufficient torque pulsation. On the contrary, in the proposed topology such scenario is well controlled as torque ripple free. Additionally, Induction motor drive is quite smooth and driven in the ranges of 300 to 1490 rpm.

Figure 5.3 OPAL-RT setup



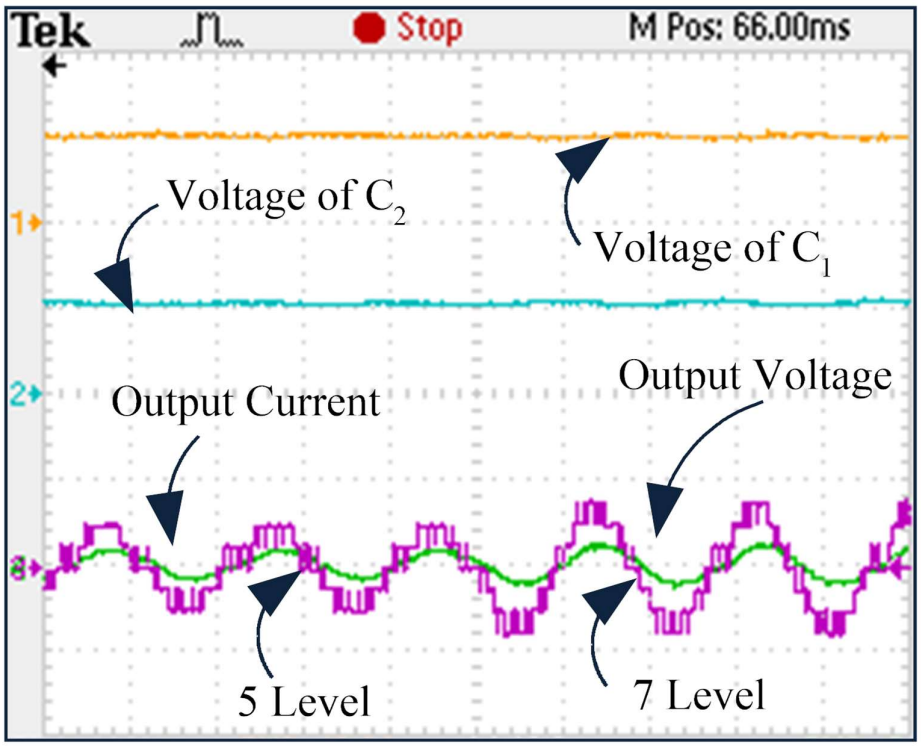
Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div)
Time scale:6 ms/div.

Figure 5.4 Hardware result for single phase boost MLI (ma = 1)

Further in Figure. 5.4, the proposed converter is operated at modulation index m_a equal to one. This information is presented in chapter 3. In the PWM switching when the reference wave touches the peak of the carrier wave then the entire nine levels are generated in the output end. On the other side, when the modulation index is varied to 0.7 the output can witness only seven levels. This is due to reference waveform varying over carrier waveform. Figure.5.5 shows the results at 0.75 modulations.

Further, in the same context, at the modulation index 0.5, the output voltage has only five levels. In the above verifications, RL load is utilized. Due to the RL load nature, the current waveforms are quite smooth and ripple free. Later, to validate the dynamic performance sudden variation is added. These variations are clearly visible in the current waveform rising from 0.5 to 1 A. current variations are very instantaneous and quite smooth without any sudden spikes in the output voltage. This is one of the greatest merits of drive applications. In many instants in induction motor drives

system witnesses sudden variations in loads while drilling, such variations can be handled smoothly. Finally, the capacitor variations are ripple-free and stiff during sudden variations. This indirectly implies boosting effects are not changed during critical instants. As aforementioned many of the traditional boost MLIs are observed with massive ripples in the capacitor voltage (range of 10% in the overall voltage). This kind of phenomenon is mainly



Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div) Time scale:6 ms/div.

Figure.5.5 Hardware result for single phase boost MLI (ma = 0.5 & 0.75)

due to PWM switching and design. Whereas in the proposed topology, PWM switching is currently designed in such a way that the design handles the capacitor to charge in the proper direction and thereby ripple-free.

5.2.1 Hardware verifications of the proposed three-phase boost MLI

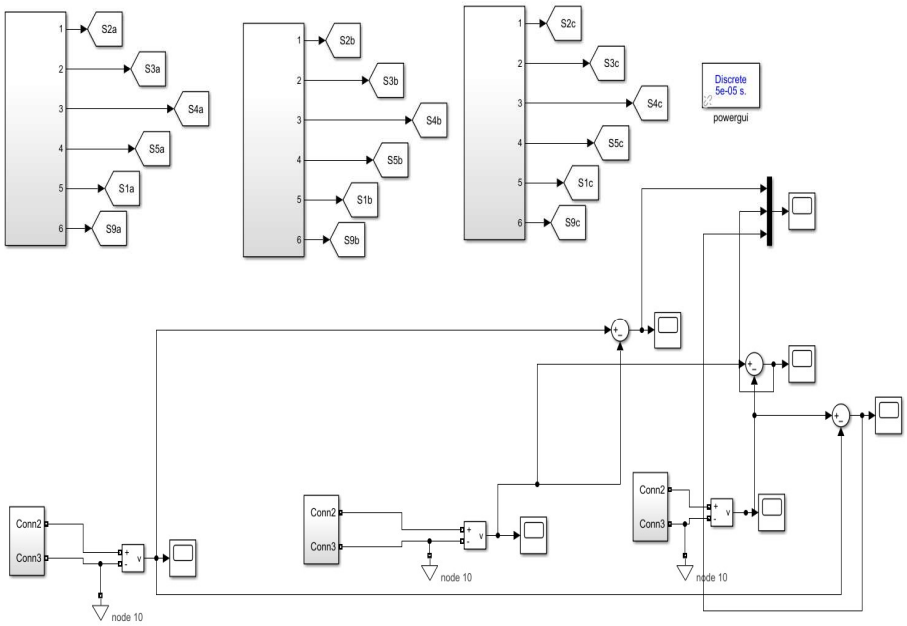


Figure 5.6 The proposed three-phase Boost – MLI.

The details of the proposed three-phase boost MLI are shown in Figure 5.6, 5.7 and 5.8 shows the performance of the boost MLI at modulation index 1. On observing the voltage and current waveforms, a total of nine levels are generated. In all the three-phase, nine levels are observed consistently with slight variations. Further, a resistive load is used to verify the nature of the current. In the HIL (hardware ware in loop) verifications, LC filter is completely absent; still the output currents are quite sinusoidal in fashion. On the other side, if the same kind of analysis is carried out in a traditional inverter; square or quasi-waveforms are observed. This has been mentioned in chapter 1. Moreover, THD values are also a very important factor in evaluating the inverter performance. As the proposed converter is designed and targeted for motor drives, a 1 Hp motor is used for verifications. As in chapter 3 verifications are presented for a traditional inverter with an induction motor drive. Herein, similar tests are conducted to boost MLI with an asynchronous induction motor. At the cost repetition, once again the point needs to be remembered i.e., “the design is targeted for mining applications and in this criterion asynchronous induction motor is the correct choice for the evaluation of the proposed MLI.

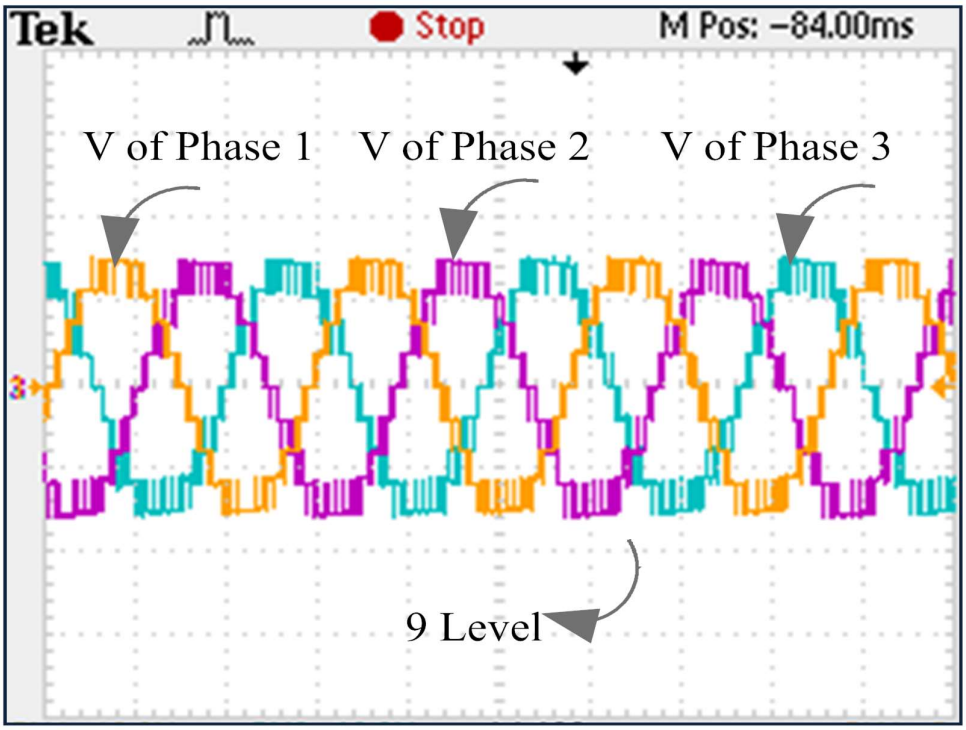
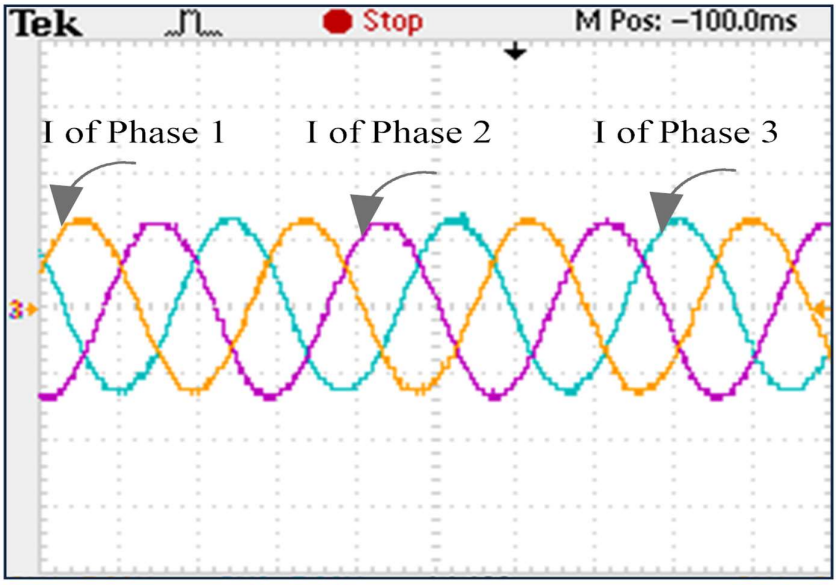


Figure 5.7 Details of Three-phase output voltage waveforms for the proposed boost MLI (ma = 1)



Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div) Time scale:6 ms/div.

Figure 5.8 Details of three phase currents for proposed boost MLI (ma = 1)

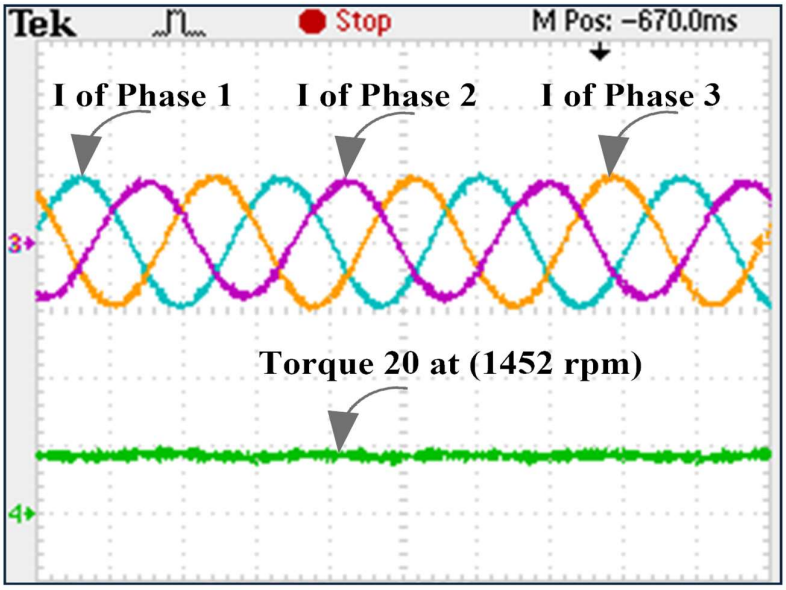
5.3 Three-phase verifications of the proposed boost MLI with different load torque

As aforementioned, speed torque variations are crucial for induction motor drives. So, to evaluate the same with the proposed MLI, four different load conditions are taken. In the first condition, T_L is set for 20 N/m and it is varied up to 53.3 N/m.

In the first condition, at T_L= 20 N/m the three-phase currents, speed and torque ripple are retrieved from HIL verifications and this is presented in Figure 5.9. on observing, the details of Figure5.9 a, the three-phase currents are stable and ripple free, and torque ripple variations are very low and at this instant and speed of the machine is 1452 rpm. Thus, at lower torques speed will be higher and in this case, speed is settled at 1452 rpm as the chosen machine is a 5.4 Hp drive. Similarly, at T_L = 30, three-phase currents, speed and torque ripple are retrieved and this is presented in Figure 5.10. on observing the results, speed is slightly reduced and torque has been increased at this instant, torque ripple also diminished drastically without many variations. In fact, multilevel inverters played a crucial role in suppressing the torque ripple because

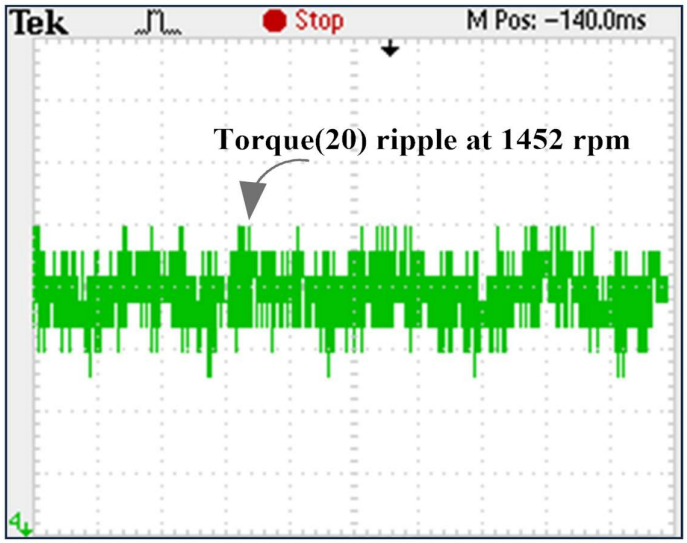
of their voltage levels. In a similar fashion, torque at 40 and 53.3 is presented in Figure 5.11 and 5.12. both the results confirm the variation of speed and torque and at this instants torque ripple is quite low and speed has also fallen from 1452 to 1350 (i.e TL = 20 to TL=53.3). In overall, the induction machine speed varied smoothly without much fall with respect to torque.

The three-phase currents also confirm the smooth performance of the machine. Many times, in mining applications current waveforms suggest the quality of the machine and functioning. Because drive sound and hissing noise are dependent on the current amplitudes and waveform nature. The more the currents are drawn, the large variations in the current profile are witnessed. However, in the present verifications, such variations are not observed. it's all because of the proposed boost MLI.



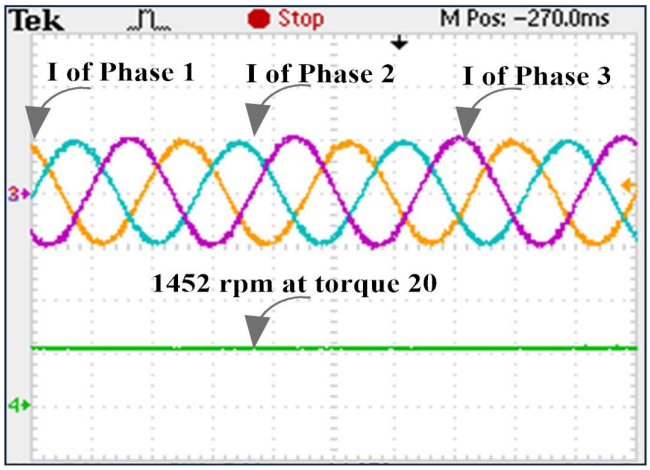
Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div)
Time scale:6 ms/div.

(a)



Details of output voltage (Scale: 60 V/div),
output current(Scale:5A/div)
Time scale:6 ms/div.

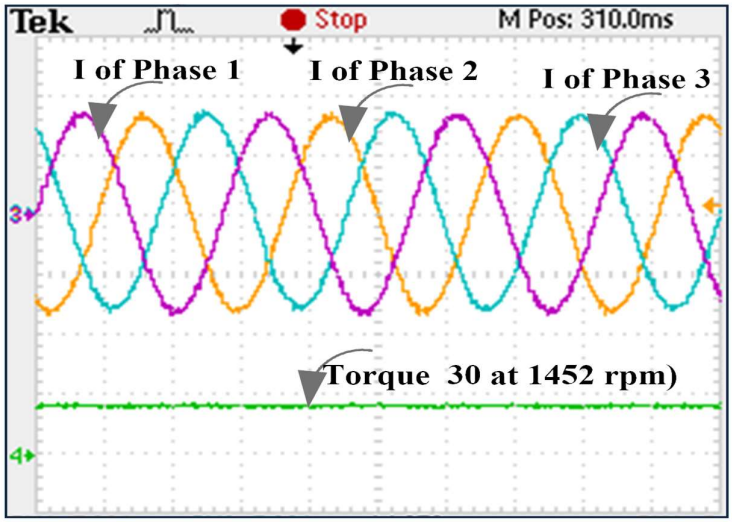
(b)



Details of output voltage (Scale: 60 V/div),
output current(Scale:5A/div)
Time scale:6 ms/div.

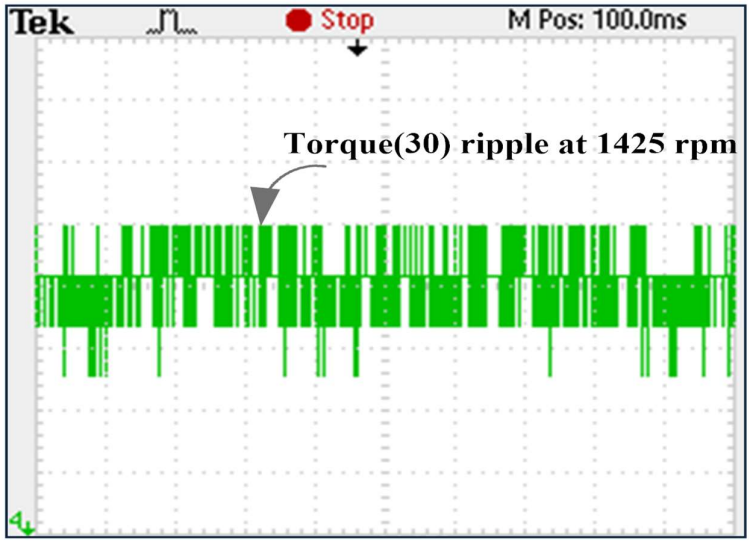
(c)

Figure 5.9 The details of a) three-phase currents and torque b) Torque ripple c) three currents and speed in rpm.



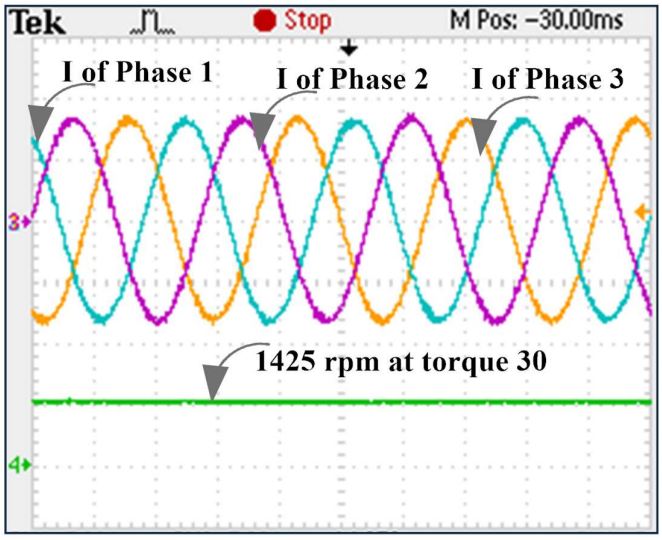
Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div) Time scale:6 ms/div.

(a)



Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div) Time scale:6 ms/div.

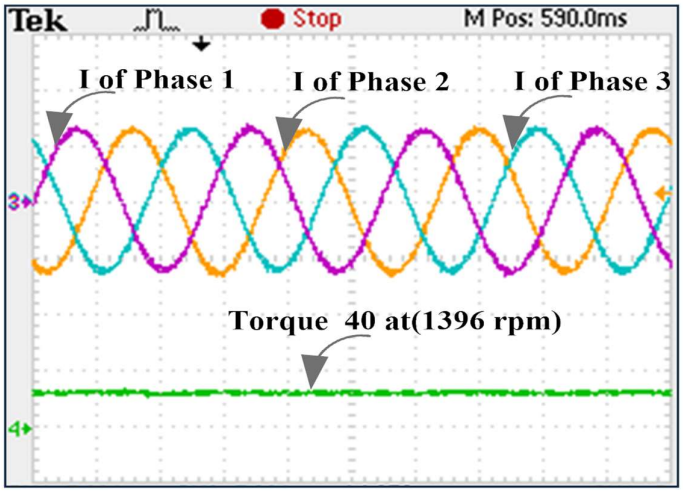
(b)



Details of output voltage (Scale: 60 V/div),
output current(Scale:5A/div)
Time scale:6 ms/div.

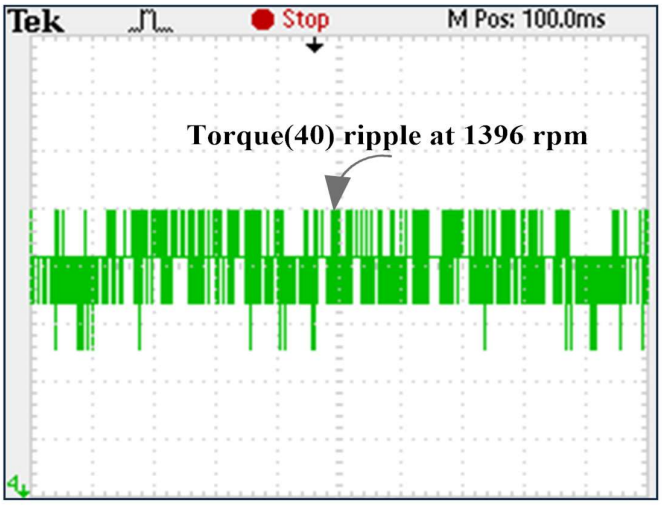
(c)

Figure 5.10 The details of a) three-phase currents and torque b) Torque ripple c) three currents and speed in rpm.



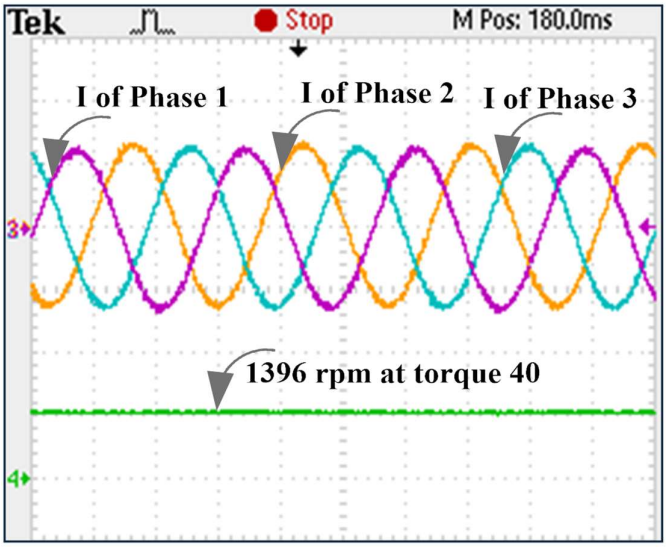
Details of output voltage (Scale: 60 V/div),
output current(Scale:5A/div)
Time scale:6 ms/div.

(a)



Details of output voltage (Scale: 60 V/div),
output current(Scale:5A/div)
Time scale:6 ms/div.

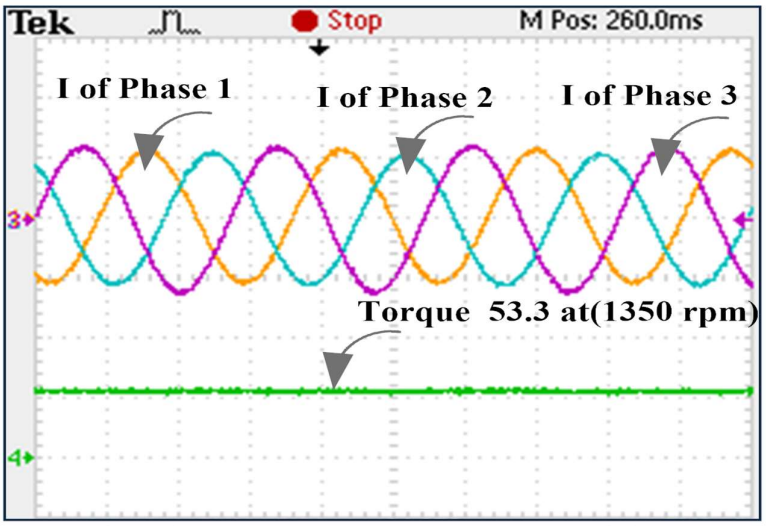
(b)



Details of output voltage (Scale: 60 V/div),
output current(Scale:5A/div)
Time scale:6 ms/div.

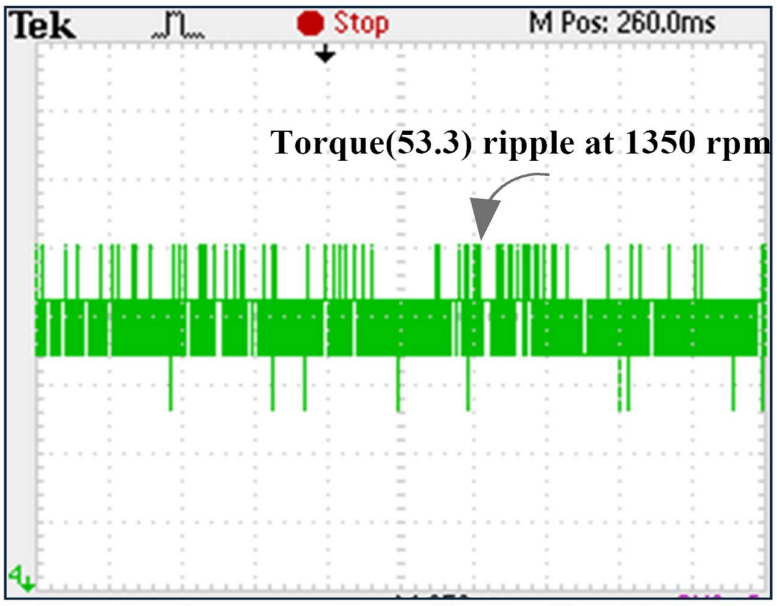
(c)

Figure 5.11 The details of a) three-phase currents and torque b) Torque ripple c) three currents and speed in rpm.



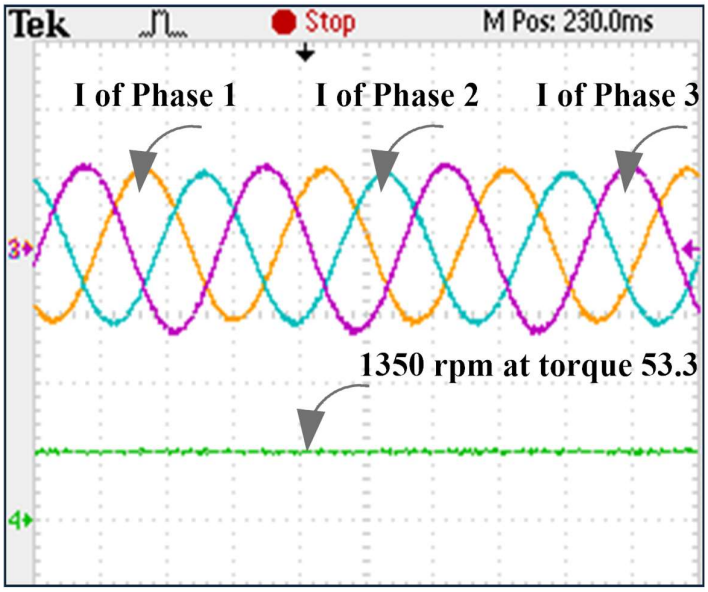
Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div) Time scale:6 ms/div.

(a)



Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div) Time scale:6 ms/div.

(b)



Details of output voltage (Scale: 60 V/div), output current(Scale:5A/div)
Time scale:6 ms/div.

(c)

Figure 5.12 The details of a) three-phase currents and torque b) Torque ripple c) three currents and speed in rpm.

Sample Calculations:

Types of torques in induction motor

T_a =gross mechanical torque (or) motor torque

T_{lost} = loss torque due to friction,windage and iron losses.

T_{sh} (or) T_L = load torque

$$T_a = T_{lost} + T_{sh}$$

Power (P_{out}) = $T_{sh} * \omega$

$$T_{sh} = Pout/\omega$$

Pout = 4000 watts

$$\omega = 2\Pi N/60$$

$\omega = 2\Pi*1430/60$

$= 149.67$ rad/sec.

$T_{sh} = 4000/149.67$

T_{sh} (or) $T_L = 26.72$ N-m,

$T_L / 2 = 13.36$ N-m,

$T_L / 4 = 6.68$N-m

Table 5.1Speed and motor torque values for different load conditions

Load torque(T_L) in N-m		**Motor torque(T) in N-m**	**Speed(N) in RPM**
T_L at sec	T_L=20	19.89	1452
T_L at 5sec	T_L =30	29.91	1425
T_L at 10sec	T_L =40	39.72	1396
T_L at 13sec	T_L =53.3	52.9	1350

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

The following conclusions are proposed as a part of the research work:

6.1. Conclusions

1. This thesis has provided advanced power converters circuit topologies (H7, H8, and Boost Multilevel Inverter) and their analysis with respect to induction motor drives. Former topologies H7 and H8 have their own mixture of advantages and disadvantages.
2. In particular, for mining applications like drilling, tractions, and elevators H7 and H8 are simple in structure. However, H7 and H8 can able to generate two levels of output voltage.
3. Two-level inverter creates common mode voltage and harmonic issues in the output terminals are demerits and to address them huge LC filters are needed to generate the quality waveforms.
4. The speed-torque response for the traditional inverter is not satisfactory. Torque ripple is around 10% and this ripple will drastically affect the drive performance. To confirm this aspect experimentation is done with different variables.
5. To overcome the disadvantages mentioned earlier, a single-stage boost Multi-Level Inverter (MLI) has been developed for use in mining applications.
6. The proposed Single-stage boost MLI circuit design, operation, and simulation studies are presented in Chapter 4. On observation, the proposed boost multilevel inverter outperforms traditional ones and can operate effectively for drilling, traction, and mining applications.
7. To confirm the performance, extensive simulations have been conducted, and a comparative table has been provided. Subsequently, the same approach is expanded to include three-phase configurations under various loading conditions. In this context, the selected loads consist of RL circuits and an induction motor drive. Additionally, the PWM switching strategy is also applied for the proposed topology which further enhanced the performance of

the drive and it also witnessed the reduction of lower order harmonics in the output terminal (without LC filter)

8. Finally, in the fifth chapter we have examined the proposed topology in the Real real-time domain with OPAL-RT. The details of the real-time simulator and its importance have been given in detail in Chapter 5.
9. Further, the three-phase proposed boost inverter has been verified in Real-time, and in this case variable loads (RL and induction motor drive) are used and torque-speed characteristics are retrieved. From the observations, voltage and current quality from the proposed MLI is harmonic free and more over torque ripples and speed are quite satisfactory for mining applications.

6.2 Future scope

In future, the proposed boost multi-level inverter can be redesigned with a lesser number of switches and a new switching strategy can be used to enhance the output performance. Moreover, it can be integrated with renewable energy sources for extracting and converting energy. The power density of multilevel inverters can be enhanced by employing new semiconductor devices, advanced cooling techniques, and improved circuit layouts to achieve higher power levels in a compact form.

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List of Publications based on Ph.D. Research Work

Sl. No.	Title of the paper	Authors (In the same order as in the paper. Underline the Research Scholar's name)	Name of the Journal/ Conference/ Symposium, Vol., No., Pages	Month &Year of Publications	Category *
1	Leakage Current Mitigation in Transformer- Less Photo Voltaic Inverter Systems For Mining Equipment	N V V Prudhvi Krishna B, B.M.Kunar, Ch. S. N. Murthy	International Journal of Innovative Technology and Exploring Engineering, Vol. 9 (2), 2932--2937 (Scopus)	December 2019	1
2	A Switched-Capacitor Based Nine-level Boost Inverter Circuit for Mining Applications	N V V Prudhvi Krishna B, B.M.Kunar, Ch. S. N. Murthy	Second international conference on advances in electrical, Computing ,communication and sustainable technologies (ICAECT2022) (IEEE)	21-22 April 2022	3
3	Simulation and real time Studies on three phase Boost multi level inverter	N V V Prudhvi Krishna B, B.M.Kunar, Ch. S. N. Murthy Y.Suresh	Expert Systems	Communicated	1
4	A Switched-Capacitor Based Seventeen-level Boost Inverter Circuit for Mining Applications	N V V Prudhvi Krishna B, B.M.Kunar, Ch. S. N. Murthy Y.Suresh	Third international conference on advances in electrical, Computing ,communication and sustainable technologies (ICAECT2023) (IEEE)	Communicated	3

*Category: 1: Journal paper, full paper reviewed 2: Journal paper, Abstract reviews 3: Conference/Symposium paper, full paper reviewed
4: Conference/Symposium paper, abstract reviewed 5: Others (including papers in Workshops, NITK Research Bulletins, Short notes etc.)
(If the paper has been accepted for publication but yet to be published, the supporting documents must be attached.)

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