Voltage Sag Compensation Technique for Three-Level Voltage Source Inverter based Dynamic Voltage Restorer

Vijayan Immanuel
Department of Electrical & Electronics Engineering,
National Institute of Technology Karnataka, Surathkal, India
vijayan@nitk.ac.in

Gurunath Yankanchi
Bharat Heavy Electricals Ltd.,
Trichy, India
gurunath@bheltry.co.in

Abstract-This paper presents a voltage sag compensation technique for Dynamic Voltage Restorer (DVR). An effective Space Vector Modulation (SVM) technique is implemented using Three-Level Diode Clamped Voltage Source Inverter (VSI) configuration. Extensive simulations of various test conditions indicate that the voltage sag compensation is seamless with negligible Total Harmonic Distortion (THD).

I INTRODUCTION

Voltage sags are most common power quality issues which occur in a power system. Voltage sag is characterized by magnitude (depth) and duration. Sag is a decrease to between 0.1 and 0.9 p.u. in RMS value at the power frequency for durations of 0.5 cycles to 1 minute. Sag is also defined as a voltage magnitude event with a magnitude less than the nominal voltage and a duration between 0.5 cycles and a few seconds. Computers, consumer electronics, process control equipment and adjustable-speed drives (both ac and dc) are perceived as most sensitive to voltage sags [1]. The Dynamic Voltage Restorer (DVR) is a series connected power quality device, which primarily can protect sensitive electric consumers against voltage sags and surges in the medium and low voltage distribution grid [2, 3]. The basic idea of the DVR is to inject a dynamically controlled voltage in series with the bus voltage. The momentary amplitudes and phases of the three injected phase voltages are controlled such that the load is protected from the detrimental effects of sag or swell. In effect, the DVR is basically a VSI which compensates the voltage sags/swells by rapidly injecting a set of three phase voltages into the lines via booster transformer. Among the key points of concern in the implementation of DVR are sag compensation capability and harmonics [4]. The DVR has to be effective in compensating voltage sags associated with phase jump.

The basic control approaches are pre-sag compensation (voltages at load end are restored to pre-sag values), in-phase compensation (voltages at load end are compensated and in phase with sagged voltage) and energy optimal compensation (voltage injected in quadrature to load current) to minimize energy injection [5]. A hybrid approach is suggested where upon the occurrence of sag, the voltage is initially restored to pre-sag magnitude and phase. Then, the load voltage is gradually shifted to be in phase with the post-sag voltage vector, thus decreasing the voltage injection requirement [6]. However in this approach, generation of reference compensation voltages uses the synchronous reference frame method with Software Phase Locked Loop (SPLL), which introduces a delay in tracking the new network angle if the sag is associated with phase angle jumps. This delay affects the dynamic response of DVR. A simpler and effective algorithm for calculating the reference compensating voltages using PQR power theory is proposed in [7], where the reference compensating voltages are generated without any time delay.

Multi-level inverter technology has emerged as an important alternative in high-power medium-voltage control applications. With the use of gate-turn-off high voltage semiconductor devices, Voltage Source Inverters (VSI) will be increasingly used in distribution voltage level applications [8]. The type of modulation techniques employed determines the RMS value of the output fundamental and the harmonic content of the output voltage waveform. The Space Vector Modulation (SVM) offers a significant advantage in the flexibility to optimize switching waveforms. Reference [9] proposed a computationally efficient SVM algorithm for general n-level inverters.

This paper proposes an effective voltage compensation scheme for the DVR. The reference compensation voltages are calculated using the approach in [7]. A Space Vector Modulation (SVM) technique is applied to a three-level diode clamped VSI to generate compensation voltages without time delay and with negligible Total Harmonic Distortion (THD).

II COMPENSATION SCHEME

The overall schematic of the DVR system is shown in Fig. 1. The main components of DVR are controller, voltage source inverter, energy source for DC link capacitor, filters and booster transformers.

During normal voltages in the line, the DVR has to be inactive in the sense that the voltage injection is zero. Upon the occurrence of voltage sag, the unbalanced voltages have to be processed to calculate the reference compensation voltages for the compensation scheme. The reference compensating voltages are generated in the p-q-r domain and transformed back into o-α-β coordinates. The reference voltages are given as inputs to drive the space vector modulator. The firing pulses are generated for a three-level diode clamped VSI. The block diagram for the control flow is shown in Fig. 2.

1-4244-0497-5/06/$20.00 © 2006 IEEE

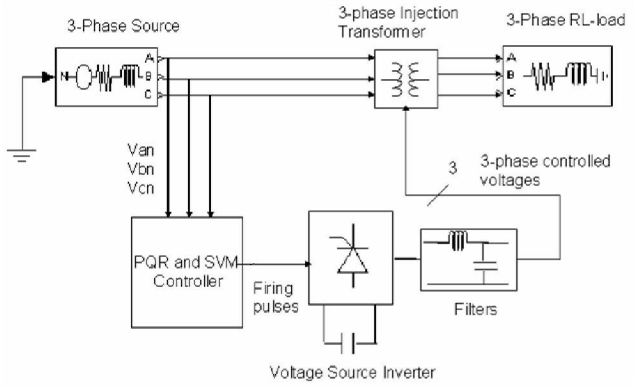

Fig. 1. Schematic of DVR System

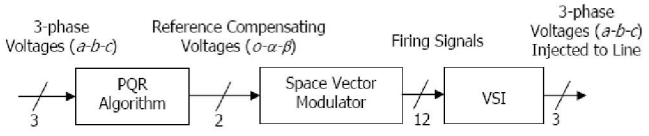

Fig. 2. Block Diagram of Control Flow

A. Generation of Reference Compensation Voltages [7]

The phase voltages of three-phase a-b-c coordinates can be transformed to o-α-β coordinates as given in (1).

$$\begin{pmatrix} v_o \\ v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \tag{1}$$

If sinusoidal balanced voltages v_{aREF}, v_{bREF} and v_{cREF} are selected for the reference waves in the a-b-c coordinates, the reference waves in o-α-β coordinates are as defined in (2).

$$V^{REF} = \begin{pmatrix} v_{\alpha REF} \\ v_{\beta REF} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{pmatrix} v_{aREF} \\ v_{bREF} \\ v_{cREF} \end{pmatrix} \tag{2}$$

Since the reference waves v_{aREF}, v_{bREF} and v_{cREF} are sinusoidal balanced, the o-axis component voltage v_{oREF} does not exist and the reference waves $v_{\alpha REF}$ and $v_{\beta REF}$ are sinusoidal and orthogonal on the in α-β plane. Using the reference waves $v_{\alpha REF}$ and $v_{\beta REF}$ in the o-α-β coordinates in a mapping matrix, the voltages in o-α-β coordinates can be transformed to p-q-r coordinates as shown in (3).

$$\begin{pmatrix} v_p \\ v_q \\ v_r \end{pmatrix} = \begin{pmatrix} 0 & \frac{v_{\alpha REF}}{v_{\alpha\beta REF}} & \frac{v_{\beta REF}}{v_{\alpha\beta REF}} \\ 0 & -\frac{v_{\beta REF}}{v_{\alpha\beta REF}} & \frac{v_{\alpha REF}}{v_{\alpha\beta REF}} \\ 1 & 0 & 0 \end{pmatrix} \begin{pmatrix} v_o \\ v_\alpha \\ v_\beta \end{pmatrix} \tag{3}$$

where, $v_{\alpha\beta REF} = \sqrt{v_{\alpha REF}^{\ 2} + v_{\beta REF}^{\ 2}}$.

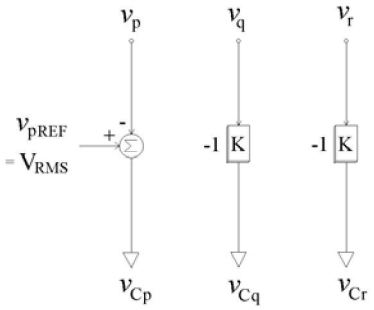

Fig.3. Block diagram for calculation of Compensating Voltages

Combining equations (1) and (3), the voltages in a-b-c coordinates can be transformed to p-q-r coordinates as expressed in (4).

$$\begin{pmatrix} v_p \\ v_q \\ v_r \end{pmatrix} = (C) \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \tag{4}$$

where $C = C_1 C_2$ and

$$C_1 = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}; \quad C_2 = \begin{pmatrix} 0 & \frac{v_{\alpha REF}}{v_{\alpha\beta REF}} & \frac{v_{\beta REF}}{v_{\alpha\beta REF}} \\ 0 & -\frac{v_{\beta REF}}{v_{\alpha\beta REF}} & \frac{v_{\alpha REF}}{v_{\alpha\beta REF}} \\ 1 & 0 & 0 \end{pmatrix}. \tag{5}$$

The block diagram for calculation of the compensating voltages is shown in Fig. 3. $v_{Cp} = v_{pREF} - v_p$ is compensated for the p-axis. $v_{Cq} = -v_q$ and $v_{Cr} = -v_r$ are compensated for the q-axis and r-axis respectively. The reference value for the p-axis v_{pREF} is equal to RMS value of the rated line voltage V_{RMS}. With this reference value, the magnitudes of the output terminal voltages are regulated to the constant rated line voltage V_{RMS}. The reference compensation voltages are calculated without time delay. These can be transformed back to o-α-β domain using the transformation given in (6) and (7).

$$\begin{pmatrix} v_{Co}^{\ *} \\ v_{C\alpha}^{\ *} \\ v_{C\beta}^{\ *} \end{pmatrix} = (C_2)^{-1} \begin{pmatrix} V_{RMS} - v_p \\ -v_q \\ -v_r \end{pmatrix} \tag{6}$$

where,

$$C_2^{-1} = \begin{pmatrix} 0 & 0 & 1 \\ \frac{v_{\alpha REF}}{v_{\alpha\beta REF}} & -\frac{v_{\beta REF}}{v_{\alpha\beta REF}} & 0 \\ \frac{v_{\beta REF}}{v_{\alpha\beta REF}} & \frac{v_{\alpha REF}}{v_{\alpha\beta REF}} & 0 \end{pmatrix} \tag{7}$$

B. Space Vector Modulation Technique for Three-Level Diode Clamped VSI Topology

The functional diagram of a three level VSI switching network is shown in Fig. 4. Each switch will assume one of

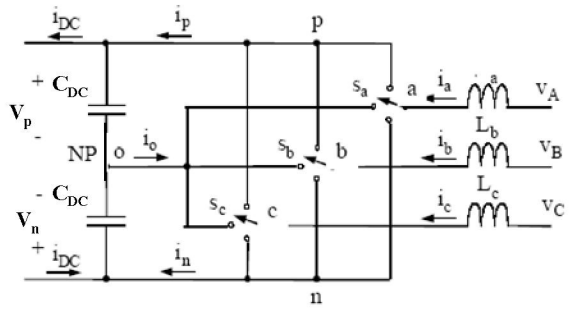

Fig. 4. Switching Network of a Three-Level VSI

three positions. For instance, S_a may be connected to positive DC rail point '*p*', negative DC rail point '*n*' or neutral point (NP) '*o*'. Each switch combination produces a unique voltage vector and can be represented as space voltage vector in one plane. The space voltage vectors are shown in Fig. 5. The vector names represent the allowable switching states, e.g., '*pon*' means switch S_a is connected to positive DC rail, S_b is connected to NP and S_c is connected to negative DC rail. There are totally 3^3 (27) allowable switching state vectors which corresponds to 6-large vectors, 6-medium vectors, 12-small vectors and 3-zerovoltage vectors. Fig. 6 is a representation of how the switching states and triangles are numbered. The numbers at the centre of triangle represent the triangle number and those at the vertices represent the switching state. The diagram contains a total of 24 triangles and tip of the reference vector may lie in any one of these triangles. The modulation scheme has to decide the switching state and the duty cycle in order to synthesize the reference voltage vector. An effective way to synthesize the voltage reference vector is by using the nearest three vectors (NTVs) as defined in (8).

$$V_{REF} = d_1 V_1 + d_2 V_2 + d_3 V_3 \tag{8}$$

where d_1, d_2 and d_3 are the duty cycles of the vectors V_1, V_2 and V_3 respectively, with the additional constraint on duty cycles defined by (9).

$$d_1 + d_2 + d_3 = 1 \tag{9}$$

C. Identification of Nearest Three Vectors (NTVs)

The first step the modulator needs to perform is to identify the NTVs, which is to identify the small triangle in which the tip of the reference vector V_{REF} is located. The approach is to

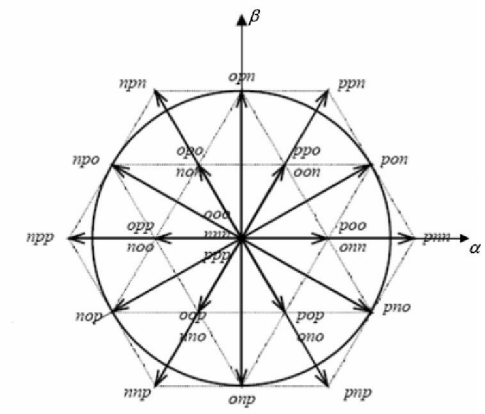

Fig. 5 Space Voltage Vectors in α - β plane

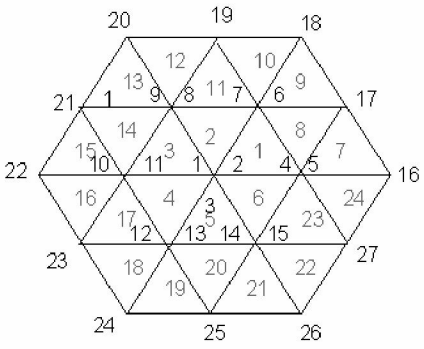

Fig. 6. Numbering of Switching States and Triangles

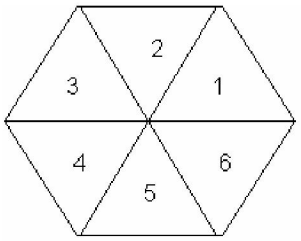

Fig. 7. Hexagon space divided into six big triangles

divide the hexagon (Fig. 6.) into six big triangles as shown in Fig. 7. The magnitude and angle θ of the reference vector V_{REF} is known. With angle information we can always determine in which triangle (triangles 1 to 6 of Fig. 7.), the tip of the reference vector is located. This bigger triangle is further divided into smaller triangles as indicated in Fig. 8. Triangle 1 (of Fig. 7.) is subdivided into four smaller triangles by the lines 1, 2 and 3. The smaller triangles are referred to as *inner small triangle* (I), *middle small triangle* (M), and (there are two) *outer small triangles* (O). The reference vector V_{REF} is decomposed into *x* and *y* components. Equations (10), (11) and (12) define the equations for the lines 1, 2 and 3 respectively.

$$y_1 = \frac{V_{pn}}{2\sqrt{3}} \tag{10}$$

$$y_2 = \frac{1}{2\sqrt{3}} V_{pn} - \sqrt{3}\left(x - \frac{V_{pn}}{6}\right) \tag{11}$$

$$y_3 = \sqrt{3}\left(x - \frac{V_{pn}}{3}\right) \tag{12}$$

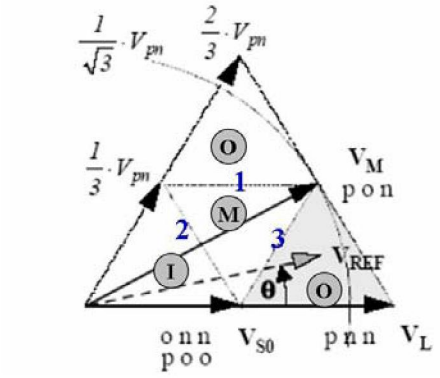

Fig. 8. Smaller Triangles to locate Reference Vector

The next task is to find out the smaller triangle (within the bigger triangle) in which the tip of the reference vector lies. This can be obtained from the linear equations (10, 11 and 12) defining the boundaries of the smaller triangles (Fig. 8.). By knowing the signs of y_1, y_2 and y_3, we can determine whether the tip of the reference vector lies in the *inner small triangle*, *middle small triangle* or *outer small triangles*. Then we can determine the NTVs to be switched on to approximate the reference vector.

D. Computation of Duty Cycles

After finding out where the tip of the reference vector lies, the task is to approximate the reference vector with the NTVs. Depending upon where the tip of the reference vector lies, the duty cycles of the NTVs to be switched on can be calculated. An illustrative case is presented here. The detailed derivation for computing the duty cycles is provided in reference [10].

If the reference vector lies in *outer small triangle* as shown in Fig.8., then,

$$V_{REF} = V_{so}.d_{so} + V_M.d_M + V_L.d_L \qquad (13)$$
$$d_{so} + d_M + d_L = 1$$

The duty cycles of NTVs are given by (14).

$$d_{so} = -\sqrt{3}m\cos(\theta) - m\sin(\theta) + 2$$
$$d_M = 2m\sin(\theta) \qquad (14)$$
$$d_L = -1 + \sqrt{3}m\cos(\theta) - m\sin(\theta)$$

where $0 < m < 1$ is the modulation index.

E. Switching Strategy

The switching strategy to be followed has to take into account the following objectives:

- minimising the switching frequency,
- uniform distribution of all conduction times between the 12 switches in order share the thermal stresses, and
- maintaing the neutral point voltage into a narrow band around $V_{dc}/2$.

These three objectives can be achieved with a three-level VSI controlled with SVM, following minimum switching sequences and with a suitable selection of the different space vectors that define the same point on the three level space. Depending upon the different sequences to obtain the voltage reference space vector, we can distinguish between the three different regions of operation: the *outer hexagon* (shaded region in Fig. 10.), the *inner star* (Fig. 11.), and the *inner hexagon* (Fig. 12.). When the voltage reference space vector changes from one region to another, the control mode will be modified appropriately. Let us consider three illustrative cases for the location of the tip of the reference voltage vector :

a) Outer Hexagon

Refering to Fig. 9., if the reference voltage space vector is situated in triangle 7(an *outer small triangle*), then there is only one minimum switching frequency sequence determined by the space vectors: 4,17,16,5 → 5,16,17,4 → 4,17,16,5…

b) Inner Star

Refering to Fig. 10, let the voltage space vector be situated in triangle 8 (*middle small triangle*). In this case also there is only

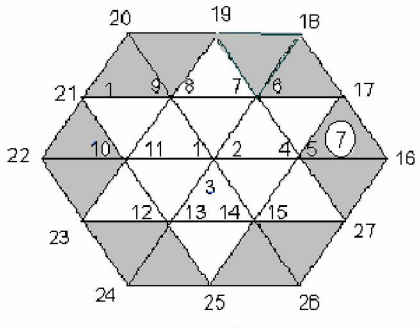

Fig. 9. Outer Hexagon

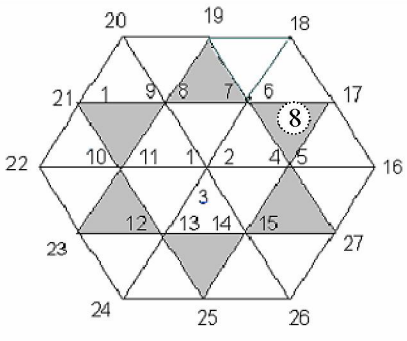

Fig.10. Inner star

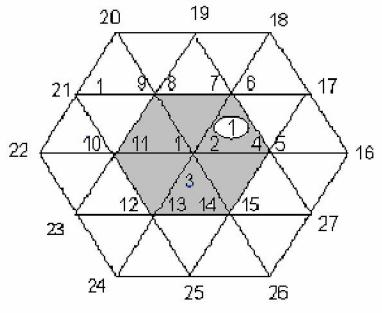

Fig. 11. Inner Hexagon

one sequence that minimizes the number of commutations of the switches: 5,7,17,4 → 4,17,7,5 → 5,7,17,4…..

c) Inner Hexagon

If the voltage space vector is situated in triangle 1(*inner small triangle*) as marked in Fig. 11., there are two different sequences that minimize the number of commutations: 3,4,6,1 → 1,6,4,3 → 3,4,6,1 … and 3,7,5,2 → 2,5,7,3 → 3,7,5,2. Both sequences are alternated in normal operation with the objective of sharing the conduction times.

III Simulation Results

The supply voltages (phase value) under normal conditions are 230 V, 50 Hz. The DVR does not respond during normal conditions. Extensive simulations were done and a few illustrative cases are presented here.

Case 1: The supply voltage dips symmetrically to 50% of rated value in each phase with no phase angle jump. The duration of sag is for 2 cycles. The reference compensation voltages Vcp, Vcq and Vcr generated by the PQR algorithm are

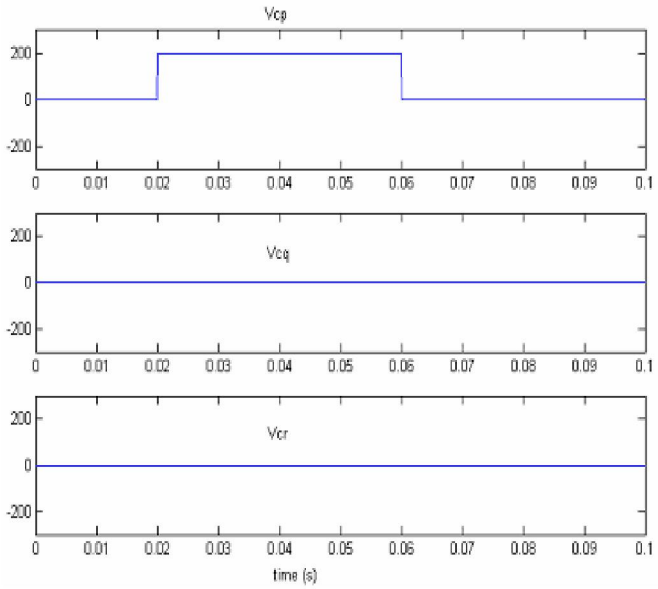

Fig. 12. Compensation Voltages Vcp, Vcq and Vcr (Case 1)

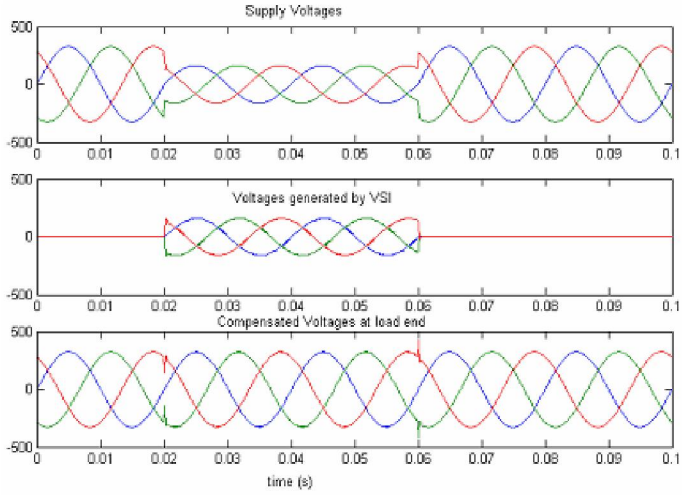

Fig. 13. Compensation of Sag by DVR (Case 1)

plotted in Fig. 12. Since there is symmetrical dip in 3-phases, the Vcp is a DC to regulate the positive sequence component (fundamental). The q-axis and r-axis compensation voltages Vcq and Vcr are zero as sag is not associated with unbalance (no negative sequence component), harmonics and DC offset (no zero sequence component). Fig. 13 shows the compensation of sag by DVR. Three sets of voltage waveforms are shown – supply voltages, voltages generated by VSI and compensated voltages at the load end. The voltages are instantaneously compensated and restored to nominal values. The glitch at the instants of start and end of sag may be due to the numerical simulation. The harmonic spectrum of the compensated phase voltage is analyzed and THD is 0.78%. Similar results are obtained with arbitrary instances of fault occurrence.

Case 2: A case of unsymmetrical fault, where phase 'a' is normal and phase 'b' voltage dips to 115V, i.e., 50% sag and phase angle jumps by – 15°. Phase 'c' voltage dips to 115V, i.e., 50% sag and phase angle jumps by 15°. The compensating voltages are shown in Fig. 14. The r-axis reference voltage Vcr which has 50 Hz frequency compensate for the zero sequence component of unbalanced source voltages. The ac components of reference voltages Vcp and Vcq which have 100 Hz frequency compensate for negative sequence component of the faulted source voltages. The DC components of Vcp and Vcq provide compensation for decreased fundamental component of the source voltages. The sag compensation by DVR is shown in Fig. 15. It is evident that the waveform compensation is instantaneous. There are some glitches in one phase, but the THD of the compensated phase voltages is 5.8%.

Case 3: A 5th harmonic, with a magnitude of 5% of the fundamental is injected into all three phases. A fault occurs on phase 'a' and the associated sag is 50%. The compensation voltages are plotted in Fig. 16. The compensation voltages Vcp and Vcq contain harmonic components before and after the occurrence of sag due to the harmonics in the source voltages.

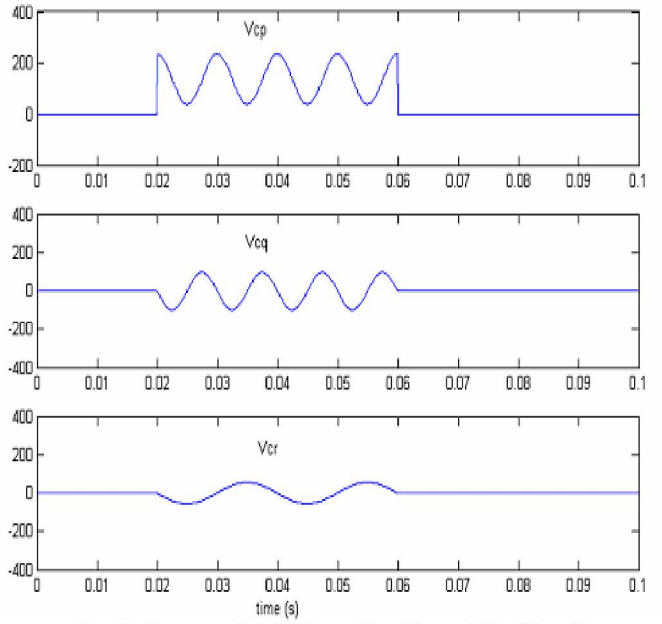

Fig. 14. Compensating Voltages Vcp, Vcq and Vcr (Case 2)

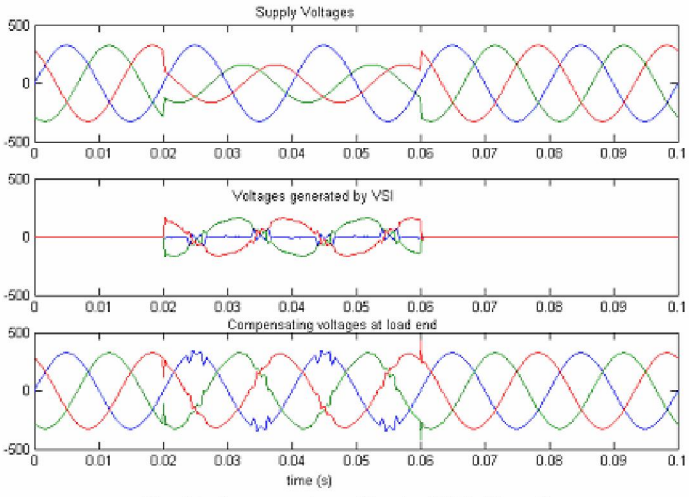

Fig. 15. Compensation of Sag by DVR (Case 2)

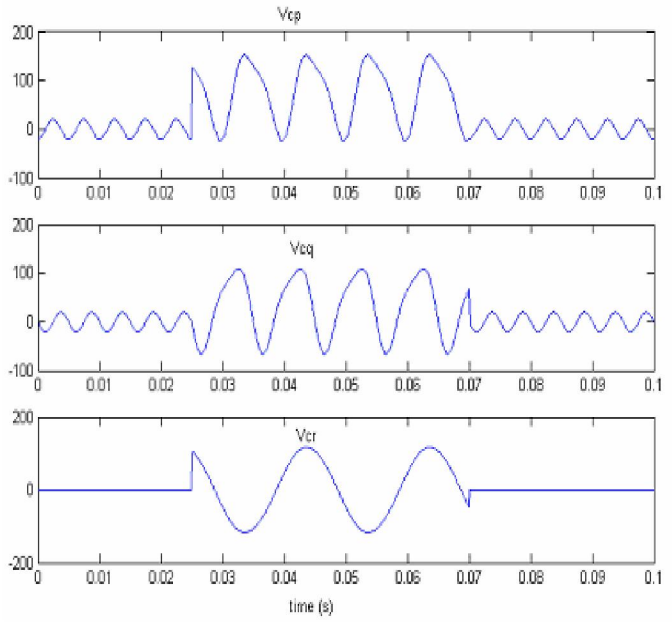

Fig. 16. Compensating Voltages Vcp, Vcq and Vcr (Case 3)

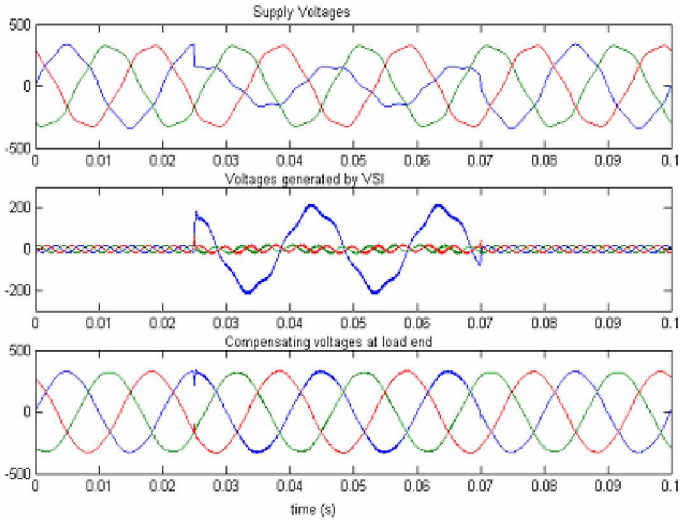

Fig. 17. Compensation of Sag by DVR (Case 3)

The voltage compensation by DVR is shown in Fig. 17. The 5th order harmonic is compensated and voltages are brought back to nominal values at the load end. The load voltages are sinusoidal. The THD of the compensated load voltages during sag is 2.1% and 1.4% in the periods before and after the sag (with the 5th harmonic component present in the supply voltage).

IV Conclusions

The PQR algorithm for calculating the reference compensation voltages is used together with an SVM technique for three-level diode clamped VSI to generate the DVR compensation voltages. The PQR algorithm in conjunction with space vector modulator works very well under a wide range of test conditions. The compensated voltages have THD varying from 0.78% for a best case to about 5.8% for the worst case. The proposed waveform synthesis technique works well and can be used for DVR applications in medium and high voltage systems as there is no time delay resulting in seamless voltage sag compensation with negligible THD.

Acknowledgment

The authors wish to acknowledge the support received from TEQIP (Technical Education Quality Improvement Program), National Institute of Technology Karnataka, Surathkal. TEQIP is a project of NPIU (National Project Implementation Unit), a Government of India unit for World Bank assisted project for Technical Education.

References

[1] Math H.J. Bollen, *Understanding Power Quality Problems*, IEEE Press Series on Power Engineering, New York, 2000.

[2] A. Sannino, M. G. Miller, and M. H. J. Bollen, "Overview of voltage sag mitigation", IEEE Proc. PES Winter Meeting, vol. 4, 2000, pp. 2872–2878.

[3] Arindam Ghosh and Gerard Ledwich, "Structures and Control of a Dynamic Voltage Restorer (DVR)," IEEE, PES Winter Meeting, 2001, pp 1027-1032.

[4] P. Daehler, R. Affolter, "Requirements Solutions for Dynamic Voltage Restorer, A Case Study", IEEE PES Winter Meeting, 2000, Volume 4, Jan. 2000, pp. 2881-2885.

[5] J. Nielsen, G. Blabjerg F., and N. Mohan, "Control Strategies for Dynamic Voltage Restorer Compensating Voltage Sags with Phase Jump", Proceedings of IEEE, APEC 2001, Vol. 2, pp. 1267-1273.

[6] V. K. Ramachandramurthy, C. Fitzer, A. Arulampalam, C. Zhan, M. Barnes and N. Jenkins, "Control of a Battery Supported Dynamic Voltage Restorer," IEE Proc- Gener. Trans. Distrib., Vol. 149, No. 5, Sept. 2002, pp. 533-541.

[7] Hyosung Kim, Jang-Hwan Kim and Seung-Ki Sul, "A Calculation for the Compensation Voltages in Dynamic Voltage Restorers by use of PQR Power Theory," APEC, Feb. 22-26, 2004, pp. 573-579.

[8] Jose Rodriguez, Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Inverters-A survey of Topologies, Controls and Applications", IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002, pp.724-738.

[9] N.Celonovic and D. Boroyevich, "A Fast Space-Vector Modulation Algorithm for Multilevel Three Phase Converters", IEEE Transactions on Industrial Applications, Vol. 37, No.2, March/April 2001, pp.637-641.

[10] G. Yankanchi, *Design and Simulation of Dynamic Voltage Restorer*, M.Tech Dissertation, Dept. of Electrical and Electronics Engineering, National Institute of Technology Karnataka, Surathkal, India, June 2005.