A Waveform Synthesis Technique for Voltage Sag Compensation using Dynamic Voltage Restorer (DVR)

Vijayan Immanuel[†] **and Gurunath Yankanchi**[‡]

Abstract--This paper presents the development of a novel waveform synthesis technique for effective voltage sag compensation for multilevel inverter based Dynamic Voltage Restorer(DVR). An effective control algorithm for calculation of reference compensating voltages based on PQR power theory together with Space Vector Modulation(SVM) technique is implemented using a three-level Diode Clamped Voltage Source Inverter(VSI) configuration. Extensive simulations are carried out under various test conditions and the results show that the proposed scheme for voltage sag compensation is seamless with negligible THD.

Index Terms-- Voltage Sag Compensation, Dynamic Voltage Restorer (DVR), Space Vector Modulation (SVM).

I Introduction

Voltage sags are most common power quality issues which occur in a power system [1]. Sag is a decrease to between 0.1 and 0.9 p.u. in RMS value at the power frequency for durations of 0.5 cycles to 1 minute. The voltage magnitude has to be maintained within the limits for proper operation of industrial customers which are sensitive to RMS voltage variations. The sensitive industrial customers like process automation, semiconductor manufacturing are very sensitive to RMS voltage variations. Sag of 70% depth for 6 cycles can trip Variable Speed Drive (VSD) and sag of 60% for 12 cycles can trip computer system (non linear load). This may lead to shutdown of plants or restart, reduced customer satisfaction and huge revenue losses. This explains the need for sag mitigation. The older techniques for sag mitigation are network based which includes, Ferro-resonant transformers, electronic tap changers and motor-generator sets. The response of such devices is very sluggish. The need is for devices with sub cycle response.

Dynamic Voltage Restorers (DVR) are an efficient and economic means to mitigate voltage sags and swells. The DVR is a series connected device, which primarily can protect sensitive electric consumers against voltage dips and surges in the medium and low voltage distribution grid [2]. The main components of DVR are controller, voltage source inverter, energy source for DC link capacitor, filters and booster transformers. The DVR is basically a voltage source inverter which compensates the missing voltage by rapidly injecting set of three phase voltages into the lines via booster transformer. The voltages can be controlled both in magnitude as well as phase. The generated voltages are rapidly injected into the line via booster transformer without any time delay. This significantly improves the dynamic response of DVR [3,4].

In this paper a method for waveform synthesis is developed such that the DVR response is in the subcycle region. The reference compensation voltages are calculated using an algorithm based on PQR power theory. The Space Vector Modulation (SVM) technique is developed to drive a three-level diode clamped inverter to generate the required compensation voltages. A DVR using three level diode clamped topology is well suited for medium and high voltage applications [5].

II Generation of Reference Compensation Voltages by PQR Algorithm [7]

In conventional methods for generation of reference compensation voltages like synchronous reference frame method, which employ Software Phase Locked Loop (SPLL, a PI compensator), delay is involved in tracking the new network angle if the sag is associated with phase angle jumps [6]. This greatly affects the dynamic response of DVR. In this paper, an algorithm based on PQR power theory[7] is used to obtain the reference voltages without time delay .

[†] Vijayan I. is with NITK Surathkal, India
[‡] G.Yankanchi is with BHEL, India

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III Space Vector Modulation (SVM) Technique for Three-Level Diode Clamped Topology

A. Switching Network of Three level VSI

The functional diagram of a three level VSI switching network is shown in Figure 1.

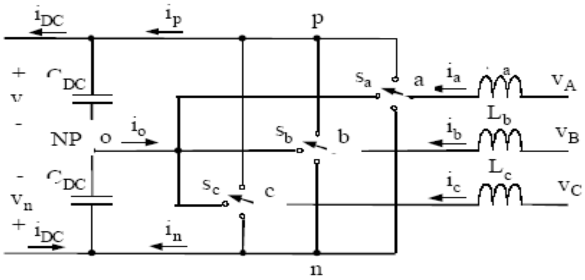
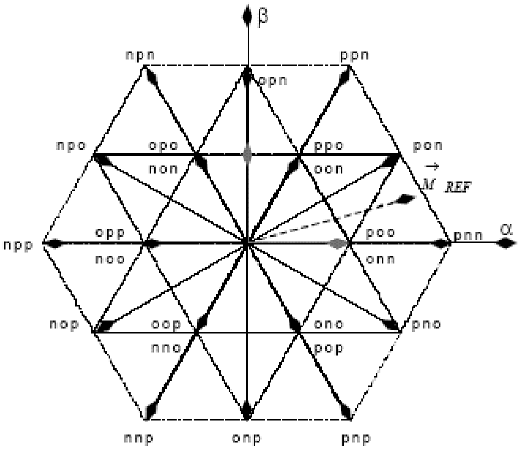


Figure 1 Switching network of a three-level VSI

Each switch will assume one of the positions like Sa may be connected to positive DC rail i.e. point ‘p’ or negative DC rail i.e. point ‘n’ or neutral point (N.P) i.e. point ‘o’. Each switch combination produces a unique voltage vector and can be represented as space voltage vector in one plane. The vector names represent the allowable switching states, e.g. ‘pon’ means switch Sa is connected to positive DC rail, Sb is connected to N.P and Sc is connected to negative DC rail. There are totally 27 (3^3) allowable switching state vectors which corresponds to 6-large vectors, 6-medium vectors, 12-small vectors and 3-zerovoltage vectors. The space voltage vectors are shown in Figure 2.

Figure 2 Space voltage vectors in $\alpha - \beta$ plane



The diagram contains totally 24 triangles and tip of the reference vector may lie in any one of the triangle as shown in Figure 3. The numbers in the middle of the triangle represent its number and the other numbers on the edges represent the switching state.

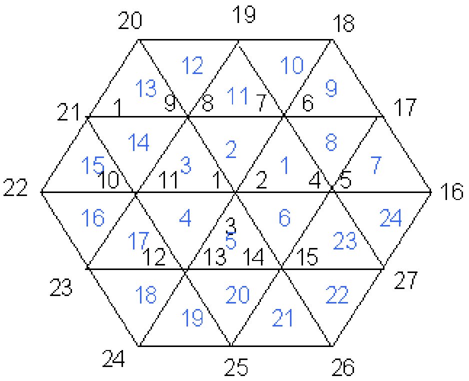


Figure 3 Three-level diagram showing numbering of switching states and triangles

The vertices of the inner hexagon correspond to two switching state vectors. The choice between them gives the key to achieve low harmonic content in the output voltage waveform and also controlling the DC-link midpoint voltage. This is possible because, for the same phase current direction if one space vector defining particular vertices causes an upper capacitor voltage increasing, the other space vector define the same vertices causes a voltage decreasing in the same capacitor.

B. Circuit Schematic of Three-level VSI

With reference to Figure 4, each leg consists of four switches. The lower leg switches are complements of the upper leg switches respectively.

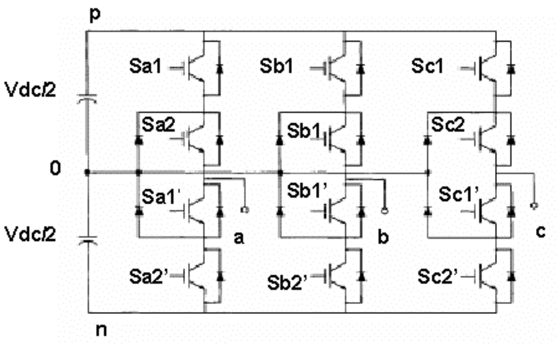
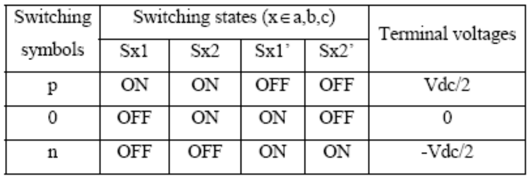


Figure 4 Circuit schematic of a Three-level VSI

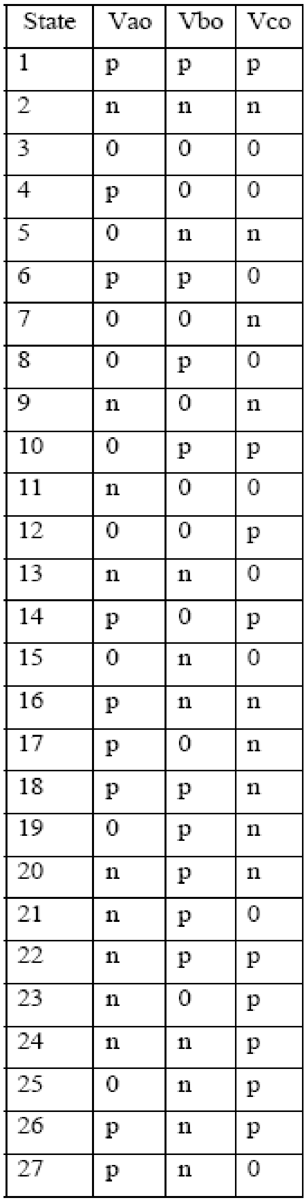
Table 1 shows switching states and terminal voltages, and Table 2 lists the output phase voltages for 27 switching states of 3-level VSI.

Table 1 Switching states and the terminal voltages of a 3-level VSI



Switching symbols	Switching states ($x \in a,b,c$)				Terminal voltages
	Sx1	Sx2	Sx1'	Sx2'	
p	ON	ON	OFF	OFF	Vdc/2
0	OFF	ON	ON	OFF	0
n	OFF	OFF	ON	ON	-Vdc/2

Table 2 Output phase voltages for 27 switching states of 3-level inverter



State	Vao	Vbo	Vco
1	p	p	p
2	n	n	n
3	0	0	0
4	p	0	0
5	0	n	n
6	p	p	0
7	0	0	n
8	0	p	0
9	n	0	n
10	0	p	p
11	n	0	0
12	0	0	p
13	n	n	0
14	p	0	p
15	0	n	0
16	p	n	n
17	p	0	n
18	p	p	n
19	0	p	n
20	n	p	n
21	n	p	0
22	n	p	p
23	n	0	p
24	n	n	p
25	0	n	p
26	p	n	p
27	p	n	0

It is the task of the modulator to decide which position the switches should assume (switching state), and the duration needed (duty cycle) in order to synthesize the reference voltage vector. In other words, it is the task of the modulator to approximate the reference vector, computed by the controller using the PWM of several switching vectors. Arguably, the best way to synthesize the voltage reference vector is by using the nearest three vectors (NTVs) as expressed by,

$$V_{REF} = d1V1 + d2V2 + d3V3 \qquad (1)$$

where, d1, d2 and d3 are the duty cycles of the vectors V1, V2 and V3 respectively, with the additional constraint on duty cycle being,

$$d1 + d2 + d3 = 1 \qquad (2)$$

C. Identification of Nearest Three Vectors (NTVs)

The first step the modulator needs to perform is to identify the NTVs, which is to determine the small triangle in which the tip of the reference vector V_{REF} is located. The first step is to divide the large space into smaller triangles as shown in Figure 5.

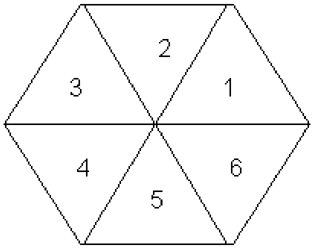


Figure 5 Hexagon space showing bigger triangles

The magnitude and angle θ of the reference vector V_{REF} is known. With angle information we can always determine in which bigger triangle the tip of the reference vector is located. After finding out the bigger triangle, the task is to find out the smaller triangle within the bigger triangle. This can be done by evaluating the sign of some linear equations defining the boundaries of the middle triangle as shown in Figure 6. The reference vector V_{REF} is decomposed into x and y components.

$$y = \frac{V_{pn}}{2\sqrt{3}} \qquad (3)$$

$$y = \frac{1}{2\sqrt{3}}V_{pn} - \sqrt{3}(x - \frac{V_{pn}}{6}) \qquad (4)$$

$$y=\sqrt{3}\left(x-\frac{V_{pn}}{3}\right) \qquad (5)$$

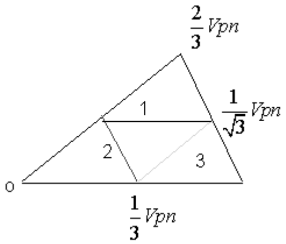


Figure 6 Division of large sector into smaller triangles

Equations (3), (4) and (5) define the equations for the lines 1, 2 and 3 respectively as shown in Figure 6. By knowing the signs of the equations, we can determine whether the tip of the reference vector lies in the inner small triangle or middle triangle or outer triangles. Then we can determine the NTVs to be switched on to approximate the reference vector

D. Computation of Duty Cycles

After finding out where the tip of the reference vector lies, the task is to approximate the reference vector with nearest three vectors. Depending upon where the tip of the reference vector lies, the duty cycles of the NTVs to be switched on can be calculated which is presented in following sections.

If the reference vector lies in OUTER SMALL TRIANGLE as shown in Figure 7, then,

$$\begin{aligned} V_{REF} &= V_{so}.d_{so}+V_M.d_M+V_L.d_L \\ d_{so}+d_M+d_L &= 1 \end{aligned} \qquad (6)$$

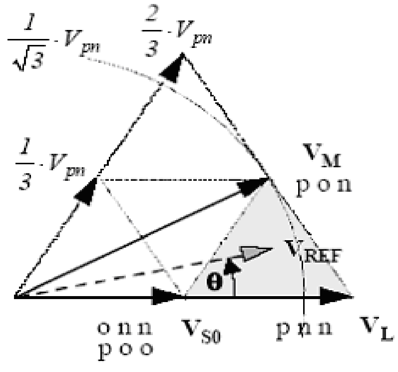


Figure 7 Synthesis of V_{REF} in the outer small triangle

The duty cycles of NTVs are given below.

$$\begin{aligned} d_{so} &= -\sqrt{3}m\cos(\theta)-m\sin(\theta)+2 \\ d_M &= 2m\sin(\theta) \\ d_L &= -1+\sqrt{3}m\cos(\theta)-m\sin(\theta) \end{aligned} \qquad (7)$$

where 0<m<1 is the modulation index.

If the reference vector lies in the INNER SMALL TRIANGLE as shown in Figure 8, then,

$$\begin{aligned} V_{REF} &= d_{so}.V_{so}+d_{s1}.V_{s1}+d_s.V_s \\ d_{so}+d_{s1}+d_s &= 1 \end{aligned} \qquad (8)$$

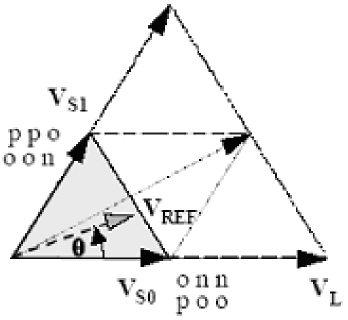


Figure 8 Synthesis of V_{REF} in the inner small triangle

The duty cycles of NTVs are given below,

$$\begin{aligned} d_{so} &= m(\sqrt{3}\cos(\theta)-\sin(\theta)) \\ d_{s1} &= 1-\sqrt{3}m\cos(\theta)-m\sin(\theta) \\ d_s &= 2m\sin(\theta) \end{aligned} \qquad (9)$$

If the reference vector lies in MIDDLE SMALL TRIANGLE as shown in Figure 9, then,

$$\begin{aligned} V_{REF} &= d_{so}.V_{so}+d_{s1}.V_{s1}+d_M.V_M \\ d_{so}+d_{s1}+d_{Ma} &= 1 \end{aligned} \qquad (10)$$

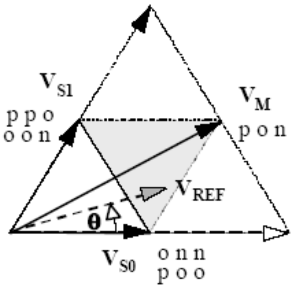


Figure 9 Synthesis of V_{REF} in the middle small triangle

The duty cycles of NTVs are given by ,

$$
\begin{aligned}
d_{so} &= 1-2m\cos(\theta) \\
d_{s1} &= 1-\sqrt{3}m\cos(\theta)+m\sin(\theta) \\
d_{M} &= -1+\sqrt{3}m\cos(\theta)+m\sin(\theta)
\end{aligned}
\tag{11}
$$

E. Switching strategy

The switching strtegy to be followed has to take into account the following objectives:

1) Minimising the switching frequency.
2) Uniform distribution of all conduction times between the 12 switches, in order share the thermal stresses
3) Maintaing the neutral point voltage into a narrow band around Vdc/2.

These three objectives can be achieved with a three level inverter controlled in SVM basis, following a minimum switching sequences and with a suitable selection of the different space vectors that define same point on the three level space. Depending upon the different sequences to obtain the volatge reference space vector, we can distinguish between the three different regions of operation: the Outer Hexagon (Figure 10), the Inner Star (Figure 11) and the Inner Hexagon (Figure 12). When the voltage reference space vector changes from one region to another, the control mode will be modified as explained below:

a) Outer hexagon

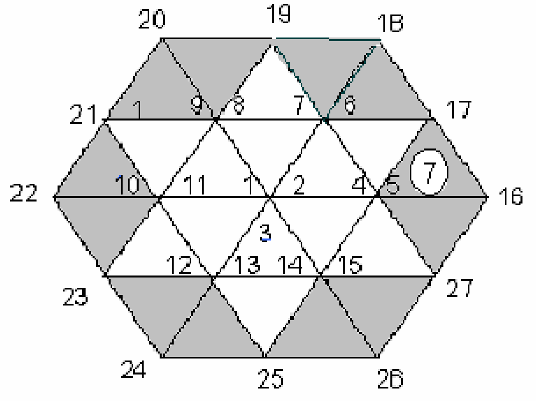


Figure 10 Outer Hexagon

Refering to Figure 10, if the reference voltage space vector is situated into the triangle 7, there is only one minimum switching frequencysequence determined by the space vectors: 4,17,16,5→5,16,17,4→4,17,16,5

b) Inner star

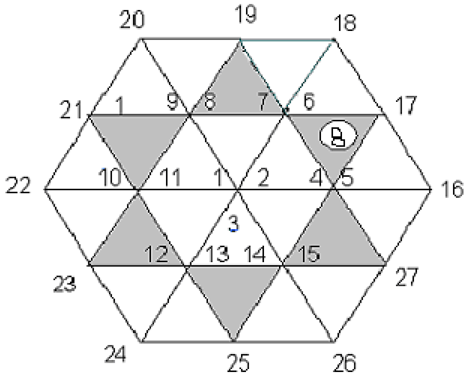


Figure 11 Inner star

Refering to Figure 11, if the voltage space vector is situated into the triangle 8, there is also only one sequence that minimises the number of commutations og the switches: 5,7,17,4→4,17,7,5→5,7,17,4…..

c) Inner hexagon

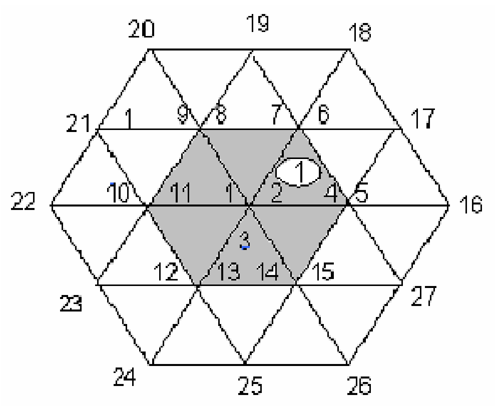


Figure 12 Inner Hexagon

Refering to Figure 12, if the voltage space vector is situated into the triangle 1, there are two different sequences that minimises the number of commutations: 3,4,6,1→1,6,4,3→3,4,6,1… and 3,7,5,2→2,5,7,3→3,7,5,2…both sequences are alternated in normal operation with objective of sharing the conduction times.

IV CONTROL FLOW

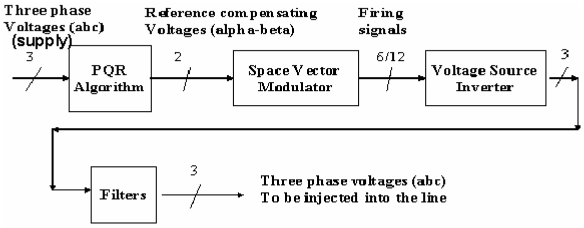


Figure 13 Block diagram of control flow

The block diagram of overall control flow is shown in Figure 13. Here the open loop feed forward control technique is adopted. After detecting the sag, the three phase voltages are processed using PQR algorithm. The reference compensating voltages are generated in PQR domain and transformed back to alpha-beta domain [8]. The alpha and beta axis reference voltages are given as inputs to drive the space vector modulator. The generated pulses are used to fire the switches of the VSI. The three phase output voltages generated by the VSI can be controlled both in magnitude and phase individually. Finally the 3-phase voltages are filtered out by a low pass filter before injecting into the line via booster transformer.

V CASE STUDIES

The supply voltages (phase value) under normal conditions are 230 V, 50 Hz. The DVR does not respond during normal conditions.

Case 1:

There is three phase balanced sag. The supply voltage dips symmetrically to 50% in each phase with no phase angle jump. The reference compensation voltages Vcp, Vcq and Vcr generated by the PQR algorithm are shown in Figure 14.

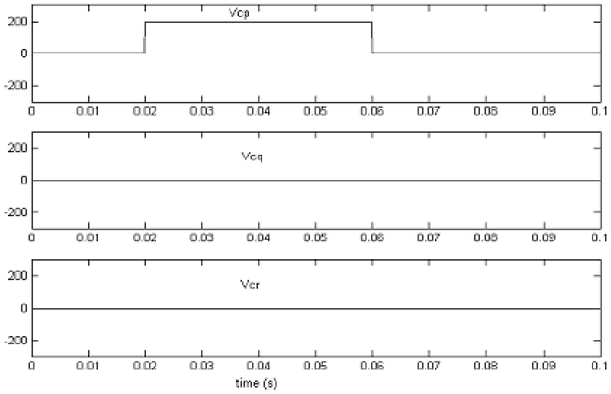


Figure 14 Compensation Voltages Vcp, Vcq and Vcr for Case 1

Since there is symmetrical dip in 3-phases, the Vcp is a DC to regulate the positive sequence component (fundamental). The q-axis and r-axis compensation voltages i.e. Vcq and Vcr are zero as sag is not associated with unbalance (negative sequence component) or harmonics and DC offset (zero sequence component). Figure 15 shows the compensation of sag by DVR.

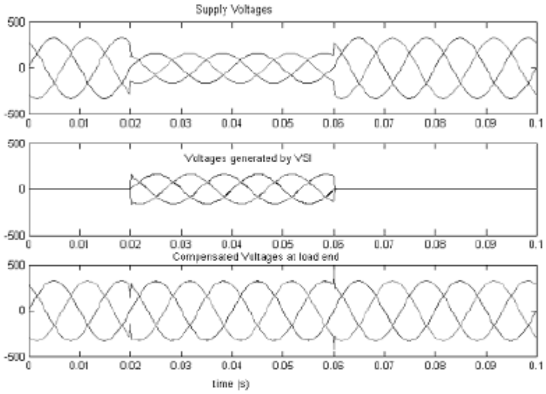


Figure 15 Compensation of Sag by DVR for Case 1

The sag stays for 2 cycles, during this period full compensation is provided by DVR without time delay. The voltages are instantaneously compensated and restored to nominal values. The harmonic spectrum of the compensated phase voltage was obtained and the THD is 0.78%.

Case 2:

An unsymmetrical fault is applied. Phase ‘a’ is normal and phase ‘b’ voltage dips to 115V i.e. 50% sag and phase angle jumps by -15°. The phase ‘c’ voltage dips to 115V i.e. 50% sag and phase angle jumps by 15°.

The compensating voltages are shown in Figure 16. The r-axis reference compensating voltage Vcr which has 50Hz frequency compensate for the zero sequence component of unbalanced source voltages. The ac components of Vcp and Vcq which have 100 Hz frequency compensate for negative sequence component of the faulted source voltages. The DC components of Vcp and Vcq provide compensation for decreased fundamental component of the source voltages. The sag compensation by DVR is shown in Figure 17. The THD of the compensated phase at the load end is 6.2 %.

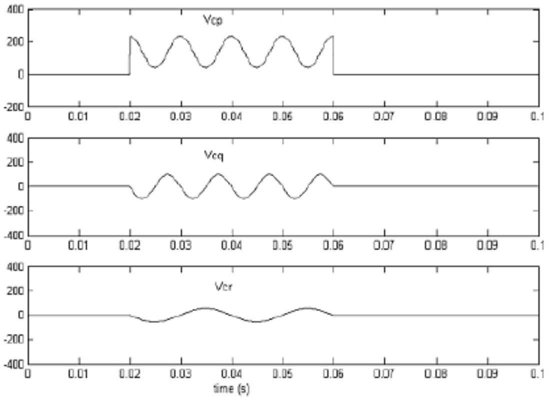


Figure 16 Compensating Voltages Vcp, Vcq and Vcr for Case 2

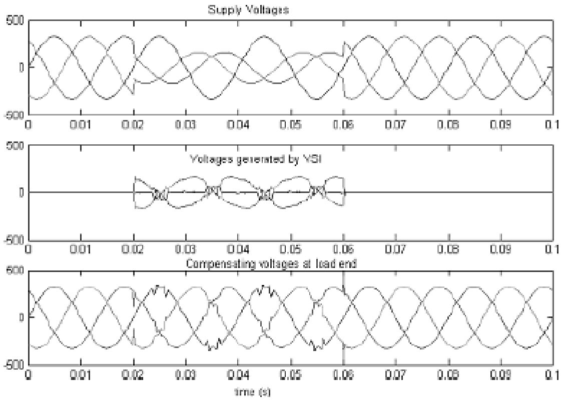


Figure 17 Compensation of Sag by DVR for Case 2

Case 3:

The supply is distorted with 5th harmonic. There is three phase balanced sag associated with 5th harmonic. The supply voltage dips symmetrically to 50% in each phase with no phase angle jump. Figure 18 shows the compensation of sag by DVR.

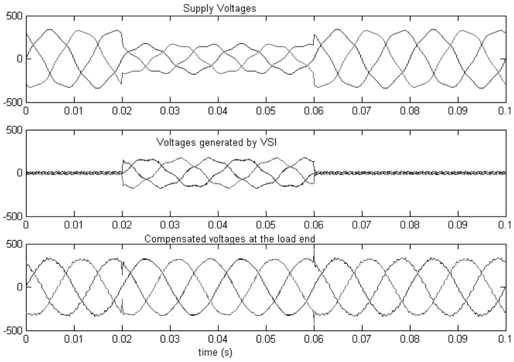


Figure 18 Compensation of Sag by DVR for Case 3

The sag stays for 2 cycles, during this period full compensation is provided by DVR without time delay. The voltages are instantaneously compensated and restored to normal values The harmonic spectrum of the compensated phase voltage is analyzed and THD obtained is 1.4%.

VI CONCLUSIONS

The PQR algorithm in conjunction with Space Vector Modulator works very well under a wide range of test conditions. The compensation of sag by DVR with three-level diode clamped VSI in case of balanced sag is excellent with output THD varying from about 0.78% for a best case to about 6.2% for the worst case. The proposed waveform synthesis technique works well and can be used for DVR applications as there is no time delay resulting in seamless voltage sag compensation.

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VII BIOGRAPHIES

Vijayan Immanuel graduated with B.Tech from KREC (now NITK) Surathkal in 1979. He obtained Ph.D. from I.I.Sc., Bangalore in 1993. He is currently Professor and Head, Dept. of Electrical & Electronics Engg., NITK Surathkal, India.

Gurunath Yankanchi obtained his B.Tech and M.Tech degrees from NITK Surathkal in 2003 and 2005 respectively. He is currently a GET with BHEL, India.