DESIGN AND MATHEMATICAL MODELING OF DUAL MATERIAL GATE JUNCTIONLESS FINFET

Thesis

Submitted in partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOPHY

by
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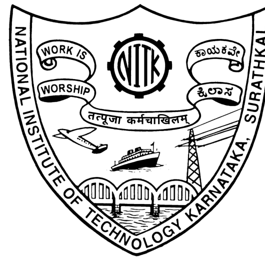

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DECLARATION

I hereby ***declare*** that the research Thesis entitled **DESIGN AND MATHEMATICAL MODELING OF DUAL MATERIAL GATE JUNCTIONLESS FINFET** which is being submitted to the ***National Institute of Technology Karnataka, Surathkal*** in partial fulfillment of the requirement for the award of the Degree of ***Doctor of Philosophy*** in **Department of Electronics and Communication Engineering** is a ***bonafide report of the research work carried out by me***. The material contained in this research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

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Abstract

Junctionless transistor (JLT) is a type of field effect transistor without any p-n junctions in its active region. Unlike conventional MOSFET, when JLT scales down in size, creating very small and shallow source and drain regions in a substrate containing dopants of opposing polarity is not needed. This simplifies the fabrication process to a great extent. Incorporating Dual Material Gate (DMG) architecture in JLT significantly enhances transistor performance in terms of reduced Short Channel Effects (SCE), better threshold voltage engineering and enhanced control over channel electrostatics. Hence a detailed investigation of the electrical behaviour and SCE in Dual Material Gate Junctionless Fin Field Effect Transistors (DMG JLFinFETs) with different gate material combinations and various gate metal length ratios is conducted in this research work. Rigorous analysis on the DC and short channel performance of DMG JLFinFET with gate length as low as 10 nm is done using the device simulator ATLAS provided by Silvaco, Inc. It is observed that by properly selecting gate materials and with suitable gate length ratios, the performance of DMG JLFinFET can be enhanced while keeping SCE at bay. In a DMG JLFinFET, it is the difference in the work function of both gate materials that decides Drain Induced Barrier Lowering (DIBL) and Sub-threshold Swing (SS) and not their individual work functions. Based on these observations, design guidelines are provided to choose the gate materials in a DMG JLFinFET as per the requirements. Of all combinations of DMG pairs examined, least DIBL of 12.88 mV/V is obtained when $\phi_{\mathrm{M1}} - \phi_{\mathrm{M2}}$ is 0.38 eV (Titanium-Aluminium and Nickel-Titanium gate pair). The degree of enhancement in the performance of DMG JLFinFET by choosing suitable spacers with proper spacer lengths (L_{SP}) is also examined. Best performance is observed in DMG JLFinFETs with HfO_2 spacer having a length of 50% of source/drain extension length.

As transistors are building blocks of Intergrated Circuits (ICs), developing robust and computationally efficient mathematical models is necessary to design complex ICs. DMG JLFinFETs showcase exemplary performance like negligible Drain Induced Barrier lowering (DIBL) and reasonably less Sub-threshold Swing (SS) alongside easier tuning of their threshold volt-

age. Hence it is imperative to model their characteristics. In this work, initially, Fourier series-based analytical model for threshold voltage (V_{th}) and SS are developed for Single Material Gate JLFinFET (SMG JLFinFET) on SOI substrate. These models take into account the location of the onset of current conduction in the channel. Therefore they are more accurate in predicting V_{th} and SS than the model available in the literature using the same approach. At channel length of 12 nm maximum deviation of threshold voltage calculated using the proposed model and numerical simulation is 1.46 V as against similar error of 3.19 V using the published model. SS model derived in this work gave a maximum error of 153.27 mV/dec whereas with the published model, the highest error was 382.95 mV/dec. It is seen that DMG JLFinFET outperforms SMG counterpart in terms of current characteristics as well as SCE. However, there is no literature available that discusses the mathematical modeling of various parameters of DMG JLFinFET. Hence, Fourier series-based channel potential and V_{th} models for DMG JLFinFET are developed and validated using TCAD simulations.

Keywords: Dual Material Gate; Drain Induced Barrier Lowering; subthreshold swing; junctionless FinFET; threshold voltage model; channel potential model.

Contents

Acknowledgements . . . i
Abstract . . . iii
List of Figures . . . ix
List of Tables . . . xvii
Abbreviations . . . xx
Notations . . . xxiii
Materials considered with their chemical formula . . . xxv

1 INTRODUCTION 1
1.1 Motivation for the present work . . . 5
1.2 Research Objectives . . . 5
1.3 Organization of the Thesis . . . 6

2 LITERATURE REVIEW 7
2.1 Introduction . . . 7
2.2 Junctionless Transistor . . . 7
2.2.1 Basic Structure of JLT . . . 8
2.2.2 Current Conduction Mechanism . . . 9
2.2.3 Regions of Operation . . . 10
2.2.3.1 Full Depletion . . . 11
2.2.3.2 Partial Depletion . . . 11
2.2.3.3 Flat Band Region . . . 11
2.2.3.4 Accumulation . . . 12
2.3 Unique Features of Junctionless Transistor . . . 13
2.4 Innovations to Enhance the Performance as well as Reduce the Short Channel Effects in a Junctionless Transistor . . . 15
2.4.1 Active Region with Non-uniform Doping . . . 16

2.4.1.1 JLT with Gaussian Doping . . . 16
2.4.1.2 JLT with Step Doping . . . 17
2.4.2 Alternate Material for Active Region of JLTs . . . 17
2.4.2.1 Germanium JLT . . . 18
2.4.2.2 Indium Gallium Arsenide JLT . . . 18
2.4.2.3 Gallium Nitride JLT . . . 18
2.4.3 Gate Electrode Engineering . . . 19
2.4.3.1 Dual Material Gate . . . 19
2.4.3.2 Triple Material Gate . . . 20
2.4.4 Multi-Gate Junctionless Transistors . . . 20
2.4.4.1 Double Gate Junctionless Transistor . . . 21
2.4.4.2 Junctionless Fin Field Effect Transistor . . . 21
2.4.4.3 Cylindrical Gate-All-Around Junctionless Transistor . 23
2.4.5 Gate Oxide and Spacer Engineering . . . 23
2.4.5.1 Gate Oxide Engineered Junctionless Transistors . . . 24
2.4.5.2 Spacer Engineered Junctionless Transistors . . . 24
2.5 Performance Comparison of Junctionless Transistor with Conventional Inversion mode Transistor . . . 25
2.6 Exclusive Survey on research works Incorporating DMG Architecture as well as Spacer Technology in Junctionless Transistors . . . 26
2.6.1 Literature Survey on DMG Architecture in Junctionless Transistor 27
2.6.2 Literature Survey on Junctionless Transistor with Spacers . . . 29
2.6.3 Literature Survey on DMG Junctionless Transistor with Spacers 33
2.7 Theoretical Modeling of Junctionless Transistors . . . 34
2.7.1 Threshold Voltage Model for Junctionless Transistors . . . 35
2.7.1.1 Threshold Voltage Models for DMG Junctionless Transistors . . . 40
2.8 Summary . . . 42

3 DUAL MATERIAL GATE JUNCTIONLESS FINFET- A COMPREHENSIVE STUDY 45

3.1 Introduction . . . 45
3.2 Structure of DMG JLFinFET and Simulation Framework . . . 46
3.3 Simulation Results . . . 48

3.3.1 Influence of Work Function of both Gate Materials on DC Characteristics of DMG JLFinFET . . . 49
3.3.2 Influence of Gate Material Length Ratio on DC Characteristics of DMG JLFinFET . . . 52
3.3.3 Short Channel Effects in DMG JLFinFETs . . . 55
3.3.3.1 Impact of $\phi_{M1} \sim \phi_{M2}$ and $\frac{L_{M1}}{L_g}$ on DIBL and Sub-threshold Swing of DMG JLFinFET: . . . 55
3.3.3.2 Impact of $\phi_{M1} \sim \phi_{M2}$ and $\frac{L_{M1}}{L_g}$ of DMG, on Relative Change in Threshold Voltage of DMG JLFinFET . . . 57
3.4 Summary . . . 62

4 Performance enhancement of Dual Material Gate Junctionless FinFETs using Dielectric Spacer 63
4.1 Introduction . . . 63
4.2 Structure of DMG JLFinFET with Spacer and Simulation Setup . . . 64
4.3 Results . . . 65
4.3.1 Analysing the Effect of Dielectric constant and Length of Spacer on Channel Electrostatics of TiAl DMG JLFinFET through Contour Plots . . . 65
4.3.2 Effect of Dielectric Constant and Length of Spacer on DC Characteristics of TiAl DMG JLFinFET. . . . 70
4.3.3 Effect of Dielectric Constant and Length of Spacer on Short Channel Effects in TiAl DMG JLFinFET. . . . 72
4.3.4 Effects of various Spacer Materials on DC and Analog Parameters of TiAl DMG JLFinFET having Optimised Spacer Length of 5 nm . . . 74
4.3.4.1 Impact of Spacer Material on the Drain Current and Transconductance . . . 75
4.3.4.2 Influence of Spacer Material on Analog Performance Metrics . . . 76
4.4 Summary . . . 79

5 An improved Fourier series based analytical model for threshold voltage and sub-threshold swing in SOI Junctionless

FinFET 81

5.1 Introduction . . . 81
5.2 Device Structure and Simulation Conditions . . . 82
5.3 Modified Model for Threshold Voltage and Sub-threshold Swing . . . 84
5.3.1 Background of Channel Potential Model Formulation . . . 84
5.3.2 Analysis of Channel Potential Variation along X, Y and Z Direction . . . 86
5.3.3 Location of Onset of Current Conduction in JLFinFET . . . 89
5.3.4 Model Formulation with Approximations based on the Location of Onset of Current Conduction . . . 91
5.3.4.1 Threshold Voltage . . . 91
5.3.4.2 Sub-threshold Swing . . . 93
5.4 Results and Discussion . . . 94
5.4.1 Validation of modified V_{th} model and comparison of its Accuracy with the Model in Ref. Hu *et al.* (2016) . . . 94
5.4.2 Validation of DIBL computed from V_{th} Model using TCAD Simulations . . . 97
5.4.3 Validation of modified SS model and comparison of its Accuracy with the Model in Ref. Hu *et al.* (2016) . . . 99
5.5 Summary . . . 102

6 Fourier series-based analytical model for channel potential and threshold voltage in Dual Material Gate SOI Junctionless FinFET 103

6.1 Introduction . . . 103
6.2 Device Structure and Simulation Conditions . . . 104
6.3 Model for channel potential of DMG JLFinFET . . . 106
6.4 Validation of Channel Potential Model with TCAD simulation . . . 113
6.4.1 Channel Potential Variation along X Direction with Device Parameter Change . . . 113
6.4.2 Channel Potential Variation in All Directions . . . 120
6.5 Model for Threshold Voltage of DMG JLFinFET . . . 122
6.5.1 Location of Onset of Current Conduction in DMG JLFinFET . . . 123

6.5.2 Analytical Model Formulation for Threshold Voltage of DMG JLFinFET 125
6.6 Validation of threshold voltage model with TCAD simulation 128
6.7 Brief of Errors that cause V_{th} Model - Simulation Mismatch 133
6.8 Summary 134

7 CONCLUSIONS AND FUTURE WORK 135
7.1 Summary and Conclusions 135
7.2 Scope of Future Work 137

Bibliography 138

Publications based on the thesis 149

List of Figures

1.1 Schematic representation of (a) DGJLT (b) JLFinFET (c) GAAJLT and (d) CGAAJLT (Kim *et al.* (2014)). 3

2.1 Cross-sectional view of SOIJLT. 8
2.2 Energy band diagram along (a) vertical cross-section and (b) horizontal cross-section, of an n-type JLT at equilibrium. 9
2.3 Regions of operation marked on V_{GS} axis. 10
2.4 3-D electron concentration profile in an n-type JLT for (a) $V_{GS}<V_{th}$ (b) $V_{GS}=V_{th}$ (c) $V_{GS}>V_{th}$ (d) $V_{GS}=V_{FB}>>V_{th}$ (Colinge *et al.* (2011)). 12
2.5 3-D electron concentration profile in an n-type junctionless transistor for (a) V_{DS} = 50 mV (b) V_{DS} = 200 mV (c) V_{DS} = 400 mV and (d) V_{DS} = 600 mV for $V_{GS}>V_{th}$ (Colinge *et al.* (2011)). 13
2.6 Effective channel length of JLT (Colinge (2018)) 14
2.7 Structure of Gaussian-doped JLT. 17
2.8 Structure of Dual Material Gate JLT. 19
2.9 Structure of Triple Material Gate JLT. 20
2.10 Cross-sectional view of Double Gate JLT (Duarte *et al.* (2011).) 21
2.11 3-D schematic view as well as a 2-D cross-sectional view of (a) SOI JLFinFET (Hu *et al.* (2016)) and (b) Bulk JLFinFET (Scarlet and Srinivasan (2018)). 22
2.12 3-D Schematic of Cylindrical Gate-All-Around JLT (Lime *et al.* (2014)). 23
2.13 (a) 3-D Schematic of SOIJLT with spacer (Gundapaneni *et al.* (2011)) and (b) Fringing field lines passing through sidewall spacer in a JLT (Kumari *et al.* (2015)). 24
2.14 3-D structure of Junctionless FinFET with dual κ spacer (Kaur *et al.* (2022)). 30

3.1 (a) 3-D structure of DMG JLFinFET and (b) 2-D cross-sectional view of DMG JLFinFET . . . 46
3.2 Comparison of transfer characteristics of JLFinFET from Lee *et al.* (2016) and calibrated simulation setup at V_{DS} = 0.7 V. . . . 47
3.3 Calibration of simulation setup with data from Barraud *et al.* (2012) . . 48
3.4 Transfer characteristics of DMG JLFinFETs with (i) Ti as M1 and other metals as M2 (red) and (ii) Ti as M2 and other metals as M1 (black), at V_{DS} = 0.7 V . . . 49
3.5 Threshold voltage of DMG JLFinFETs with (i) Ti as M1 and other metals as M2 (red) and (ii) Ti as M2 and other metals as M1 (black), at V_{DS} = 0.7 V . . . 50
3.6 Energy band diagram along a cutline (x direction) located at the middle of channel in DMG JLFinFET with different gate metal pairs, at V_{GS} = V_{tunn} and V_{DS} = 0.7 V . . . 51
3.7 Transfer characteristics of TiAl DMG JLFinFET (red) and AlTi DMG JLFinFET (black) for varying $\frac{L_{M1}}{L_g}$ (expressed in %), at V_{DS} = 0.7 V . . 53
3.8 Threshold Voltage of TiAl DMG JLFinFET and AlTi DMG JLFinFET for varying $\frac{L_{M1}}{L_g}$ (expressed in %), at V_{DS} = 0.7 V . . . 53
3.9 Energy band diagram along a cutline (x direction) at the middle of channel in AlTi DMG JLFinFET and TiAl DMG JLFinFET for varying $\frac{L_{M1}}{L_g}$, at V_{GS} = V_{tunn} and V_{DS} = 0.7 V. . . . 54
3.10 Variation in (a) DIBL and (b) SS with difference in the work function of M1 and M2. . . . 55
3.11 Variation in (a) DIBL and (b) SS with varying $\frac{L_{M1}}{L_g}$ keeping total gate length fixed to 10 nm . . . 56
3.12 Threshold voltage and relative change in threshold voltage of DMG JLFinFETs belonging to (a) $\phi_{M1} > \phi_{M2}$ category and (b) $\phi_{M1} < \phi_{M2}$ with gate metal pair arranged (from left to right) in the ascending order of $\phi_{M1} \sim \phi_{M2}$. . . . 59
3.13 Threshold voltage and relative change in threshold voltage of PtAu DMG JLFinFET, Au SMG JLFinFET and Pt SMG JLFinFET. . . . 60
3.14 Threshold voltage and relative change in threshold voltage for varying $\frac{L_{M1}}{L_g}$ in (a) TiAl DMG JLFinFET and (b) AlTi DMG JLFinFET keeping total gate length fixed to 10 nm. . . . 61

4.1 (a) 3-D structure and (b) 2-D cross-sectional view along A-A' cutline, of Dual Material Gate Junctionless FinFET with spacer 64
4.2 Contour plot of electric field along a cut-plane parallel to xz plane at y = $\frac{T_{\text{fin}}}{2}$ in TiAl DMG JLFinFET with (a) varying spacer materials having L_{SP} = 5 nm (b) TiO_2 spacer with varying L_{SP}, for V_{GS} = V_{DS} = 0.7 V. (x, z) = (x, 0 μm) is gate oxide-channel interface and (x, z) = (x, 0.005 μm) is buried oxide-channel interface. 66
4.3 Contour plot of electron concentration along a cut-plane parallel to xz plane at y = $\frac{T_{\text{fin}}}{2}$, in TiAl DMG JLFinFET with (a) no spacer in OFF/ON state, (b) SiO_2 spacer in OFF/ON state and (c) TiO_2 spacer in OFF/ON state. L_{SP} for all these transistors is 5 nm. (x, z)=(x, 0 μm) is gate oxide-channel interface and (x, z) = (x, 0.005 μm) is buried oxide-channel interface. 68
4.4 Contour plot of electron concentration along a cut-plane parallel to xz plane at y = $\frac{T_{\text{fin}}}{2}$ in TiAl DMG JLFinFET (a) with no spacer in OFF/ON state, (b) 2.5 nm TiO_2 spacer in OFF/ON state, (c) 5 nm TiO_2 spacer in OFF/ON state and (d) 7.5 nm TiO_2 spacer in OFF/ON state. (x, z)=(x, 0 μm) is gate oxide-channel interface and (x, z) = (x, 0.005 μm) is buried oxide-channel interface. 69
4.5 Variation in (a) ON current (black), OFF current (red) and (b) $\frac{I_{ON}}{I_{OFF}}$ with dielectric constant of spacer for L_{SP} = 2.5 nm, 5 nm and 7.5 nm. . 70
4.6 Transfer characteristics for TiAl DMG JLFinFET (having no spacer) including as well as excluding band-to-band tunneling model in the simulator at V_{DS} = 0.7 V 71
4.7 Variation in I_{tunn} with dielectric constant of spacer for L_{SP} = 2.5 nm, 5 nm and 7.5 nm. 71
4.8 (a) DIBL and (b) SS variation with dielectric constant of spacer (L_{SP} = 2.5 nm, 5 nm and 7.5 nm.) for L_g = 10 nm, 20 nm and 30 nm 73
4.9 (a) Transfer characteristics and (b) transconductance with respect to V_{GS}, of TiAl DMG JLFinFET with different spacer materials at V_{DS} = 0.7 V. 75
4.10 Variation of (a) output characteristics (b) output conductance with respect to V_{DS} of TiAl DMG JLFinFET with different spacer materials at V_{GS} = 0.7 V. 76

4.11 Variation of (a) transconductance generation factor (TGF) with V_{GS} and (b) intrinsic gain with overdrive voltage, of TiAl DMG JLFinFET with various spacer materials at V_{DS} = 0.7 V. 76

4.12 Variation of output resistance with V_{GS} of TiAl DMG JLFinFET with different spacer materials at V_{DS} = 0.7 V. 77

5.1 3-D structure of JLFinFET on SOI substrate 83

5.2 (a) 2-D cross sectional view of JLFinFET in xz plane at y = 0 and (b) channel potential variation along A-A' between points 'S' and 'T' at different V_{GS}. V_{DS} taken is 0.5 V. 87

5.3 (a) 2-D cross sectional view of JLFinFET in yz plane at x = $\frac{L_g}{2}$ and (b) channel potential variation along B-B' between points 'M' and 'N' at different V_{GS}. V_{DS} taken is 0.5 V. 87

5.4 (a) 2-D cross sectional view of JLFinFET in xz plane at y = 0 and (b) channel potential variation along C-C' between points 'U' and 'V' at different V_{GS}. V_{DS} taken is 0.5 V. 88

5.5 (a) Electron concentration at various z locations (at x = $\frac{L_g}{2}$, y = 0) in the channel with varying gate voltage (at V_{DS} = 0.5 V) and (b) contour plot of channel potential along a cross section in xy plane of JLFinFET, at y = 0 nm (V_{DS} = 0.5 V and V_{GS} = 0.6 V). 89

5.6 (a) Electron concentration at various y locations (at x = $\frac{L_g}{2}$, z = $\frac{H_{fin}}{2}$) in the channel with varying gate voltage (at V_{DS} = 0.5 V) and (b) contour plot of channel potential along a cross section of JLFinFET, at z = $\frac{H_{fin}}{2}$ nm (V_{DS} = 0.5 V and V_{GS} = 0.6 V). 90

5.7 Threshold voltage variation with gate length obtained from analytical model in equation 5.25 and TCAD simulation for three different T_{fin} - H_{fin} combinations where (a) H_{fin} is fixed to 12 nm and T_{fin}=(12 nm, 10 nm and 8 nm) and (b) T_{fin} is fixed to 8 nm and H_{fin}=(15 nm, 12 nm and 9 nm), at V_{DS} = 0.5 V. 94

5.8 Comparison of the accuracy of the model in equation (23) and the model published in Hu *et al.* (2016) for predicting threshold voltage for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that H_{fin} in all cases is fixed to 12 nm while T_{fin} is chosen to vary (12 nm, 10 nm and 8 nm). 96

5.9 Comparison of the accuracy of the model in equation (23) and the model published in Hu *et al.* (2016) for predicting threshold voltage for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that T_{fin} in all cases is fixed to 8 nm while H_{fin} is chosen to vary (15 nm, 12 nm and 9 nm). 97

5.10 DIBL with varying gate length for three different T_{fin} - H_{fin} combinations where (a) H_{fin} is fixed to 12 nm and T_{fin}=(12 nm, 10 nm and 8 nm) and (b) T_{fin} is fixed to 8 nm and H_{fin}=(15 nm, 12 nm and 9 nm). . 98

5.11 SS with varying gate length for three different T_{fin}-H_{fin} combinations where (a) H_{fin} is fixed to 12 nm and T_{fin}=(12 nm, 10 nm and 8 nm) and (b) T_{fin} is fixed to 8 nm and H_{fin}=(15 nm, 12 nm and 9 nm). . . . 99

5.12 Comparison of the accuracy of the model in equation 5.30 and the model published in Hu *et al.* (2016) for predicting sub-threshold swing for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that H_{fin} in all cases is fixed to 12 nm while T_{fin} is chosen to vary (12 nm, 10 nm and 8 nm). 100

5.13 Comparison of the accuracy of the model in equation 5.30 and the model published in Hu *et al.* (2016) for predicting sub-threshold swing (SS) for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that T_{fin} in all cases is fixed to 8 nm while H_{fin} is chosen to vary (15 nm, 12 nm and 9 nm). 101

6.1 3-D structure of DMG JLFinFET on SOI substrate. 105

6.2 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{fin}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different channel lengths, L_g = 20 nm, 30 nm and 50 nm. 114

6.3 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{fin}}{2}$) in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different channel length ratios, L_c : L_s = 1:2, 1:1 and 2:1. 114

6.4 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{fin}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different fin heights, H_{fin} = 8 nm, 10 nm and 12 nm. 115

6.5 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different fin widths, T_{fin} = 5 nm, 8 nm and 10 nm. 115

6.6 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{DS} = 0.5 V, for three different gate voltages ,V_{GS} = 0.1 V, 0.3 V and 0.5 V. 116

6.7 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V, for three different drain voltages, V_{DS} = 0.3 V, 0.5 V and 0.7 V. 117

6.8 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different control gate work functions, ϕ_c = 4.85 eV, 5 eV and 5.25 eV. 117

6.9 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different screen gate work functions, ϕ_s = 4.4 eV, 4.6 eV and 4.8 eV. 118

6.10 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$) in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different channel doping concentrations, N_d = 10^{18} cm^{-3}, $5X10^{18}$ cm^{-3} and 10^{19} cm^{-3}. 119

6.11 Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different gate oxide thickness, t_{ox} = 1.2 nm, 1.5 nm and 1.7 nm. . 119

6.12 (a) DMG JLFinFET structure with xy cutplane located at z = $\frac{H_{\text{fin}}}{2}$ (b) 2-D cross-sectional view of DMG JLFinFET with channel bounded by the points P, Q, R, S, T and U and (c) potential variation between two side gates (in y direction) at z = $\frac{H_{\text{fin}}}{2}$ for V_{GS} = 0.3 V and V_{DS} = 0.5 V, at two different x locations (x = 6 nm belonging to region 'C' and 24 nm belonging to region 'S'.) 121

6.13 (a) DMG JLFinFET structure with xz cutplane located at y = 0 (b) 2-D cross sectional view of DMG JLFinFET with channel bounded by the points A, B, C, D, E and F and (c) potential variation along z direction at y = 0 for V_{GS} = 0.3 V and V_{DS} = 0.5 V, at two different x locations (x = 6 nm belonging to region 'C' and 24 nm belonging to region 'S'). 122
6.14 Contour plot of potential from source to drain along (a) xy cutplane located at z = $\frac{H_{\text{fin}}}{2}$ and (b) xz cutplane located at y = 0, in a DMG JLFinFET with $V_{GS} = V_{th}$ and V_{DS} = 0.5 V. 124
6.15 Potential variation in a DMG JLFnFET along A-A' cutline (A-A' cutline is along z direction at x = x_{min}, y = 0) for different V_{GS}, V_{DS} is fixed to 0.5 V. 125
6.16 Threshold voltage variation with gate length for DMG JLFinFETs with three different fin thickness (T_{fin} = 5 nm, 8 nm and 10 nm). 129
6.17 Threshold voltage variation with gate length for DMG JLFinFETs with three different fin height (H_{fin} = 8 nm, 10 nm and 12 nm). 130
6.18 Threshold voltage variation with gate length for DMG JLFinFETs with three different $L_c : L_s$ ratio ($L_c : L_s$ = 2:1, 1:1 and 1:2). 131
6.19 Threshold voltage variation with gate length for DMG JLFinFETs with three different control gate work function (ϕ_c = 4.85 eV, 5 eV and 5.25 eV). 132
6.20 Threshold voltage variation with gate length for DMG JLFinFETs with three different screen gate work function (ϕ_s = 4.4 eV, 4.6 eV and 4.8 eV). 132

List of Tables

2.1 Key literatures which compare performance of junctionless as well as conventional inversion mode transistors. 25

2.1 Key literatures which compare performance of junctionless as well as conventional inversion mode transistors. (Continued). 26

2.2 Summary of key literature on DMG in junctionless FETs. 28

2.2 Summary of key literature on DMG in junctionless FETs (Continued). . 29

2.3 Summary of key literature on junctionless FETs with spacers. 31

2.3 Summary of key literature on junctionless FETs with spacers. (Continued). 32

2.3 Summary of key literature on junctionless FETs with spacers. (Continued). 33

2.4 Summary of literature on DMG junctionless FETs with spacer technology. 34

2.5 Summary of literature with threshold voltage model in junctionless transistors. 38

2.5 Summary of literature with threshold voltage model in junctionless transistors (Continued). 39

2.5 Summary of literature with threshold voltage model in junctionless transistors (Continued). 40

2.6 Summary of literature on threshold voltage modeling in Dual Material Gate junctionless transistors. 41

2.6 Summary of literature with threshold voltage model in junctionless transistors (Continued). 42

3.1 Parameter specifications of Dual Material Gate Junctionless FinFET . 47

3.2 Choice list of Gate Metals used along with their Work Functions 47

3.3 I_{tunn} for DMG JLFinFETs having gate material pairs with $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$ 51

3.4 List of observations on I_{tunn} of under situations, $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$ in DMG JLFinFET 52

3.5 I_{tunn} for DMG JLFinFETs having gate material pairs such that $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$ 54
3.6 List of combinations of gate metal pairs considered for DMG JLFinFET categorised based on ϕ_{M1} greater/lower than ϕ_{M2}, along with their corresponding work function difference. 58
3.7 Comparison of proposed transistor with published literatures on DMG structure 62

4.1 Parameter specifications of Dual Material Gate Junctionless FinFET with spacers 65
4.2 Choice list of materials used as spacers along with their dielectric constants 65
4.3 Comparison of performance metrics of DMG JLFinFET with conventional and junctionless FETs published in literature. 78

5.1 Device Parameters 83
5.2 Coordinate information 84

6.1 Device Parameters 105
6.2 Co-ordinate information 106

Abbreviations

JL	Junctionless
IM	Inversion Mode
FET	Field Effect Transistor
DGFET	Double Gate Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complimentary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
JLT	Junctionless Transistor
JNT	Junctionless Nanowire Transistor
SOIJLT	Junctionless Transistor with SOI substrate
SRH	Schockley Read Hall
SMG	Single Material Gate
DMG	Dual Material Gate
DMG FET	Dual Material Gate Field Effect Transistor
DMG JNT	Dual Material Gate Junctionless Nanowire Transistor
SOI	Silicon On Insulator
2-D	2 Dimensional
3-D	3 Dimensional
SCE	Short Channel Effects
DIBL	Drain Induced Barrier Lowering
SS	Sub-threshold Swing
GDP JLT	Gaussian-Doped Junctionless Transistor
SDP JLT	Step-Doped Junctionless Transistor
Si JLT	Silicon Junctionless Transistor
Ge JLT	Germanium Junctionless Transistor
InGaAs	Indium Gallium Arsenide
InGaAs JLT	Indium Gallium Arsenide Junctionless Transistor
GaN JLT	Gallium Nitride Junctionless Transistor
DMG JLT	Dual Material Gate Junctionless Transistor
SMG JLT	Single Material Gate Junctionless Transistor
DGJLT	Double Gate Junctionless Transistor
SMG DGJLT	Single Material Gate Double Gate Junctionless Transistor

TMG	Triple Material Gate
TMG JLT	Triple Material Gate Junctionless Transistor
FinFET	Fin Field Effect Transistor
JLFinFET	Junctionless Fin Field Effect Transistor
SOI IMFinFET	IMFinFET with SOI substrate
SOI JLFinFET	JLFinFET with SOI substrate
Bulk JLFinFET	JLFinFET with Bulk substrate
Bulk IMFinFET	IMFinFET with Bulk substrate
GAAJLT	Gate All Around Junctionless Transistor
GAAIMT	Gate All Around Inversion Mode Transistor
CGAAJLT	Cylindrical Gate All Around Junctionless Transistor
RF	Radio Frequency
IC	Integrated Circuit
IM MOSFET	Inversion Mode MOSFET
DMG SOIJLT	Dual Material Gate JLT with SOI substrate
DMG JLFinFET	Dual Material Gate Junctionless FinFET
TiAl DMG JLFinFET	Titanium Aluminium Dual Material Gate Junctionless FinFET
AlTi DMG JLFinFET	Aluminium Titanium Dual Material Gate Junctionless FinFET
DMG DGJLT	Dual Material Gate Double Gate JLT
DMG DGMOSFET	Dual Material Gate Double Gate MOSFET
FoM	Figure of Merit
DMG CGAAJLT	Dual Material Gate Cylindrical Gate-All-Around junctionless transistor
SMG JNT	Single Material Gate junctionless Nanowire Transistor
TGF	Transconductance Generation Factor
TCAD	Technology Computer Aided Design
GCA	Gradual Channel Approximation
IRDS	International Roadmap for Devices and Systems
ALD	Atomic Layer Deposition
TAE	Tilt Angle Evaporation

Notations

T	Temperature
V_{GS}	Gate voltage
V_{DS}	Drain voltage
V_S	Source voltage
V_{BS}	Substrate voltage
V_{th}	Threshold voltage
V_{FB}	Flat band voltage
V_{EA}	Early voltage
V_{tunn}	Gate voltage at which tunneling occurs
V_t	Thermal voltage
V	Quasi-Fermi potential
q	Electronic charge
V_R	Reference voltage
Ψ_{sch}	Gate schottky barrier voltage
ϕ_M	Work function of gate
ϕ_S	Work function of active region
I_d	Drain current
I_{dsub}	sub-threshold current
Ψ	Electric potential
ε_{si}	Permittivity of silicon
ε_{ox}	Permittivity of gate oxide material
N_d	Doping concentration of channel
N_{peak}	Peak doping concentration of channel
N_{sub}	Substrate doping
L_g	Physical gate length
σ	Standard deviation
I_{OFF}	OFF current
I_{ON}	ON current
I_{tunn}	Tunneling current
$\frac{I_{ON}}{I_{OFF}}$	ON-OFF current ratio
L_{M1}	Length of gate metal near source in DMG
L_{M2}	Length of gate metal near drain in DMG

g_m	Transonductance of transistor
f_T	Unity gain cut-off frequency
f_{MAX}	Maximum oscillation frequency
A_V	Intrinsic gain
L_{sp}	Length of spacer
L_{sd}	source/drain extension length
L_c	Control gate
L_s	Screen gate
t_{ox}	gate oxide thickness
t_{si}	silicon film thickness
t_{box}	buried oxide thickness
T_{fin}	thickness of fin
T_{eff}	Effective thickness of fin
H_{fin}	height of fin
H_{eff}	Effective height of fin

Materials considered with their chemical formula

Si	Silicon
Ge	Germanium
InGaAs	Indium Gallium Arsenide
GaN	Gallium Nitride
Al	Aluminium
Ta	Tantalum
Ti	Titanium
Ni	Nickel
Au	Gold
Pt	Platinum
SiO_2	Silicon Dioxide
HfO_2	Hafnium Oxide
Al_2O_3	Aluminium Oxide
Si_3N_4	Silicon Nitride

Chapter 1

INTRODUCTION

The present-day witnesses an inevitable domination of electronics for the smooth conduction of our day-to-day activities. Electronics have reached every strata of mankind as people have become accustomed to living a digital life. Hence there is a high demand for reasonably priced, energy-efficient and portable electronic products that satisfy the needs and preferences of people all over the world. The development of tiny, real-world-producible, power-efficient transistors is now imperative. Ever since the invention of the first transistor in 1947, the scientific community has put utmost effort into fabricating transistors superior to those in existence at the time. Planar single gate Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), were unable to keep up with the increasing demands for speed and power as technology developed. To create advanced transistors that meet the needs of modern Very Large Scale Integrated circuits (VLSI circuits), novel and multi-gate structures such as Double Gate MOSFET (Solomon *et al.* (2003)), Gate-All-Around MOSFET (Sleight *et al.* (2010)), Tunnel FET (Avci *et al.* (2015)), FinFET (Jurczak *et al.* (2009)) etc have been developed. Apart from creating innovative non-conventional architectures, applying methods like adjusting the channel doping profile and choosing gate materials enhances transistor efficiency while tackling the problem of Short Channel Effects (SCE).

An invention in 2011 by J.P Colinge introduced a new category of transistor named "Junctionless Transistor". As the name suggests, it is uniformly doped throughout the semiconductor film such that there doesn't exist any p-n junction in the active region. As a result, forming a very small and shallow source and drain regions in a substrate containing dopants of opposing polarity can be avoided. This simplifies the fabrication process. Due to their bulk conduction mechanism, unlike surface conduction in

conventional MOSFETs, junctionless transistors (JLTs) are less resistant to damage caused by poor quality gate oxide-semiconductor interfaces and surface trap charges. To ensure full depletion of extensively doped semiconductor film in the OFF state of a JLT, work function of gate material should be greater. As the gate voltage (V_{GS}) is increased, JLT traverses through four regions of operation: (a) full depletion, (b) partial depletion, (c) flat band region and (d) accumulation. The threshold voltage is defined as the gate voltage when JLT switches from full depletion to partial depletion and the transistor starts conducting current. Comparing the performance of junctionless FETs with conventional FETs, there is improvement in the characteristics exhibited by junctionless devices. Improvement in SCEs like Drain Induced Barrier Lowering (DIBL) and Sub-threshold Swing (SS) is visible in junctionless transistors compared to conventional transistors especially at gate lengths as low as 20 nm (Singh and Yadav (2022), Park *et al.* (2012)).

Researchers from all over the world have investigated on various methods that can improve the properties of JLTs. Adopting non-uniform doping techniques such as step and Gaussian doping could enhance the performance of JLTs (Mondal *et al.* (2013), Song and Li (2014)). In comparison to a uniformly doped structure, a non-uniform doping profile in JLT results in a lower OFF current (I_{OFF}) and better suppression of SCE. However, they suffer from fabrication challenges as well as inherent depletion regions in the channel due to gradients in doping concentration. Multiple studies were conducted on JLT with germanium channel (Wu *et al.* (2014)), Indium Gallium Arsenide channel (Pan *et al.* (2015)) and Gallium Nitride channel (Im *et al.* (2013)).

Since the gate material's work function is a crucial factor in determining how a JLT operates, engineering the gate terminal is expected to have a major impact on transistor properties. Hence, numerous works were published in the literature which highlight the merits of Dual Material Gate (DMG) or Triple Material Gate (TMG) in a JLT. By placing a metal with a higher work function near the source side and a lower work function near the drain side, the influence of drain bias on channel potential can be effectively minimized. This gives way to a lesser shift in threshold voltage with drain bias and hence SCE like DIBL can be efficiently suppressed (Lou *et al.* (2012), Li *et al.* (2014)).

Many articles exist that examine the performance of multi-gate junctionless transistors because multi-gate structures allow for increased gate control over channel region. Some of the multi-gate JLTs are Double Gate Junctionless Transistor (DGJLT) (Duarte

et al. (2011)), Junctionless Fin Field Effect Transistor (JLFinFET) (Liu *et al.* (2013)), Gate-All-Around Junctionless Transistor (GAAJLT) (Yang *et al.* (2018)) and Cylindrical Gate-All-Around Junctionless Transistor (CGAAJLT) (Lime *et al.* (2014)). A schematic representation of junctionless transistors with more than one gate is shown in Figure 1.1. It is observed that employing more than one gate will improve the performance by several orders of magnitude making multi-gate architecture an attractive idea among device engineers.

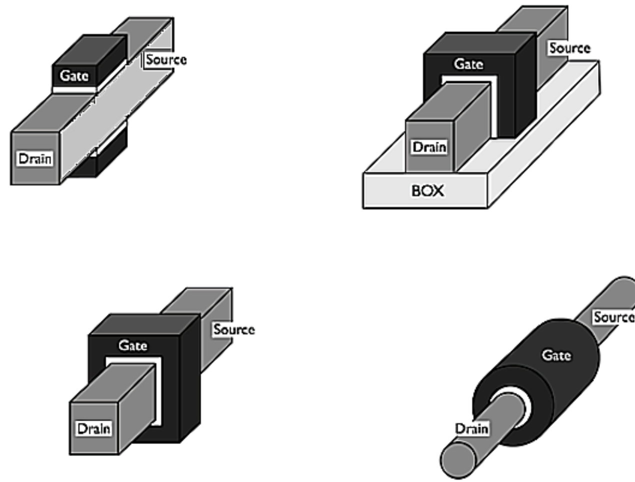


Figure 1.1: Schematic representation of (a) DGJLT (b) JLFinFET (c) GAAJLT and (d) CGAAJLT (Kim *et al.* (2014)).

The gate control over the channel is strengthened by using appropriate dielectric materials as spacers on each side of the gate (Gundapaneni *et al.* (2011)). Hence transistor with spacers exhibits superior characteristics and are more resistant to SCE. However, due to the higher gate capacitance, selecting oxides with higher dielectric constants (κ) has the disadvantage of lowered Radio Frequency (RF) metrics like unity gain cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) (Baruah and Paily (2013*b*)). To maintain the advantages of having spacers without compromising RF metrics, dual κ spacer technology is used (Sreenivasulu and Narendar (2022)). However, dual κ technology faces fabrication challenge due to the placement of different dielectric materials side-by-side on both sides of the gate.

Several studies focusing on DGJLT with DMG and spacers were published to investigate the degree of improvement in device characteristics with both technolo-

gies (Baruah and Paily (2013*a*), Amin and Sarin (2016)). When DMG and spacer technology are combined, significant improvements are shown in the Direct Current (DC) and analog parameters. However, less research has been done on the design space associated with the coupling of DMG and spacer technologies in a market-friendly FinFET version in the junctionless regime. Thus, in this thesis, a thorough analysis is done on the electrical behavior of the DMG JLFinFET with a spacer.

Along with cross-inspecting the characteristics of a transistor with Technology Computer Aided Design (TCAD) simulations, it is necessary to frame a mathematical expression for various parameters like threshold voltage (V_{th}), drain current (I_d), etc considering the physics involved in its functioning. To forecast the behaviour of multi-transistor circuits constructed using newly developed transistors, circuit simulators are fed with their mathematical models. Device engineers therefore create reliable mathematical models that can replicate the behaviour of newly proposed transistors. Numerous precise and time-efficient models for JLTs can be found in the literature. An exclusive survey on the threshold voltage model of JLTs has produced several interesting articles that model V_{th} for various JLT categories like SOIJLT (Gnani *et al.* (2012))), DGJLT (Chiang (2012), Jiang *et al.* (2015)), CGAAJLT (Hu *et al.* (2014)) and JLFinFET (Trevisoli *et al.* (2013), Hu *et al.* (2016)). These articles present V_{th} models of JLTs with gate lengths ranging from 10 nm to 1 μm.

Several research groups have worked on mathematical models of DMG JLTs. However, V_{th} models were derived mostly for DMG in DGJLT and CGAAJLT owing to the simplicity posed by these two structures due to their structural symmetry. V_{th} model developed for DMG DGJLT agrees well with TCAD simulation results (Agrawal *et al.* (2015), Awasthi *et al.* (2022)). V_{th} models developed for CGAAJLT with gate length (L_g) in the range of 10 nm to 100 nm are available in the literature. Analytical models developed for V_{th} matches closely with simulated results and also the superior performance of DMG devices over SMG devices is observed (Li *et al.* (2013), Biswal *et al.* (2015)). Temperature-dependant V_{th} model for DMG CGAAJLT that takes into account effects due to localized charges is derived (Pratap *et al.* (2015*a*)). This work highlights the lesser impact of localised charges on V_{th} of DMG when compared with SMG structure. Preethi and Balamurugan (Preethi and Balamurugan (2021)) use finite differentiation method to accurately model V_{th} of CGAAJLT.

As the present-day semiconductor market is manufacturing FinFET-based circuits for various applications, it is necessary to explore the modeling space of FinFET

despite the difficulty posed by them due to their non-symmetrical structure. Hence this thesis derives the potential in the channel of a JLFinFET with DMG and then subsequently presents the closed form analytical model for their threshold voltage.

1.1 Motivation for the present work

To create the best circuits for electronic devices, there is a constant and passionate search for the "perfect" transistor. JLTs emerge as a suitable candidate for transistors with lower dimensions as their fabrication is relatively easy. To get optimal results in JLTs, many approaches across various JLT types are investigated. When DMG is used in a JLT, performance is shown to significantly improve. Many research articles focus on improvements obtained by using DMG in DGJLT (Chebaki *et al.* (2016)) and CGAAJLT (Lou *et al.* (2012)). However, the design space of DMG in JLFinFET is less explored. As the semiconductor market relies on FinFET-based circuits, it is necessary to qualitatively investigate the magnitude of enhancement in characteristics of JLFinFET with DMG. It is also observed that choosing suitable spacers will further improve the device performance metrics while keeping SCE at bay. Hence a detailed exploration of using spacers in a DMG JLFinFET gives insight on their suitability to construct superior circuits and systems. From an application perspective, it is imperative to model the characteristics of DMG JLFinFETs. Accurate, efficient models can be plugged into a circuit simulator, to observe the behaviour of multi-transistor circuits made of DMG JLFinFET. Furthermore, to the best of our knowledge, no literature exists that discusses the modeling of JLFinFET with the DMG architecture. Based on these observations, research objectives are derived.

1.2 Research Objectives

- To evaluate the effect of gate material work function along with their length ratios on DC characteristics and short channel effects and hence provide design guidelines for dual material gate junctionless FinFET suitable for 10 nm regime.

- To determine the impact of dielectric constant and length of spacer material in improving current characteristics and suppressing short channel effects of a dual material gate junctionless FinFET.

- To analytically model threshold voltage and sub-threshold swing of single material gate junctionless FinFET.
- To analytically model channel potential and the threshold voltage of dual material gate junctionless FinFET.

1.3 Organization of the Thesis

The focus of this thesis is to analyse the electrical characteristics of DMG JLFinFET with different gate material combinations and determine the performance enhancement obtained by adding various dielectric oxides as spacers. This thesis also focuses on developing analytical models for parameters like threshold voltage of both Single Material Gate and Dual Material Gate JLFinFET.
Chapter 2, reports the background of junctionless transistors, their functioning and unique features. Further, a brief discussion on various innovative techniques incorporated in junctionless transistors for performance enhancement is presented. The key literature highlighting the effect of dual material gate as well as spacer engineering in junctionless transistors is discussed. A survey of threshold voltage modeling in junctionless transistors with different ranges of channel lengths is also done.
Chapter 3, gives a detailed analysis of the impact of gate material properties on the characteristics of DMG JLFinFET. The influence of work function as well as the length ratio of gate materials on SCE is also presented and requirement-based design guidelines for DMG JLFinFET are provided.
Chapter 4, describes the effect of the dielectric constant and length of the spacer on DC characteristics as well as SCE of DMG JLFinFET. This chapter also presents the influence of various spacer materials on analog Figures of Merit.
Chapter 5, gives a potential-based analytical model for the threshold voltage and subthreshold swing of single material gate JLFinFET taking into account the location of onset of current conduction.
Chapter 6, gives a potential-based analytical model for the channel potential and threshold voltage of dual material gate JLFinFET.
Finally, Chapter 7, concludes this thesis by describing the contribution of this thesis and throwing highlights on possible future works.

Chapter 2

LITERATURE REVIEW

2.1 Introduction

Electronic goods play a pivotal role in enhancing the quality of life for mankind. There is always an increased demand for smaller, energy-efficient and low cost electronic devices. Hence scientists are continuously striving to create the ideal transistor through ongoing research and development efforts. As a result of this, many new transistors were invented over time, that display superior characteristics compared to the existing devices. One such invention happened in 2011 when J. P. Colinge proposed a new category of transistors named Junctionless Transistors (JLT). JLT has an active region that is uniformly doped throughout with dopant of the same type (Colinge *et al.* (2011)). These transistors do not have p-n junctions in their active region (source-channel-drain). In this chapter, a brief discussion is done on the operation and conduction mechanisms of junctionless transistors as well as innovations to improve their performance and suppress SCE. Research works highlighting the effect of Dual Material Gate (DMG) as well as spacers on the characteristics of JLTs are reviewed. Finally, several analytical models of JLTs are examined with a particular focus on threshold voltage modeling in JLTs with DMG architecture.

2.2 Junctionless Transistor

The junctionless transistor is a type of transistor without any p-n junctions in its active semiconductor region. The gate terminal of a JLT controls the channel's resistance, which in turn controls the current that passes through the transistor. As the transistor

scales down in size, the challenges involved in developing an extremely shallow source and drain regions in a substrate containing dopants of opposite polarity, was the key motivation behind the invention of JLT. Hence fabrication process was expected to be significantly simpler.

2.2.1 Basic Structure of JLT

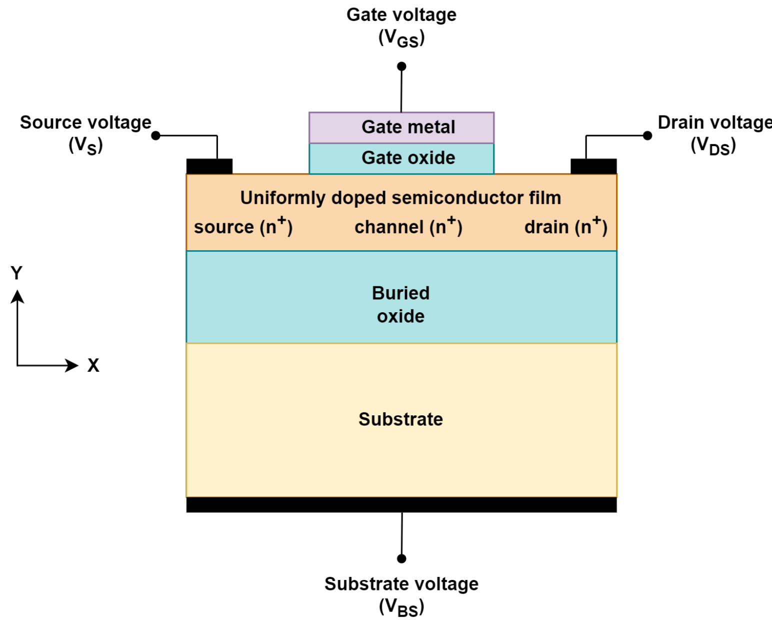


Figure 2.1: Cross-sectional view of SOIJLT.

The basic structure of a JLT comprises a heavily doped thin semiconductor layer (active region) over a substrate (bulk or SOI). N-type JLT has an active region doped with n-type impurities while p-type JLT has p-doped active region. When a bulk substrate is used, dopants within the active region are of opposite polarity compared to the dopants present in the semiconductor substrate, thus creating a p-n junction vertically. The depletion region formed due to this p-n junction isolates the active region from the bulk. However, when SOI substrate is used, buried oxide plays the role of isolating the active layer from the bulk. The cross-sectional view of JLT with SOI substrate (SOIJLT) is shown in Figure 2.1. Gate oxide is located above the channel as shown in Figure 2.1. Above the gate oxide, suitable material (metal or polysilicon) is deposited for the gate contact. Metallization is done beneath the substrate and over source and drain regions as shown in Figure 2.1 for substrate, source and drain

contacts respectively.

2.2.2 Current Conduction Mechanism

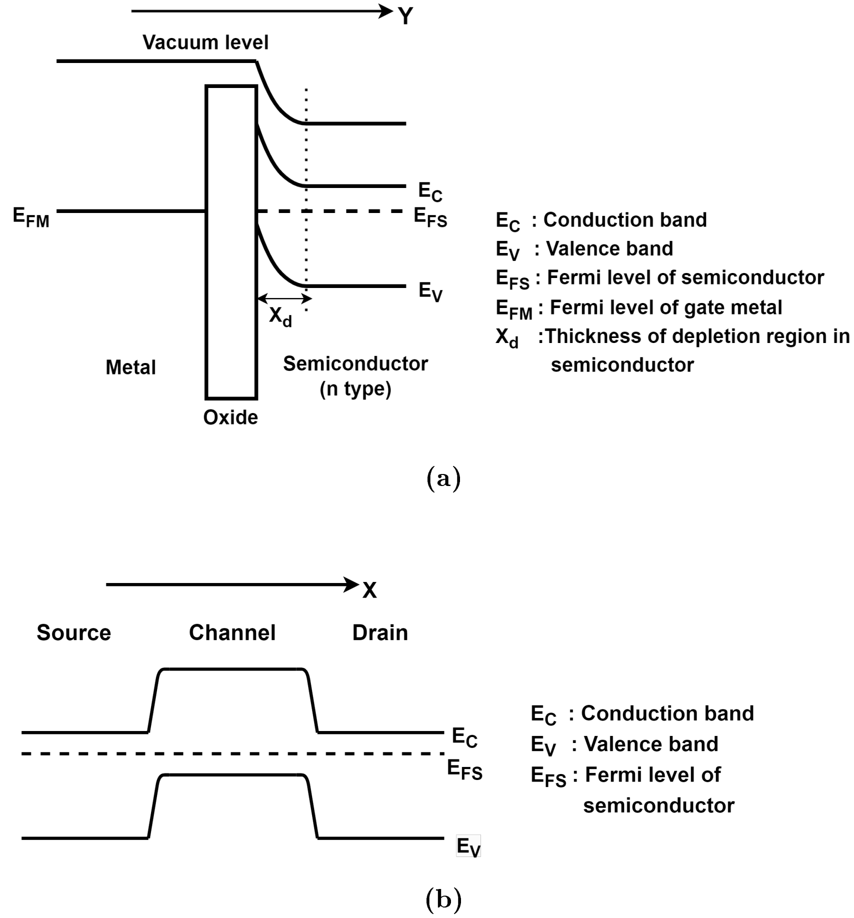


Figure 2.2: Energy band diagram along (a) vertical cross-section and (b) horizontal cross-section, of an n-type JLT at equilibrium.

At zero gate bias, the difference in the work function of the gate material (ϕ_{M}) and the active layer (ϕ_{S}) is the fundamental factor that decides whether the JLT is in ON state or OFF state. It may be noted that OFF state of a transistor refers to the situation when gate bias is lesser than threshold voltage and channel is therefore completely depleted preventing current flow. In ON state, $\mathrm{V_{GS}}$ is greater than $\mathrm{V_{th}}$ and current flows through the channel upon applying a positive drain voltage. For n-type JLT, a metal with a high value of work function ($\phi_{\mathrm{M}} \geq 5$ eV) is chosen as the gate material. The source-channel-drain region in JLT is uniformly doped with

high doping concentration ($N_d \geq 10^{19}$ cm^{-3}) to ensure a highly conductive channel path and thereby obtaining a high drain current (I_d). As a result, JLTs are expected to operate faster and more efficiently (Colinge *et al.* (2010*a*)). When $\phi_M - \phi_S > 0$ (there exists a difference in Fermi level of gate and semiconductor), Fermi levels then tend to align by pushing away electrons from gate oxide-semiconductor interface. This lead to uncovering the immobile dopant ions near the semiconductor-gate oxide interface. As a result the bands bend as shown in Figure 2.2(a) and 2.2(b). Hence at zero gate bias, the channel gets depleted of mobile charge carriers and the transistor is in OFF state. However, a voltage applied at the gate terminal, modulates the conduction-valence bands and hence control the current flow through the channel. Drain bias is fixed to a suitable voltage both in ON state and OFF state. V_{DS} aids in electron flow from source to drain during ON state. When the gate bias gets more negative (consider n-type transistor), it aids in depleting the channel more thereby turning the transistor OFF. When V_{GS} is increased in positive direction, the depletion in the channel reduces, hence the barrier existing between source and channel as well as drain and channel reduces and the transistor turns ON. On applying a suitable drain bias, current flows through the bulk of the channel between the source and drain depicting bulk conduction phenomenon. It is also necessary to have a thin semiconductor film as active region in a junctionless transistor to ensure full depletion of the channel region at zero gate bias despite heavy doping in the channel region.

2.2.3 Regions of Operation

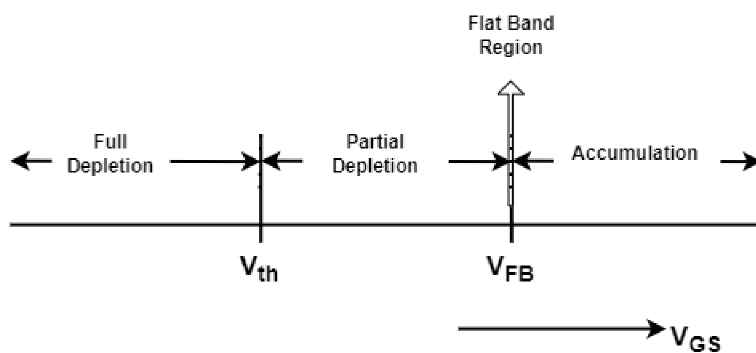


Figure 2.3: Regions of operation marked on V_{GS} axis.

Since the operation of a junctionless transistor differs greatly from that of a conventional "junctioned" transistor, it is essential to understand how changes in gate bias cause JLTs to switch among different operating regimes. The various regions of operation of a JLT discussed by Colinge *et al.* (2011) is depicted in Figure 2.3. All the explanations by default pertain to n-type JLT.

2.2.3.1 Full Depletion

When V_{GS} is zero or negative, the channel of JLT is expected to be completely depleted of mobile charge carriers. Hence hardly any current flows through the channel. JLT is then said to be in full depletion and the transistor is in OFF state. The semiconductor film must be thin enough as well as work function of gate material should be higher to ensure full depletion of the channel at zero gate bias.

2.2.3.2 Partial Depletion

As V_{GS} increases from zero in the positive direction, the depletion region across the source-channel-drain region starts uncovering and at a particular gate voltage, a neutral film extends from source to drain. This voltage is known as threshold voltage (V_{th}). When V_{GS} is further increased above V_{th}, more and more parts of the channel get undepleted, making way for current to flow through the channel. This region where the channel is partially depleted and is capable of passing current through it is called partial depletion. The partial depletion regime extends until the entire channel gets undepleted and becomes a neutral film conducting current. It is observed that the location in the channel where the neutral film starts forming depends on the type of JLT. Hence when the transistor crosses threshold, the current starts flowing through the neutral region formed in the channel which is mostly located in the bulk of the transistor. This is unlike the conventional transistor where current flows through the surface of the channel.

2.2.3.3 Flat Band Region

JLT is said to be in a flat band region when the entire channel is neutral (without any depletion region) and the whole film conducts current through it. The gate voltage at which the transistor reaches this state is known as flat band voltage (V_{FB}).

2.2.3.4 Accumulation

When V_{GS} is further increased from flat band voltage, electrons start getting attracted toward the semiconductor-gate oxide interface. Under the influence of a positive drain bias current starts flowing through the semiconductor-gate oxide interface (surface conduction) and the transistor is said to be in the accumulation region.

Electron concentration profile inside the cuboidal semiconductor region of a JLT for various gate biases is shown in Figure 2.4. It must be noted that when the transistor switches to partial depletion region, it turns ON. JLT generally operates in full depletion, partial depletion and flat band region. In accumulation region more electrons pile up near semiconductor-gate oxide interface This in turn increases surface scattering, interface traps, carrier-carrier scattering etc. Hence mobility gets degraded and transconductance decreases in a JLT under accumulation.

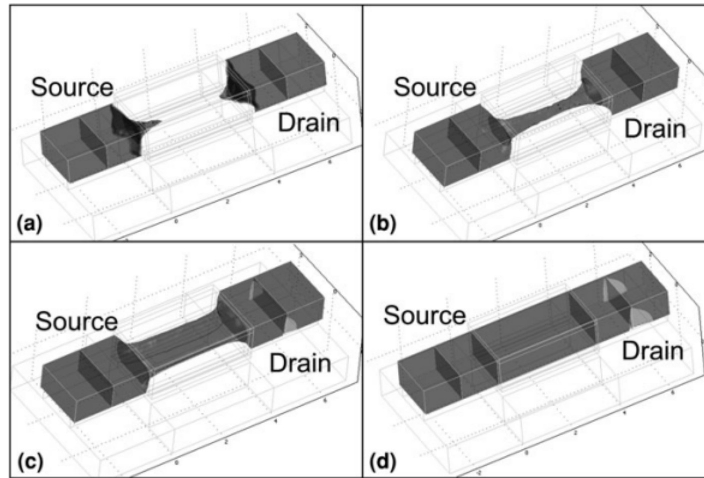


Figure 2.4: 3-D electron concentration profile in an n-type JLT for (a) $V_{GS}<V_{th}$ (b) $V_{GS}=V_{th}$ (c) $V_{GS}>V_{th}$ (d) $V_{GS}=V_{FB}>>V_{th}$ (Colinge *et al.* (2011)).

Figure 2.5 shows the 3-D electron concentration profile in the active region of a JLT with increasing drain voltage (in the positive direction) when the transistor is in ON state. It can be seen that the performance of a JLT with an increase in V_{DS} is the same as a conventional MOSFET. In the ON state, when V_{DS} is increased with a fixed V_{GS}, the depletion region broadens and thereby channel tapers near the drain terminal and eventually gets pinched off. When V_{DS} is increased further, I_D remains constant and the transistor enters in saturation region like a conventional MOSFET.

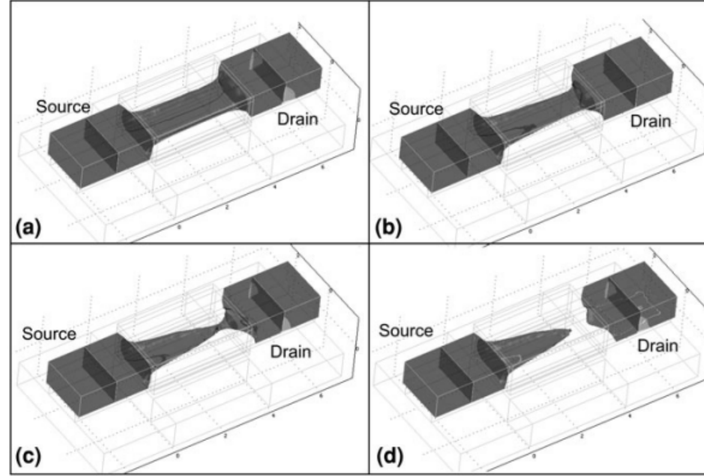


Figure 2.5: 3-D electron concentration profile in an n-type junctionless transistor for (a) V_{DS} = 50 mV (b) V_{DS} = 200 mV (c) V_{DS} = 400 mV and (d) V_{DS} = 600 mV for $V_{GS} > V_{th}$ (Colinge *et al.* (2011)).

2.3 Unique Features of Junctionless Transistor

The working principle of junctionless transistors is different compared to conventional MOSFETs. JLT possesses distinctive characteristics that distinguish it from conventional transistors. Some of them are

1. Bulk conduction:- The current in a JLT starts flowing through a channel created at the bulk of the transistor when gate voltage exceeds the threshold voltage. This feature doesn't exist in conventional MOSFETs where the conducting channel is created at the gate oxide-channel interface. Hence the conduction mechanism is bulk conduction in a JLT. Therefore surface scattering and interface trap effects don't play a major role in affecting mobility of carriers in a JLT.

2. Effective channel length:- In a JLT, the distance between the undepleted source and undepleted drain is defined as effective channel length. When the device is OFF, effective channel length will be lower at the bulk (lower than physical gate length) and more at the channel region near the gate (more than the physical gate length) as shown in Figure 2.6. With more negative gate bias, effective channel length can be increased further which can be greater than the physical gate length throughout (bulk to interface). However in the ON state, the physi-

cal length of gate (L_g) is considered as effective channel length.

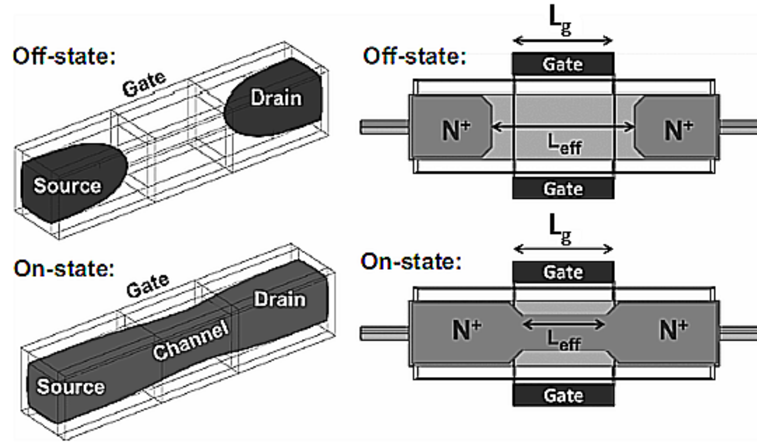


Figure 2.6: Effective channel length of JLT (Colinge (2018))

3. High flat-band voltage:- Unlike in conventional MOSFET, junctionless transistors have flat band voltage which is significantly higher than threshold voltage. This can be attributed to the high work function of gate material used, to deplete the entire channel when no bias is applied (Colinge *et al.* (2011)).

4. Low electric field in channel in ON state:- In the ON state of JLT, as the channel becomes neutral without any depletion charges, it has very low electric field. This facilitates reduced mobility degradation caused by the electric field in the channel (Colinge *et al.* (2010*b*)).

5. Mobility degradation due to impurity scattering mechanism:- As the active region in a JLT is heavily doped, ionized impurity atoms act as scattering centers affecting the path of current carriers and hence mobility is degraded. However, this degradation in mobility significantly reduces due to shielding effect in weak accumulation mode of operation (Rudenko *et al.* (2012)). Phonon scattering and surface roughness scattering which play a significant role in degrading mobility in conventional MOSFET doesn't have much significance in affecting mobility in JLT.

6. Enhanced carrier ballisticity:- Unlike in conventional MOSFETs, since there are no p-n junctions in junctionless transistors, source-channel barrier height van-

ishes in the ON state. This prevents back-scattering events in a JLT and therefore enhances carrier ballisticity in the sub-10 nm regime (Dehdashti Akhavan *et al.* (2011)).

7. Reduced short channel effects:- JLT also faces degradation in its performance due to SCE like inversion mode transistors. Nevertheless, the magnitude of performance degradation due to SCE like Drain Induced Barrier Lowering (DIBL), V_{th} roll-off and Sub-threshold Swing (SS) is considerably less in a JLT (Lee *et al.* (2010), Colinge *et al.* (2010*b*)).

8. Band-to-band tunneling in OFF state:- When the heavily doped channel in JLT is volume depleted, the bands in the channel across the length of JLT, bend as shown in Figure 2.2(b). Supplying more negative voltage at the gate terminal and a suitable positive voltage in the drain terminal, causes the energy bands to bend in such a way that there is a significant overlap between the valence band of the channel region and the conduction band of the drain region. This in turn gives rise to the tunneling of electrons at the channel-drain interface (from the valence band of channel to the conduction band of the drain). Hence band-to-band tunneling current flows in the OFF state of a JLT (Sahay and Kumar (2016)).

9. More sensitivity to process variations:- JLT is sensitive to process variations like line edge roughness, work function variability and channel width variation. As the channel width and work function of gate material are fundamental parameters in deciding electrical characteristics (ON current, threshold voltage etc), JLT is more susceptible to process variations than conventional MOSFETs (Nawaz *et al.* (2014)).

2.4 Innovations to Enhance the Performance as well as Reduce the Short Channel Effects in a Junctionless Transistor

As the channel length shrinks, JLTs face challenges due to SCE as well as its inherent demerits like sensitivity to process variations, band-to-band tunneling in OFF state,

mobility degradation due to impact ionization, realising volume depletion with feasible semiconductor film thickness etc. Immense research is going on to invent various techniques that enhance the transistor performance while suppressing SCE to a minimum. These include using non-planar multi-gate structures, engineering the gate material, using high mobility channel materials with various types of non-uniform doping concentrations and incorporating various structural modifications. This section provides an overview of diverse approaches applied to junctionless devices, aiming to achieve enhanced transistor performance while simultaneously mitigating SCE.

2.4.1 Active Region with Non-uniform Doping

2.4.1.1 JLT with Gaussian Doping

In Gaussian-doped JLT (GDP JLT), doping concentration along the thickness of semiconductor film (t_{si}) is Gaussian in nature (Mondal *et al.* (2013)). However, the doping profile along the length of the active region (lateral direction) is uniform as shown in Figure 2.7. Gaussian doping profile in the active region is obtained by ion-implantation process. Effective doping concentration at a given location in the active region (N_d (x,y)) is given by equation 2.1, where N_{peak} is the peak doping concentration present at the top surface of semiconductor active region, σ is the standard deviation of the doping concentration spread around peak concentration.

$$N_d(x,y) = N_{peak} \exp\left(-\frac{y^2}{2\sigma^2}\right) \tag{2.1}$$

Compared to uniformly doped JLT, efficient volume depletion is realized in GDP JLT as the lower doping concentrations near the semiconductor-buried oxide interface aid in extending the depletion region further. Also, lower doping concentration near buried oxide reduces mobile carriers available for conduction in the OFF state. Hence a much lower OFF current (I_{OFF}) is observed in GDP JLT. However, GDP JLT suffers from lower ON current (I_{ON}) due to the large resistance offered by active region in the ON state. Two factors contribute to large channel resistance. (1) Inherent depletion in the channel due to n^+-n junctions. These junctions arise out of doping gradient along Y direction in the channel. (2) Lower doping concentration at semiconductor-buried oxide interface.

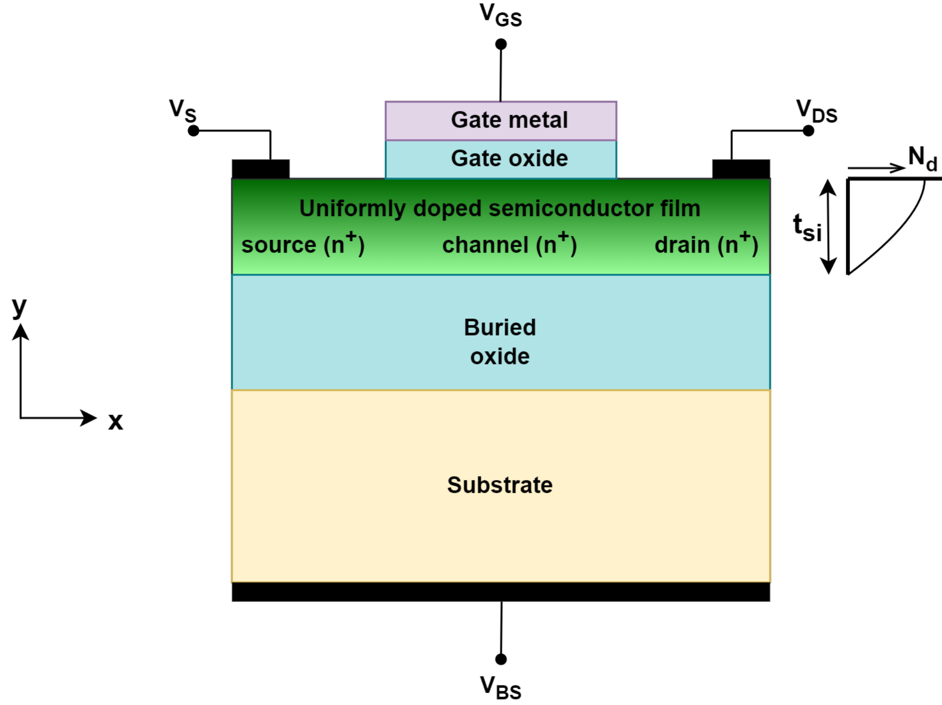


Figure 2.7: Structure of Gaussian-doped JLT.

2.4.1.2 JLT with Step Doping

In Step-doped JLT (SDP JLT), the active region consists of two regions with distinct doping concentration. The active region is vertically divided into two regions where, the region near the gate has a high doping concentration and the region near buried oxide has low doping concentration. Step doping in the active device layer of a multi-gate junctionless structure with SOI substrate is given by (Song and Li (2014)). I_{ON} improves and I_{OFF} decreases in a SDP JLT. SDP JLT has the added advantage of better immunity to SCE. However, they suffer from technological challenges involved in realising a step doping profile in the active layer. It becomes very difficult to achieve ultra-sharp doping transition between two regions using processes like ion implantation.

2.4.2 Alternate Material for Active Region of JLTs

As the current conduction path in the ON state of JLT is at the bulk, the effects of interface traps and defects which arise when materials without naturally occurring

oxide are used, become insignificant. This opens the door to the possibility of using high mobility material-based JLT rather than silicon-based JLT (Si JLT) to increase transistor performance.

2.4.2.1 Germanium JLT

Due to reduced interaction between the gate dielectric-semiconductor interface and carrier flow, inherent drawbacks of utilising germanium as a semiconductor material, such as the inability to generate a high-quality gate dielectric and the existence of interface defects and traps, are eliminated in junctionless architectures. In germanium JLT (Ge JLT), Fermi level pinning near valence band aids in better depletion of channel region and therefore efficient volume depletion can be realised (Wu *et al.* (2014)). Quantum confinement in Ge JLT also supports efficient volume depletion of the channel thereby enhancing its performance (Jhan *et al.* (2015)).

2.4.2.2 Indium Gallium Arsenide JLT

In a conventional MOSFET with Indium Gallium Arsenide (InGaAs) semiconductor material, performance is seriously degraded due to surface traps and defects. These MOSFETs have much negative threshold voltage unsuitable for circuit applications. However, junctionless transistor with InGaAs material (InGaAs JLT) doesn't suffer from surface traps and defects owing to the volume conduction phenomenon of junctionless structures, thereby offering a positive threshold voltage suitable for logic applications (Djara *et al.* (2016)). InGaAs JLT exhibits higher I_{ON} than Si JLT due to lower rate of impurity scattering in the InGaAs channel (Pan *et al.* (2015)). Improvement in SCE is also expected in InGaAs JLT due to the large barrier height at the source-channel interface.

2.4.2.3 Gallium Nitride JLT

Gallium Nitride junctionless transistors (GaN JLT) have lower I_{OFF} and enhanced breakdown voltage as compared to inversion mode GaN transistors (Im *et al.* (2013)). Fabricating GaN JLTs on a silicon substrate offers the benefit of a substantial valence band offset, which effectively blocks tunneling and diffusion currents Lee *et al.* (2015).

2.4.3 Gate Electrode Engineering

As the gate work function (ϕ_M) is a key factor that determines the transistor characteristics in a junctionless transistor, constructing the gate electrode with two or three materials having suitable work functions promotes better functioning of JLTs.

2.4.3.1 Dual Material Gate

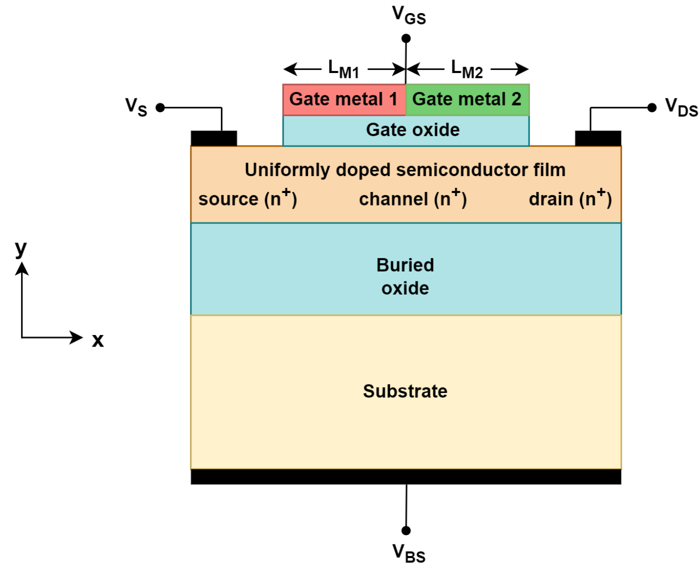


Figure 2.8: Structure of Dual Material Gate JLT.

In a Dual Material Gate (DMG) architecture, the gate terminal comprises two different metals kept side by side such that metal near the source (with length L_{M1}) has in general, a higher work function than metal near the drain (with length L_{M2}). The schematic diagram of a DMG junctionless transistor (DMG JLT) is shown in Figure 2.8. This kind of gate composition has a significant effect in reducing SCEs like DIBL. This is because the gate material with lower work function (located near drain) screens the channel beneath the gate material with higher work function, from drain field thereby reducing the impact of drain on channel field. This type of architecture has the added advantage of better carrier transport efficiency which in turn results in better current driving capacity (Lou *et al.* (2012)).

2.4.3.2 Triple Material Gate

In a Triple Material Gate (TMG) structure, the gate electrode comprises three metals (with lengths L_{M1}, L_{M2} and L_{M3}) placed side by side such that the metal closer to the source has the highest work function and the metal closer to the drain has the least work function among all the metals used to construct the gate electrode. The schematic of a Triple Material Gate JLT (TMG JLT) is shown in Figure 2.9. This type of gate architecture introduces two steps in the electrostatic potential profile in the channel. Better suppression of DIBL and improved carrier transport efficiency is expected in TMG JLT (Li *et al.* (2014)). However due to the difficulty in depositing three different gate materials side by side especially in nanometre ranges, TMG structures are difficult to fabricate compared to DMG structures.

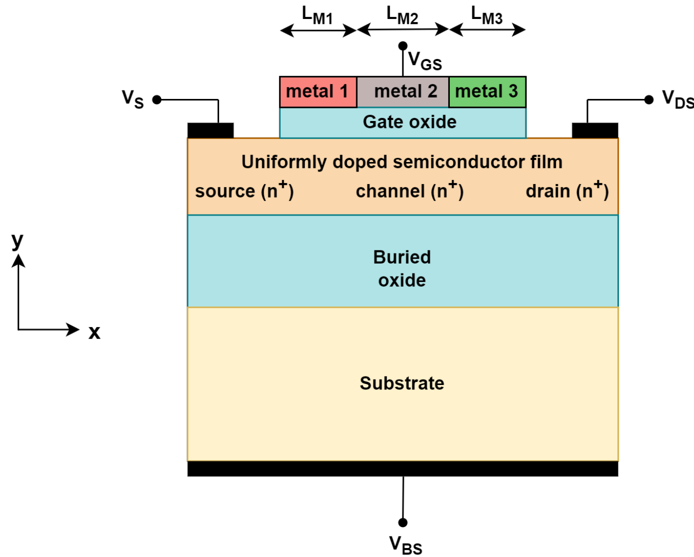


Figure 2.9: Structure of Triple Material Gate JLT.

2.4.4 Multi-Gate Junctionless Transistors

The purpose of adding many gates to a transistor is to increase the gate's control over the channel region, which will improve the performance of the transistor as well as decrease SCE. Various multi-gate structures used in junctionless transistors are described here.

2.4.4.1 Double Gate Junctionless Transistor

Double Gate Junctionless Transistor (DGJLT) has two gates on both sides of the active region as shown in Figure 2.10. The presence of two gates aids in the volume depletion of the channel in the OFF state and enhanced current flow in the ON state. Owing to the enhanced gate control over the channel, there is better suppression of SCE. As DGJLT has a symmetric structure both in x and y directions, modeling various electric parameters is easier. There is abundant literature focusing electrical nature backed by mathematical models for DGJLT (Duarte *et al.* (2011), Kumari *et al.* (2015)).

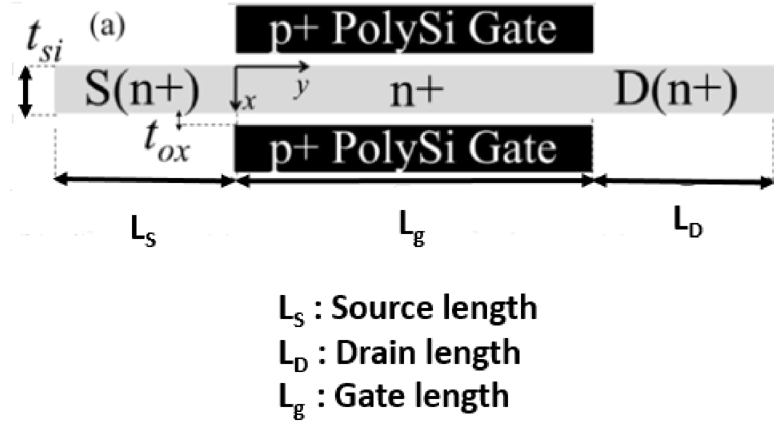


Figure 2.10: Cross-sectional view of Double Gate JLT (Duarte *et al.* (2011).)

2.4.4.2 Junctionless Fin Field Effect Transistor

Similar to conventional Fin Field Effect Transistor (FinFET), junctionless FinFET (JLFinFET), has gate on three sides of the channel. In these non-planar transistors, the gate exerts good control over the channel and modulates the current flow. JLFinFETs can be classified into two categories based on the substrate used.

(a) Junctionless SOI FinFET: In Junctionless FinFET with SOI substrate (SOI JLFinFET), the uniformly doped silicon film lies over a buried oxide substrate. The 3-D schematic view as well as a 2-D cross-sectional view of SOI JLFinFET is shown in Figure 2.11(a). SOI JLFinFET has a higher I_{ON} compared with the Junctionless Bulk FinFET. This is due to the depletion layer formed at active region-bulk sub-

strate junction. As a result there is reduction in effective channel thickness thereby decrease in the area for current flow in a Junctionless Bulk FinFET. However in the SOI counterpart channel thickness doesn't get affected due to the presence of an oxide layer beneath the active region. Hence, from a delay perspective, SOI JLFinFET is a better candidate.

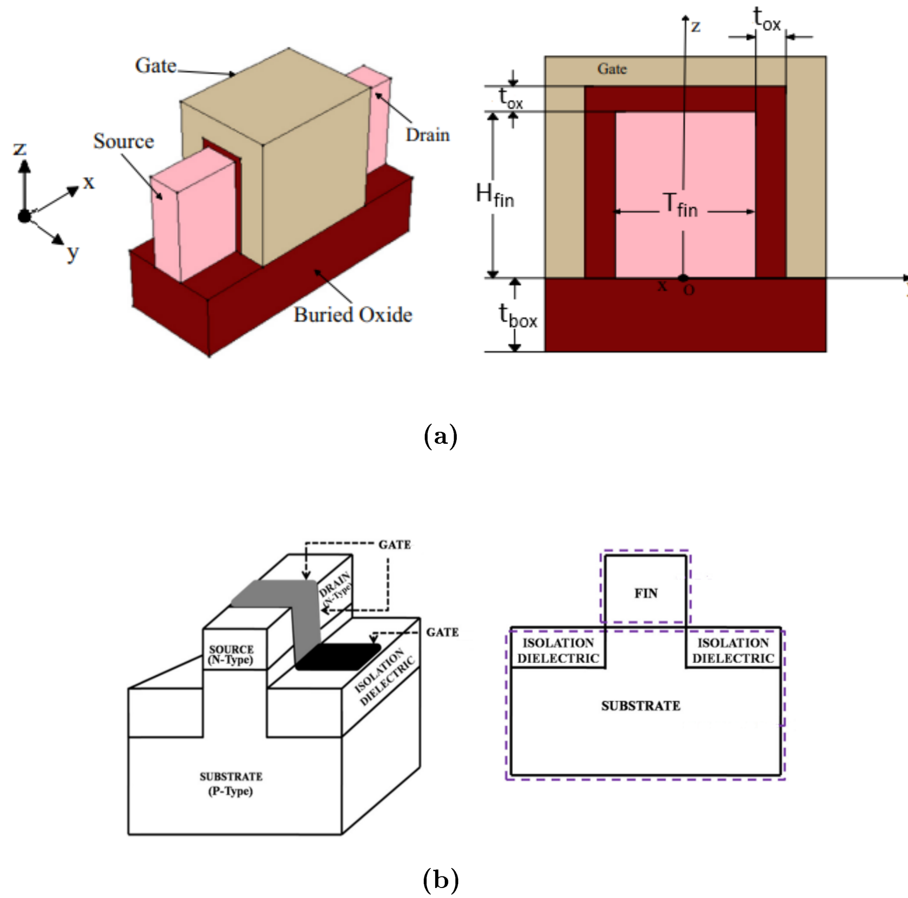


Figure 2.11: 3-D schematic view as well as a 2-D cross-sectional view of (a) SOI JLFinFET (Hu *et al.* (2016)) and (b) Bulk JLFinFET (Scarlet and Srinivasan (2018)).

(b) Junctionless Bulk FinFET: In Junctionless Bulk FinFET (Bulk JLFinFET), uniformly doped silicon film, is situated on the top of a substrate doped with opposite type dopants. The 3-D schematic view as well as a 2-D cross-sectional view of Bulk JLFinFET is shown in Figure 2.11(b). Bulk JLFinFET has a lower I_{OFF} due to effective channel thickness being lower than physical channel thickness. This situation arises due to the presence of a p-type substrate beneath n-type active re-

gion (in n-type transistor), which gives way to the formation of a depletion region near substrate-active region interface that extends into the channel. The width of the depletion region extending into the channel region can be tuned with the doping concentration of the substrate.

2.4.4.3 Cylindrical Gate-All-Around Junctionless Transistor

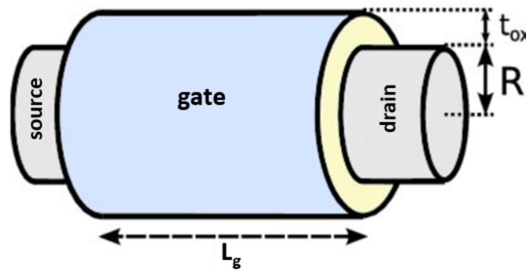


Figure 2.12: 3-D Schematic of Cylindrical Gate-All-Around JLT (Lime *et al.* (2014)).

A Cylindrical Gate-All-Around Junctionless Transistor (CGAAJLT) is a promising candidate due to better gate control over the channel combined with enhanced immunity to SCE. They have the added advantage of fairly simple, symmetric structure. The 3-D schematic view of a CGAAJLT is shown in Figure 2.12. These devices show an extremely high linearity which is beneficial for both analog and Radio Frequency (RF) applications (Wang *et al.* (2013)). However, there are challenges in using CGAAJLT in Integrated Circuits (ICs).

2.4.5 Gate Oxide and Spacer Engineering

As the transistor size shrinks down, using SiO_2 as the gate oxide material is detrimental. This is due to the fact that having a low κ dielectric as gate oxide results in a lower potential barrier at channel-source interface. As holes are formed in the channel due to band to band tunneling of electrons from channel to drain of the transistor, parasitic BJT is formed in the transistor structure. Lower potential barrier at source-channel interface due to low κ dielectric can easily trigger the parasitic BJT action, thereby causing an increase in leakage current during OFF state of the transistor (Ghosh *et al.* (2014)). The short channel effects does not get suppressed easily

with SiO_2 as gate oxide. Hence to improve the transistor characteristics, suitable gate dielectric combinations as well as spacer dielectric compositions play a major role.

2.4.5.1 Gate Oxide Engineered Junctionless Transistors

In a JLT, gate oxide composed of two or more oxide materials (high κ as well as low κ) arranged one above the other or side by side are explored by various researchers and the findings are available in the literature. It is observed that using high κ oxide materials like HfO_2, Al_2O_3, to construct gate oxide, improves I_{ON}, reduces I_{OFF} and suppresses SCE (Bousari *et al.* (2019*b*), Baidya *et al.* (2017)). Improvement is visible in analog and RF parameters like transconductance (g_m) and unity gain cut-off frequency (f_T) when hetero gate dielectric structure is incorporated in junctionless transistors (Baruah and Paily (2015)).

2.4.5.2 Spacer Engineered Junctionless Transistors

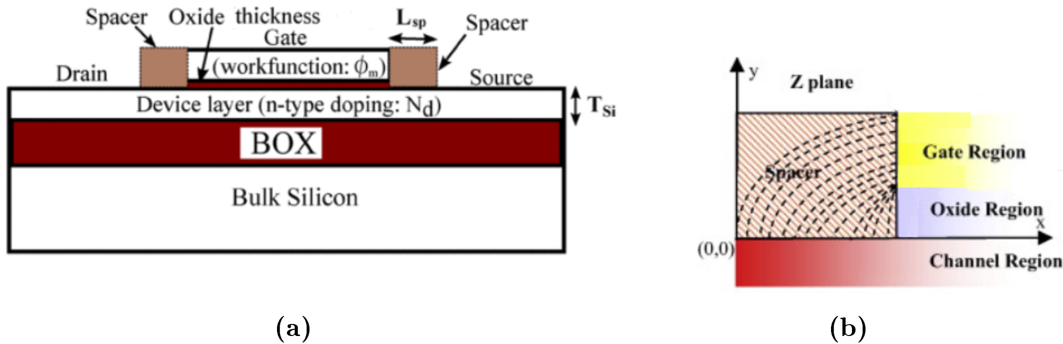


Figure 2.13: (a) 3-D Schematic of SOIJLT with spacer (Gundapaneni *et al.* (2011)) and (b) Fringing field lines passing through sidewall spacer in a JLT (Kumari *et al.* (2015)).

Figure 2.13(a) shows the schematic of a SOIJLT with sidewall spacer. When a voltage is supplied at the gate terminal, electric field lines emanating from the gate electrode pass through the spacer dielectric as shown in Figure 2.13(b). In these devices, the gate is capable of modulating the active region beneath the spacer through fringing field. In the OFF state, a high κ dielectric spacer ensures depletion of the active region beyond the physical gate length and thereby suppresses I_{OFF} significantly. In the ON state, these fringing field enables the channel to provide more carriers for conduction, increasing I_{ON}. Hence the inclusion of high κ spacers improves parameters like ON-

OFF current ratio ($\frac{I_{\text{ON}}}{I_{\text{OFF}}}$), DIBL, SS etc. However, high κ spacers results in larger gate capacitance due to an increase in fringe capacitance. Hence spacers made of suitable high κ-low κ dielectric combinations bring out the best transistor performance.

2.5 Performance Comparison of Junctionless Transistor with Conventional Inversion mode Transistor

While the simplicity of fabrication is a notable advantage, it is essential to thoroughly evaluate the performance of junctionless devices in comparison to conventional junction transistors. Since the birth of JLT in 2011, many articles have been published that closely analyse and compare the behaviour of conventional junction (inversion mode) and junctionless transistors. While the transistor size shrinks, junctionless transistors especially the multiple gate variants like FinFETs and GAAJLT are more immune to SCE (Moon *et al.* (2013), Park *et al.* (2011)). Although I_{ON} of junctionless and conventional transistors lie mostly in the same range, I_{OFF} is lower in junctionless structures. This in turn results in better $\frac{I_{\text{ON}}}{I_{\text{OFF}}}$ for junctionless transistors (Han *et al.* (2013*a*),Thirunavukkarasu *et al.* (2015)). However, various performance metrics like SS, I_{ON}, I_{OFF} etc, are more sensitive to structural parameters in a junctionless transistor (Parihar *et al.* (2013)). Table 2.1 lists some of the key literature comparing junctionless and conventional inversion mode transistors along with their major findings.

Table 2.1: Key literatures which compare performance of junctionless as well as conventional inversion mode transistors.

Type of Transistor	**Published article and Nature of work**	**Gate length**	**Key findings**
DGJLT	**Parihar *et al.* (2013) (simulation-based article)**	**20 nm**	• **Parasitic capacitance lower in DGJLT.** • **Structural parameter sensitivity is more in DGJLT than Inversion Mode DGFET.**

Table 2.1: Key literatures which compare performance of junctionless as well as conventional inversion mode transistors. (Continued).

Type of Transistor	Published article and Nature of work	Gate length	Key findings
GAAJLT	Moon *et al.* (2013) (experiment-based article)	150 nm	• V_{th} roll off lower in junctionless device. • Reducing width of nanowire, improves SS and DIBL.
SOI JLFinFET	Park *et al.* (2011) (experiment-based work)	20 nm	• Both transistors are fabricated. • Measured value of SS and DIBL are low for JLFinFET. • I_{ON} almost same for JLFinFET and IMFinFET.
Bulk JLFinFET	"Han *et al.* (2013*b*) ""Thirunavukkarasu *et al.* (2015) (simulation-based works)	"15 nm ""3 nm	• Bulk JLFinFET has higher $\frac{I_{ON}}{I_{OFF}}$ and better immunity to SCE than Bulk IMFinFET. • SS better in JLFinFET than IMFinFET. • DIBL better in IMFinFET. • I_{ON} is almost same for both transistors.

2.6 Exclusive Survey on research works Incorporating DMG Architecture as well as Spacer Technology in Junctionless Transistors

In Section 2.4, various innovative ways and different architectures adopted for improving the characteristics of junctionless transistors were explained. The focus of this work is on the FinFET variant of the junctionless transistor due to its wide acceptability in the market as these days FinFET-based circuits are manufactured by

the major semiconductor industries. However, using a combination of two techniques, Dual Material Gate (DMG) architecture and spacer technology, on a FinFET variant of junctionless transistor was a research space less explored. As the fabrication complexity involved in constructing JLFinFETs are lower compared to conventional FinFETs especially around 10 nm, incorporating Dual Material Gate (DMG) architecture along with spacer technology on a JLFinFET makes them a better candidate for current technology over a conventional FinFET with DMG and spacer. Hence, in this section, various research works handling junctionless transistors with DMG architecture as well as having spacers are discussed. All the research works mentioned in this section are classified into three categories: (a) junctionless transistors with DMG, (b) junctionless transistors with spacers and (c) junctionless transistors with both DMG and spacers.

2.6.1 Literature Survey on DMG Architecture in Junctionless Transistor

The idea of using a Dual Material Gate in a transistor was invented in 1999 by (Long *et al.* (1999)). It was observed that DMG architecture suppresses SCE as well as enhances transconductance. Since the invention of junctionless transistors in 2011, many research groups have analysed the effect of DMG in a junctionless transistor. It is observed that the inclusion of DMG enhances analog and RF parameters in a planar SOIJLT making them a suitable candidate for CMOS circuits (Wagaj and Patil (2019)). Chebaki *et al.* (Chebaki *et al.* (2016)) draw a comparison between the electrical nature of DGJLT with DMG as well as Single Material Gate (SMG) architecture and conclude that DGJLT with DMG outperforms SMG structure in terms of analog and RF performance parameters.

In 2012, a thorough investigation was done on the impact of using DMG on the device characteristics of a CGAAJLT (Lou *et al.* (2012)). It was observed that, CGAAJLT with DMG has many desirable features, such as high I_{ON}, a large $\frac{I_{ON}}{I_{OFF}}$, improved g_m, high f_T, high f_{MAX} and reduced DIBL. For optimum performance of CGAA JLT, control gate-screen gate ratio of 1:1 and work function difference of 0.5 eV between the gate materials were suggested. In the work by Pravin *et al.* (Pravin *et al.* (2016)), it is proved that CGAAJLT with high κ gate oxides like HfO_2 substantially reduces power dissipation in inverter circuits. Hence CGAAJLT is a good candidate

for low-power VLSI circuits. However, given the extensive use of FinFETs in the semiconductor industry, there is a growing interest in investigating the performance of DMG in JLFinFETs. In the work by Kusuma *et al.* (Kusuma and Talari (2022)), impact of tuning the work functions of metals constituting DMG and using suitable gate oxide combinations on transistor performance metrics is explored. Despite their holistic approach to understanding the behaviour of DMG in JLFinFETs, there has been little investigation into how fine adjusting gate material work function and gate length ratio impact SCE such as DIBL and SS. In this thesis, a detailed investigation is done to understand the behaviour of DMG JLFinFET for gate lengths as low as 10 nm. The dependence of DIBL, SS and relative change in threshold voltage on work functions and length ratios of gate materials were closely analysed. Hence the gate material combinations and length ratios that give the best possible performance in terms of SCE can be determined. Table 2.2 gives a list of notable works (along with their key findings) associated with DMG architecture in junctionless transistors.

Table 2.2: Summary of key literature on DMG in junctionless FETs.

Type of Transistor	**Published Article and Nature of work**	**Gate length**	**Key findings**
DMG SOIJLT	**Wagaj and Patil (2019) (simulation-based work)**	**20 nm**	• **f_T, A_V and static power dissipation better in DMG SOIJLT.** • **CMOS circuits with DMG SOIJLT outperformed circuits with DMG SOIMOSFET.**
DMG DGJLT	**Chebaki *et al.* (2016) (simulation-model work)**	**100 nm**	• **DMG DGMOSFET has higher I_d and improved FoMs as compared to DMG DGJLT.** • **Source/Drain heavily doped extensions reduces series resistance, improving I_d.**

Table 2.2: Summary of key literature on DMG in junctionless FETs (Continued).

Type of Transistor	Published Article and Nature of work	Gate length	Key findings
DMG CGAAJLT	**Lou *et al.* (2012)** **Pravin *et al.* (2016)** **(simulation-based work)**	**40 nm**	• **I_{ON}, DIBL and g_m better with DMG architecture.** • **f_T and f_{MAX} higher in DMG than SMG.** • **Best performance with L_{M1} : L_{M2} of 1:1 and workfunction difference of 0.5 eV.** • **SS superior for SMG JLT** • **Power dissipation lowered using DMG with high κ gate oxides.**
DMG JLFinFET	**Kusuma and Talari (2022)** **(simulation-based work)**	**14 nm**	• **High κ gate oxide improves $\frac{I_{ON}}{I_{OFF}}$, SS and DIBL.** • **Fine-tuning of gate work function reduces SCE.** • **Significant improvement in $\frac{I_{ON}}{I_{OFF}}$ observed with Si_3N_4-HfO_2 combination as gate oxide.**

2.6.2 Literature Survey on Junctionless Transistor with Spacers

In a junctionless transistor, the inclusion of spacers on both sides of the gate (source side and drain side) enhances the performance alongside suppressing SCE significantly. Several research works highlight the impact of using spacer technology in a JLT. It is observed that adding spacers made of materials, particularly with high dielectric constant (κ) improves electrostatic control of gate over the channel as well as suppresses SCE to a large extent in SOIJLT (Gundapaneni *et al.* (2011)). Incorporating high κ spacers in DGJLT improves analog performance metrics while there is a degradation in RF metrics like f_T and f_{MAX} due to an increase in gate capacitance (Baruah and Paily (2013*b*), Biswas *et al.* (2017)). In work by Kumari *et al.* (Kumari *et al.* (2015)), it is reported that along with dielectric constant, length of the spacer (L_{sp}) on both

sides of the gate also plays a crucial role in promoting DGJLT for both analog and digital applications. However, using a high κ gate dielectric with a narrow low κ spacer can pave the way for steep SS in DGJLT (Gupta and Kranti (2016)).

A detailed exploration of the influence of spacer material on the characteristics of GAAJLT was done by Yang *et al.* (Yang *et al.* (2018)). They conclude that with an increase in dielectric constant of spacer, I_{ON} and $\frac{I_{ON}}{I_{OFF}}$ increase, whereas SS and DIBL decrease for different L_g, source/drain extension length (L_{SD}) and nanowire directions. By selecting a high κ spacer, better suppression of fluctuations in transistor performance is achieved (Yang *et al.* (2018)). Adding asymmetric spacers (spacer length at the source side lesser than that at the drain side) in GAAJLT boosts transistor performance making them a suitable choice for low-power applications (Sreenivasulu and Narendar (2021*a*)).

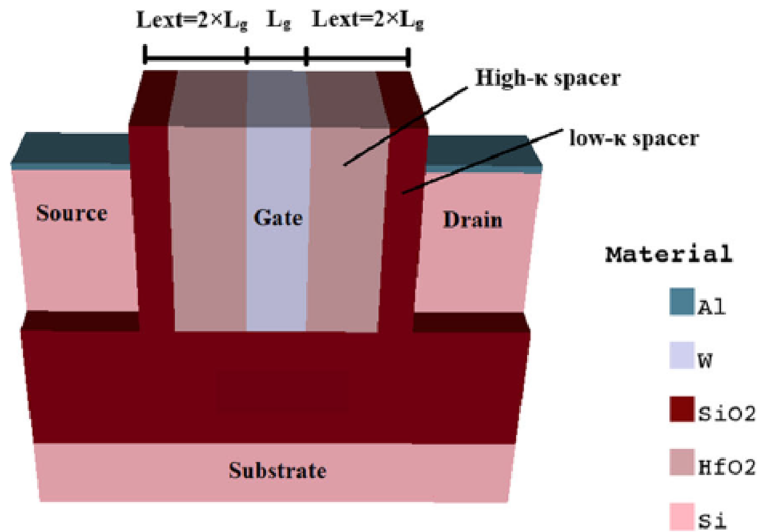


Figure 2.14: 3-D structure of Junctionless FinFET with dual κ spacer (Kaur *et al.* (2022)).

Another type of spacer technique widely researched in JLTs is dual κ spacer architecture. In most cases, high κ dielectric material will be placed near the gate and next to it another low κ spacer material will be placed as shown in Figure 2.14. It is observed that analog/RF FoMs of a trigate JLT with dual κ spacer only on the source side are less sensitive to the device parameters variations like gate oxide thickness (t_{ox}) and doping concentration (N_d) (Saini and Choudhary (2016)). It is also reported that

the placement of dual κ spacers and their proportion has a significant impact on device characteristics of a JLFinFET (Kaur *et al.* (2022)). As the proportion of spacer with high κ increases, $\frac{I_{ON}}{I_{OFF}}$ and A_V increase and DIBL decrease. Scaling down to channel length of 3 nm and 1 nm, still gave a reasonably good $\frac{I_{ON}}{I_{OFF}}$ of around 10^9 in a JLFinFET with silicon channel adopting dual κ spacer technology (Sreenivasulu and Narendar (2021*b*)). Quantum confinement in such lower dimensions aids in reducing I_{OFF} by a large amount. However, during the fabrication process, while depositing the spacer on both sides of the gate, realizing steep sidewalls (side wall angle = 90°) is a challenging task. In this context, a detailed examination is done on the effectiveness of high κ spacers in suppressing variations in transistor characteristics caused by non-ideal sidewall angles (Lou *et al.* (2014)). In the work by Bousari *et al.* (Bousari *et al.* (2019*a*)), a close inspection is done on the influence of high κ spacers on the behaviour of JLFinFET. A successful reduction of leakage current, enhancement of $\frac{I_{ON}}{I_{OFF}}$ and improvement in SCE is observed by adding high κ spacers like HfO_2 in a JLFinFET. Table 2.3 summarises key literature regarding junctionless transistors with spacers.

Table 2.3: Summary of key literature on junctionless FETs with spacers.

Type of Transistor	**Published article and Nature of work**	**Gate length**	**Key findings**
SOIJLT with high κ spacer	**Gundapaneni *et al.* (2011) (simulation-based study)**	**20 nm**	• **High κ spacer results in increase in effective L_g in OFF state.** • **I_{OFF} reduced significantly with high κ spacer.** • **SS and DIBL improve with high κ spacers.**
DGJLT with spacer	***Baruah and Paily (2013*b*) **Kumari *et al.* (2015) ***Roy and Biswas (2017) ++Gupta and Kranti (2016) (simulation-based works)**	***20 nm, **32 nm, ***30 nm ++50 nm**	• **g_m, A_V and TGF increases with κ of spacer.** • **I_{ON} decrease with increasing spacer width.** • **f_T and f_{MAX} degrade as κ of spacer increases.**

Table 2.3: Summary of key literature on junctionless FETs with spacers. (Continued).

Type of Transistor	Published article and Nature of work	Gate length	Key findings
			• TGF less sensitive to variation in κ of spacer. • JLTs with spacers outperform IM MOSFETs in terms of voltage gain, f_T and f_{MAX}. • Steep SS achieved in DGJLT devices having high κ gate dielectric and narrow low κ sidewall spacer.
GAAJLT with high κ spacer	[+]Yang *et al.* (2018) [2]Sreenivasulu and Narendar (2021*a*) (simulation-based works)	[+]5 nm [2]10 nm	• I_{ON}, $\frac{I_{ON}}{I_{OFF}}$, SS, DIBL better with high κ spacers. • Spacers ($\kappa > 12$ can) better for suppressing fluctuations by device parameters. • With more channel-drain distance, influence of V_{DS} is reduced over channel with asymmetric spacer, minimizing SCE.
JLFinFET with dual κ spacer	[x]Saini and Choudhary (2016) [xx]Kaur *et al.* (2022) [a]Sreenivasulu and Narendar (2022) (simulation-based works)	[x]20 nm [xx]15 nm [a]3 nm	• With dual κ spacer minimum SCE and I_{ON}, $\frac{I_{ON}}{I_{OFF}}$, SS, TGF and A_V is better. • As proportion of high κ spacer increases, $\frac{I_{ON}}{I_{OFF}}$, A_V increase, DIBL decrease. • Dual κ spacer reduces parasitic capacitances.
JLFinFET with high κ spacer	Lou *et al.* (2014) Bousari *et al.* (2019*a*) (simultion-based works)	10 nm	• High κ spacer lowers sub-threshold characteristics variation due to changing sidewall angle.

Table 2.3: Summary of key literature on junctionless FETs with spacers. (Continued).

Type of Transistor	Published article and Nature of work	Gate length	Key findings
			• **Optimised performance when $L_{sp} = \frac{L_{SD}}{2}$.** • **High κ spacer in JLFinFET gives better I_{OFF}, I_{ON}, $\frac{I_{ON}}{I_{OFF}}$, SS and DIBL.**

2.6.3 Literature Survey on DMG Junctionless Transistor with Spacers

Examining literature about junctionless transistors with spacers as well as Dual Material Gate architecture in junctionless transistors separately, it is evident that these two techniques significantly improve the electrical nature and at the same time, reduce SCE thereby ensuring down-scaling to sub-10 nm regime. Hence, by combining the above two techniques, junctionless transistors are expected to have superior characteristics and high immunity to SCE. Navigating across multiple research works about junctionless transistors, a few articles were obtained that handle junctionless transistors with Dual Material Gate incorporating spacer technology. Table 2.4 puts forth key findings from literature discussing DMG junctionless transistors with spacers. Baruah and Paily (Baruah and Paily (2013*a*)) gave a detailed picture of the effectiveness of adding spacers in a DMG DGJLT, especially in terms of analog Figures of Merit (FoM). A comparative analysis is done among SMG DGJLT, DMG DGJLT and DMG DGJLT with spacer structures and found that DMG DGJLT with high κ spacers outperforms the other two structures. Similar work by Amin and Sarin, report the improvements observed with the inclusion of high κ spacers in a DMG DGJLT (Amin and Sarin (2016)). Characteristics of DMG DGJLT were analysed varying properties of spacer materials as well as gate length ratio in the DMG. A recent study showcases the nature of DMG DGJLT with spacer as well as hetero gate dielectric and checks its suitability for analog as well as digital applications (Bashir *et al.* (2022)). It is claimed that DMG DGJLT with high κ spacers having hetero gate dielectric is a promising candidate for low technology nodes. However, much research has not been

done on using DMG architecture with spacer technology on multi-gate transistors like FinFETs in the junctionless regime. As the semiconductor industries have switched to FinFET technology, it is imperative to investigate the performance of JLFinFET having DMG architecture with suitable spacers.

Table 2.4: Summary of literature on DMG junctionless FETs with spacer technology.

Type of transistor	**Published article and Nature of work**	**Gate length**	**Key findings**
DMG DGJLT with spacers	**Baruah and Paily (2013*a*) (simulation-based study)**	**40 nm**	• **High κ spacers give better gm, V_{EA} and A_V than DMG DGJLT without spacer as well as SMG DGJLT.** • **SS improved with high κ spacers.** • **TGF in sub-threshold region lower in DMG structure.** • **f_T lower in DMG structure with high κ spacer.**
Dopingless DMG DGJLT with high κ spacer	**Amin and Sarin (2016) (simulation-based study)**	**15 nm**	• **Dopingless DMG DGJLT with high κ space shows superior I_{ON}, g_m, V_{EA} and A_V.**
DMG DGJLT with dual κ gate oxide and high κ spacer	**Bashir *et al.* (2022) (simulation-based study)**	**20 nm**	• **High κ gate sidewall spacer in DMG DGJLT having dual κ gate oxide gives significant improvements in analog and digital FoMs.**

2.7 Theoretical Modeling of Junctionless Transistors

To understand the electrostatic nature of transistor, researchers examine them through (i) Technology Computer Aided Design (TCAD) simulations, (ii) mathematical modeling and (iii) experimental characterisation, before launching them in market. Simulation process involves dissecting a transistor using a fine mesh having lakhs of nodes and computing potential at these nodes with Poisson's equation employing multiple iterative methods. Hence this approach is cumbersome and time-consuming and cannot be used to study behaviour of electronic circuits having large number of transis-

tors. Experimental characterisation requires semiconductor fab and involves multiple fabrication process that are again time consuming and costly. Hence device world rely heavily on mathematically modeling a transistor taking into account physics involved. Accurate mathematical models derived gives insight into the performance of a transistor under different conditions. Circuit simulators use mathematical models that are both robust and computationally efficient to assess the performance of multi-transistor circuits and optimize them prior to soldering them into ICs. Various modeling approaches have been adopted by researchers worldwide to describe the electrical behaviour of junctionless transistors like analytical modeling, compact modeling and atomistic modeling. Nonetheless, the analytical modeling is the modeling approach adopted to model junctionless transistor in this work.

In the analytical modeling approach, Poisson's equation is solved using the boundary conditions and certain valid approximations to obtain the channel potential model. It may be noted that solving the 2-D Poisson's equation is sufficient for planar devices like SOIJLT whereas a solution in all 3 coordinates (x,y,z) becomes necessary for non-planar devices like FinFET, especially for lower channel dimensions (sub-20 nm). Although approximations like Gradual Channel Approximation (GCA), depletion approximation etc simplify the solution to a large extent, considering the present-day channel dimensions, many approximations become invalid. Hence modeling these miniature transistors becomes a tough task. Since the invention of the junctionless transistor, many articles have been published that put forth mathematical models for threshold voltage, drain current, sub-threshold swing etc. In the upcoming subsection, an overview of various threshold voltage model literature available for junctionless transistors is presented.

2.7.1 Threshold Voltage Model for Junctionless Transistors

To model the threshold voltage, the initial step is to obtain the expression for potential in the channel of JLT by solving Poisson's equation. To solve Poisson's equation, suitable boundary conditions, assumptions and approximations are considered. It may be noted that for short channel multi-gate present-day transistors, it is necessary to solve 3-D Poisson's equation. The solution for 3-D Poisson's equation gives the expression for channel potential in terms of x, y and z coordinates. Then closed form of expression for threshold voltage is obtained by applying the threshold voltage condition, at specific locations in the channel (Hu *et al.* (2014), Manikandan and Balamurugan

(2021)). It must be noted that similar to the case of conventional transistors, GCA fails for JLT when channel length becomes comparable with its thickness. Challenges while modeling threshold voltage of junctionless transistors are:-

- As the conduction happens mostly in the bulk, expression for channel potential in the bulk has to be solved for deriving the expression for threshold voltage.
- For modeling threshold voltage of transistor with sub-50 nm channel dimensions, entire channel potential model is required. This is unlike the case of conventional transistor where only surface potential model is needed for obtaining threshold voltage expression.
- As the conduction mechanism is different from conventional transistors, threshold voltage condition is not taken as twice Fermi potential.
- The condition for threshold in junctionless transistor considers the point in channel that gets undepleted last (minimum potential point in x direction), paving the way for current flow, as transistor traverses from OFF state to ON state.

In 2012, Gnani *et al.* (Gnani *et al.* (2012)) developed an analytical model for the threshold voltage of SOIJLT. Influence of substrate doping (N_{sub}) as well as buried oxide thickness (t_{box}) on threshold voltage was analysed and it is observed that V_{th} increases with a decrease in t_{box} and an increase in N_{sub}. Analytical potential-based models for the threshold voltage of short channel junctionless DGJLTs were developed Chiang (2012), Jiang *et al.* (2015), Holtij *et al.* (2013). In the work by Chiang *et al.* (Chiang (2012)), the V_{th} model developed for DGJLT can be extended to junction-based counterparts as well. This article has concluded that for gate lengths varying from 10 nm to 40 nm, JL devices exhibit better performance than IM devices in terms of SS, DIBL, V_{th} roll-off etc. A series-based analytical expression for the threshold voltage of DGJLT that shows a good match with simulation results, was derived by Jiang *et al.* (Jiang *et al.* (2015)). A conformal mapping technique was applied to determine the channel potential in a DGJLT Holtij *et al.* (2013). It is observed that with increasing N_d, there is decrease in V_{th}. With decrease in L_g, the channel becomes more affected by DIBL. In the practical scenario, the fabrication process involving ion-implantation would result in non-uniformly doped channels (mostly Gaussian doped). Hence some articles explore the physics of JLTs with Gaussian doping. In the work by Singh *et al.* (Singh *et al.* (2016)), the 2-D Poisson's equation is solved and the V_{th}

model is derived for DGJLT with Gaussian profile in the active region. For effective suppression of DIBL and other SCE, the straggle parameter and peak concentration of the Gaussian doping profile also have a profound effect. An explicit expression is developed for V_{th} of CGAAJLT and the dependence of V_{th} on silicon body radius, N_d, t_{ox} and L_g is analysed (Hu *et al.* (2014)). Hu *et al.* also proposed a new method to extract threshold voltage namely, the 'ϕ_{min}' method, which is employed in this thesis.

As JLFinFET is a promising candidate for current market requirements, there is a huge demand for mathematical models that replicate their electrical characteristics. Hence, various research teams model their behaviour through different approaches. Extensive survey was done to study various threshold voltage models of JLFinFET to bring out an effective model that could be extended for DMG JLFinFET as well. Threshold voltage model for a long channel trigate JLT, that takes into account quantum confinement and incorporates influence of temperature was developed by Trevisoli *et al.* (Trevisoli *et al.* (2011)). This model analyses the influence of various device parameters on V_{th} and very well matches both simulation as well as experimental results. In another work by Trevisoli *et al.* (Trevisoli *et al.* (2013)), V_{th} model was developed for the long channel ($L_g = 1$ μm) SOI JLFinFET. In this work, a new V_{th} extraction method is proposed. V_{th} is considered as V_{GS} when $\frac{g_m}{I_d}$ drops to half of its maximum value. The V_{th} model is validated with experimental as well as simulated results for various device parameters. Both the articles by Trevisoli team (Trevisoli *et al.* (2011),Trevisoli *et al.* (2013)) model V_{th} for 1 μm long channel JLFinFET which is nowadays obsolete. A potential model for narrow and tall SOI JLFinFET ($L_g = 200$ nm) where the channel is completely controlled by lateral gates is obtained by solving 2-D Poisson's equation (Liu *et al.* (2016)). The model developed for channel potential matches with simulated data in depletion mode of operation. V_{th} model derived was used to analyse influence of V_{BS} on V_{th}. Nonetheless, there is a discrepancy between modeled results and simulated results for channel lengths as large as 200 nm. So the model might be highly inaccurate for present-day dimensions. Another study conducted on SOI JLFinFET has provided an analytical model for channel potential as well as threshold voltage with channel lengths ranging from 10 nm to 60 nm (Hu *et al.* (2016)). In this work, using suitable approximations and boundary conditions, 3-D Poisson's equation is directly solved by incorporating the Fourier series. The threshold voltage model was then derived and its capability in predicting simulation results was examined for various channel lengths. Although they put forth an appealing modeling

approach, the mismatch between modeled and simulated data was significantly large for dimensions lower than 25 nm. Table 2.5 summarises the key literature about the threshold voltage model of junctionless transistors.

Table 2.5: Summary of literature with threshold voltage model in junctionless transistors.

Type of transistor	Published article and and Nature of work	Gate length	Key findings
SOIJLT	Gnani *et al.* (2012) (simulation-model work)	200 nm	• Potential and V_{th} model developed for SOIJLT. • Dependence of V_{th} on V_{BS} and t_{box} is analysed.
DGJLT	Chiang (2012) (simulation-model work)	10 nm to 40 nm	• V_{th} model developed for short channel DGJLT. • V_{th} model extendable for IM devices as well. • Better performance by junctionless device than IM device in reducing V_{th} roll-off, DIBL, SS.
	Holtij *et al.* (2013) (simulation-model work)	22 nm to 100 nm	• 2-D analytical model for potential for DGJLT is developed. • V_{th} model developed for DGJLT. • V_{th} model predicts the simulated value for $10^{18} \leq N_d \leq 5{\times}10^{19}$.
	Jiang *et al.* (2015) (simulation-model work)	10 nm to 60 nm	• Potential and V_{th} model developed for DGJLT. • Series expansion used to solve Poisson's equation. • Model and TCAD results match well.
Gaussian doped DGJLT	Singh *et al.* (2016) (simulation-model work)	20 nm to 100 nm	• Model for potential and V_{th} developed.

Table 2.5: Summary of literature with threshold voltage model in junctionless transistors (Continued).

Type of transistor	Published article and Nature of work	Gate length	Key findings
			• V_{th} reduced with decrease in L_g and N_{peak} of Gaussian profile. • V_{th} decrease with increase in V_{DS}, channel thickness, t_{ox} and Gaussian profile straggle parameter.
CGAAJLT	Hu *et al.* (2014) (simulation-model work)	10 nm to 60 nm	• 2-D potential model developed for CGAA JLT. • V_{th} model match with simulation results for $L_g > 25$.
trigate JLT	Trevisoli *et al.* (2011) (simulation-model-experimental work)	1 μm	• V_{th} model developed and validated with experimental results. • Quantum confinement and corner effects considered. • Infuence of temperature on V_{th} analysed.
SOI JLFinFET	Trevisoli *et al.* (2013) (simulation-model-experimental work)	1μm	• New V_{th} extraction method obtained from $\frac{g_m}{I_D}$ graph. • V_{th} model derived. • V_{th} model valid for different T_{fin}-H_{fin} pairs, N_d and t_{ox} values.
	Liu *et al.* (2016) (simulation-model work)	200 nm	• 2-D potential model between lateral gates in SOI JLFinFET developed in sub-threshold region. • V_{th} model developed.

Table 2.5: Summary of literature with threshold voltage model in junctionless transistors (Continued).

Type of transistor	Published article and Nature of work	Gate length	Key findings
SOI JLFinFET	**Hu *et al.* (2016) (simulation-model work)**	**10 nm to 60 nm**	**• 3-D potential model developed for channel of SOI JLFinFET. • V_{th} model shows match with slight margin of error for 20 nm $\leq L_g \leq$ 60 nm.**

2.7.1.1 Threshold Voltage Models for DMG Junctionless Transistors

As explained in section 2.4.3, owing to the benefits of using a DMG architecture in junctionless transistors, a survey was done on the published literature that deals with mathematical modeling of V_{th} in junctionless transistors with DMG. Although several articles were available handling threshold voltage modeling of junctionless transistors, not many works were published that put forth mathematical models for V_{th} for DMG junctionless transistors. As the DMG gate comprises two gate materials with different work functions placed side by side, while solving Poisson's equation, two extra boundary conditions are considered along with the usual set of boundary conditions that appear while modeling a single material gate structure. These extra boundary conditions are:- (a) channel potential is continous at the interface of dissimilar gate metals (b) Electric flux is continuous at the interface of both gate materials. Hence potential model expression for the channel region beneath each gate material is developed separately. Once the potential model is developed, the minimum channel potential point is located for the region under gate material with higher work function (as gate material with higher work function has more control over the channel). Then incorporating the threshold voltage condition, an analytical model for V_{th} is developed.

Almost all the works available in the literature associated with analytical modeling of V_{th} of a DMG structure in the junctionless regime, focus on either DGJLT or CGAAJLT. There is inherent easiness in solving the Poisson's equation for symmetric structures. A potential model for DMG DGJLT under various regions of operation (full depletion, partial depletion, near flat band) was developed and the V_{th} model was derived (Agrawal *et al.* (2015)). V_{th} dependence on t_{ox}, t_{si} and N_d was studied and the

model derived by Agrawal *et al.*, matched with the simulation results. A similar work was published which explored the analytical modeling aspects of DMG DGJLT which has a dual-doped channel (Awasthi *et al.* (2022)). Excellent match was obtained between model and simulation results for L_g as low as 20 nm. 2-D Poisson's equation in cylindrical coordinates is solved to obtain channel potential model in CGAAJLT and applying threshold voltage condition, V_{th} model is derived (Li *et al.* (2013), Biswal *et al.* (2015)). In both these articles, the V_{th} model is validated for different L_g. A temperature-dependent V_{th} model for CGAAJLT was developed which takes into account the effect due to localized charges that are created due to damages occurring while fabrication like hot electron stress, process damage and radiation-induced damage (Pratap *et al.* (2015*a*)). In their work, it is visible that V_{th} in DMG CGAAJLT is less immune to localized charges than the SMG structure. Another work about analytical modeling of CGAAJLT, used finite differentiation method to model potential in the channel (Preethi and Balamurugan (2021)). They have decomposed 2-D Poisson's equation to two 1-D equations and obtained potential model with a comparatively simpler solution. V_{th} model then derived was validated with simulation results for different L_g, t_{si} and t_{ox}. A list of literature available for analytical modeling in DMG JLTs along with key findings is given in Table 2.6. As DMG JLFinFET can be a probable candidate for the semiconductor industry due to its superior characteristics and high immunity to SCE, it is necessary to model its electrical characteristics like drain current, threshold voltage, SS etc.

Table 2.6: Summary of literature on threshold voltage modeling in Dual Material Gate junctionless transistors.

Type of transistor	**Published article and Nature of work**	**Gate length**	**Key findings**
DMG DGJLT	**Agrawal *et al.* (2015)** **(simulation-model work)**	**100 nm**	• **V_{th} model developed.** • **Effect of t_{si}, t_{ox}, N_d on V_{th} explored.**
	Awasthi *et al.* (2022) **(simulation-model work)**	**20 nm to 40 nm**	• **Centre channel potential and V_{th} model developed.**

Table 2.6: Summary of literature with threshold voltage model in junctionless transistors (Continued).

Type of transistor	Published article and Nature of work	Gate length	Key findings
CGAAJLT	Li *et al.* (2013) (simulation-model work)	20 nm to 80 nm	• Model for channel potential and V_{th} developed. • Better suppression of SCE by DMG devices compared to SMG.
	Biswal *et al.* (2015) (simulation-model work)	20 nm to 100 nm	• Potential and V_{th} model developed. • Effective conduction path considered while modeling. • DMG devices superior compared to SMG devices.
	Pratap *et al.* (2015*b*) (simulation-model work)	20 nm	• Temperature dependent V_{th} model with localized charges developed. • Effect of localized charges reduces at higher temperatures.
	Preethi and Balamurugan (2021) (simulation-model work)	10 nm to 50 nm	• Potential, V_{th} modeled using finite differentiation. • V_{th} model developed matched TCAD results for various film thickness and t_{ox}.

2.8 Summary

In this chapter, a review of the various techniques to enhance the characteristics of junctionless transistors is presented. Suppression of SCE as well as enhancement in

current characteristics by incorporating DMG as well as spacer engineering in JLT is explored through published literature. It is observed that with a suitable combination of gate materials and with appropriate spacers, significant enhancement is observed in characteristics of SOIJLT, DGJLT and CGAAJLT. However, to the best of our knowledge, a study that elaborates on the impact of properties of metals in a DMG structure on the electrical behaviour of JLFinFETs is not available. Effectiveness of spacers in enhancing the performance of DMG JLFinFETs is also less explored. With the motive of deriving a closed form of expression for channel potential and threshold voltage of junctionless FinFET, analytical models available in the literature pertaining to junctionless transistors were reviewed. An in-depth study was done on various threshold voltage modeling techniques employed in various types of junctionless transistors. Threshold voltage models on DMG junctionless structures were also reviewed. It was observed that many published works about DMG focus on modeling potential and threshold voltage for symmetric structures like DGJLT and CGAAJLT. As the market switched to FinFET technology, it is necessary to bring forth models for JLFinFET. However, owing to the complexity of solving 3-D Poisson's equation in asymmetric structures like JLFinFETs, few literature were found related to them. Nevertheless, to the best of our knowledge, no literature was available discussing potential and V_{th} models of JLFinFET with DMG. Hence considering better immunity to SCE, it becomes imperative to analyse DMG JLFinFET and mathematically model its parameters.

Chapter 3

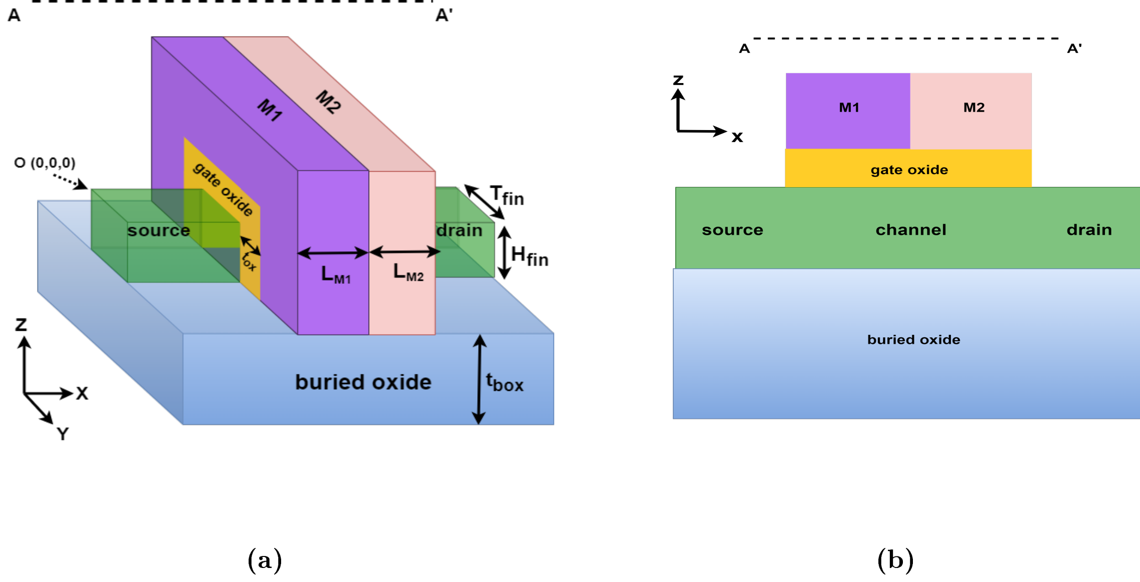
DUAL MATERIAL GATE JUNCTIONLESS FINFET- A COMPREHENSIVE STUDY

3.1 Introduction

In this chapter, an elaborate analysis of the electrical behaviour as well as short channel effects of DMG JLFinFETs with different gate metal pairs and varying gate metal length ratios is presented. It is observed in Chapter 2 that junctionless transistors with DMG architecture display superior characteristics and provide better immunity to SCE (Long *et al.* (1999)). The gate material closer to the source, namely M1, has a dominating influence on transistor performance than the gate material closer to the drain (named M2) in DMG structures. Studies are carried out on a DMG-JLFinFET which combines the merits of junctionless transistor and DMG architecture on FinFET. The effect of metal gate work function variation and metal gate length ratio, on transfer characteristics, threshold voltage, DIBL and SS are discussed in detail.

Section 3.2 gives the structural details of DMG JLFinFET with insights into the simulation framework used. Section 3.3 discusses various simulation results highlighting the effect of work function and length ratio of gate materials on the characteristics as well as SCE in a DMG JLFinFET. This is followed by section 3.4 which summarises the work presented in this chapter.

3.2 Structure of DMG JLFinFET and Simulation Framework



(a) (b)

Figure 3.1: (a) 3-D structure of DMG JLFinFET and (b) 2-D cross-sectional view of DMG JLFinFET

Figure 3.1 shows a 3-D structure and 2-D cross-sectional view of DMG JLFinFET along the cutline A-A'. It shall be noted that analysis in this chapter is done on the behaviour of n-type DMG JLFinFET. The dimensions of DMG JLFinFET listed in Table 3.1 are conforming to current International Roadmap for Devices and Systems (IRDS) requirement (Hoefflinger (2020)). To accurately predict the performance of DMG JLFinFET, a 3-D device simulator named ATLAS by Silvaco, Inc. is used (Manual (2016*a*)). As the gate length of the transistor under study is 10 nm, quantum effects couldn't be neglected. Thus Quantum Mechanical Drift Diffusion Mode Space model along with field-dependent mobility model, generation-recombination model and band-to-band tunneling model, are used in the simulation. Various metals considered for M1 and M2 are listed in Table 3.2.

Figure 3.2 shows that the simulation results from Lee *et al.* (2016) were reproduced by the calibrated simulation setup used in this work. The authors of Lee *et al.* (2016) had patented the fabrication method of Junctionless Field Effect Transistor Cho and Kim (US Patent 10068971, Sep. 2018).

Table 3.1: Parameter specifications of Dual Material Gate Junctionless FinFET

Parameter	Value
Total gate length (L_g)	10 nm
Fin height (H_{fin})	5 nm
Fin thickness (T_{fin})	5 nm
Gate oxide thickness (t_{ox})	3 nm
Gate metal 1 length (L_{M1})	5 nm
Gate metal 2 length (L_{M2})	5 nm
Buried oxide thickness (t_{box})	10 nm
Gate oxide material	HfO_2
Buried oxide material	SiO_2
Channel doping concentration (N_d)	10^{18} cm^{-3}
Source/drain extension length (L_{ext})	9 nm

Table 3.2: Choice list of Gate Metals used along with their Work Functions

Metal	Work Function (eV)
Tantalum (Ta)	4.1
Aluminium (Al)	4.28
Titanium (Ti)	4.66
Nickel (Ni)	5.04
Gold (Au)	5.39
Platinum (Pt)	5.65

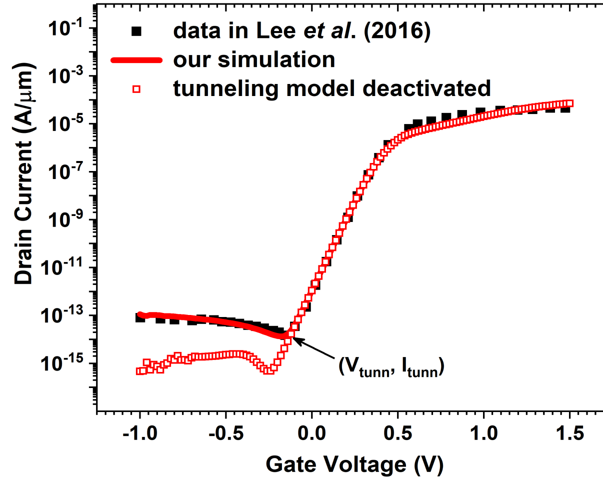


Figure 3.2: Comparison of transfer characteristics of JLFinFET from Lee *et al.* (2016) and calibrated simulation setup at $V_{DS} = 0.7$ V.

When the tunneling model is deactivated in the simulator, the drain current through the transistor in the OFF state is significantly lower, indicating that tunneling is a prominent phenomenon in the deep depletion region of junctionless transistors. Tunneling current (I_{tunn}) is defined as the current when lateral band-to-band tunneling becomes the dominant phenomenon causing current flow in a JLFinFET (indicated in Figure 3.2) when gate voltage (V_{GS}) sweeps in the negative direction. V_{GS} corresponding to I_{tunn} is denoted as V_{tunn}. In Figure 3.2, I_{tunn} is 1.32x10^{-14} A/μm and V_{tunn} is -0.18 V. The calibrated simulation setup also reproduced the transfer characteristics of a fabricated JLFinFET given in Barraud *et al.* (2012). This is shown in Figure 3.3.

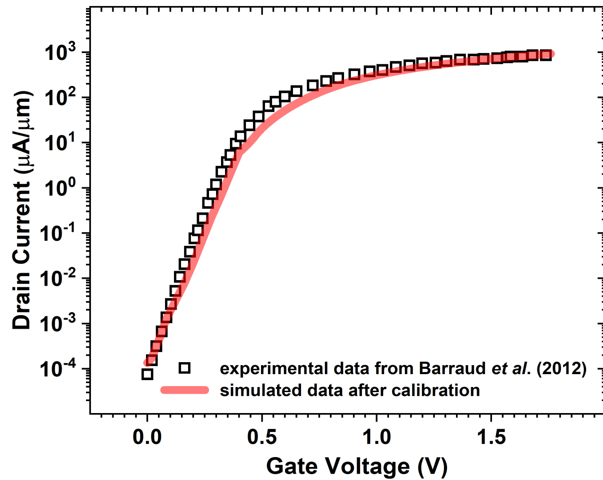


Figure 3.3: Calibration of simulation setup with data from Barraud *et al.* (2012)

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Fabrication of DMG JLFinFET can be done utilizing advanced techniques like Atomic Layer Deposition (ALD), Tilt Angle Evaporation (TAE) and metal wet etch process. TAE explained in Long *et al.* (1999) uses a single mask for DMG, where one metal is deposited in the region not falling under the shadow of photoresist. The second metal is deposited in the remaining region by normal evaporation method.

3.3 Simulation Results

This section demonstrates the effects of gate material engineering on the electrical characteristics as well as performance metrics of DMG JLFinFET. Gate material work

function difference and the ratio of the length of M1 to total gate length were varied to explore the effect on DC charactersitics as well as SCE in a DMG JLFinFET.

3.3.1 Influence of Work Function of both Gate Materials on DC Characteristics of DMG JLFinFET

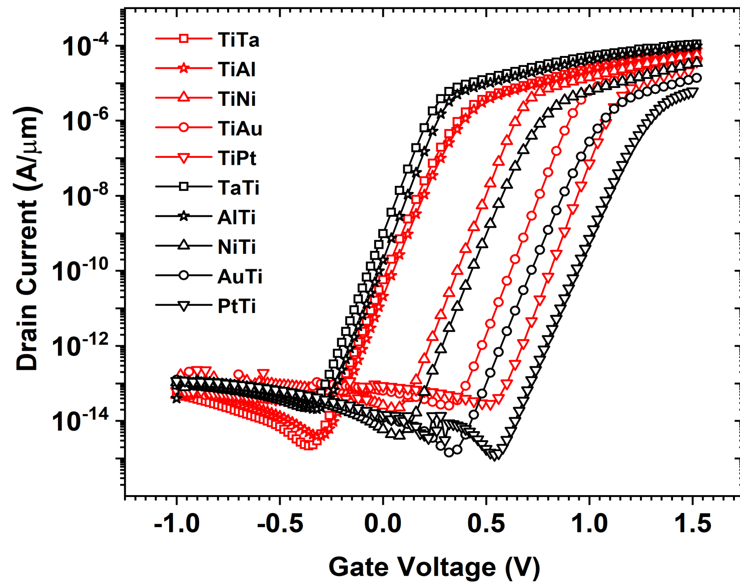


Figure 3.4: Transfer characteristics of DMG JLFinFETs with (i) Ti as M1 and other metals as M2 (red) and (ii) Ti as M2 and other metals as M1 (black), at $V_{DS} = 0.7$ V

The analysis carried out in this sub-section consider DMG JLFinFETs with Titanium as one of the gate materials (either M1 or M2). This is because, Titanium with work function of 4.66 eV lies at the middle of the range of work functions of all metals considered for analysis. Hence, observations are made under both situations where the work function of M1 (ϕ_{M1}) is greater as well as lower than the work function of M2 (ϕ_{M2}). For all the DMG JLFinFETs considered in this section, $\frac{L_{M1}}{L_g}$ is chosen to be 50%.

Figure 3.4 shows the transfer characteristics of two sets of DMG JLFinFETs. All the DMG JLFinFETs belonging to the first set have Titanium as M1 and one of the metals listed in Table 3.2 as M2 (red). The second set has Titanium as M2 and other metals as M1 (black). The well-known observation that, in a transistor, as the work

function of gate material (M1 or M2) is increased, there is shift in transfer characteristics towards positive V_{GS} direction. Hence threshold voltage (V_{GS}) increases. This is visible in Figure 3.5. The threshold voltage is taken as the gate voltage at which current through the transistor is $\frac{effective\ fin\ width}{total\ gate\ length} \times 10^{-7}$ A/μm (Rassekh and Fathipour (2020)). As seen in Figure 3.5, the shift in V_{th} is more pronounced (about 1.04 V) with variation in ϕ_{M1} from 4.1 eV (Ta) to 5.65 eV (Pt) as compared to variation in ϕ_{M2} by the same range (0.75 V). This is due to the dominance of M1 in keeping the channel depleted and thereby deciding the threshold voltage. V_{th} of SMG JLFinFET with Titanium gate (work function = 4.66 eV) is also added in Figure 3.5 for reference. Of all metals considered in Figure 3.5, only Ta and Al have a lower work function than Ti. As the threshold voltage primarily depends on the work function of M1, combinations of TaTi and AlTi result in transistors with lower threshold voltage than TiTa and TiAl combinations. This is the cause for comparatively lower threshold voltage only for combinations where Ta and Al constitute M1, for the case where M1 varies.

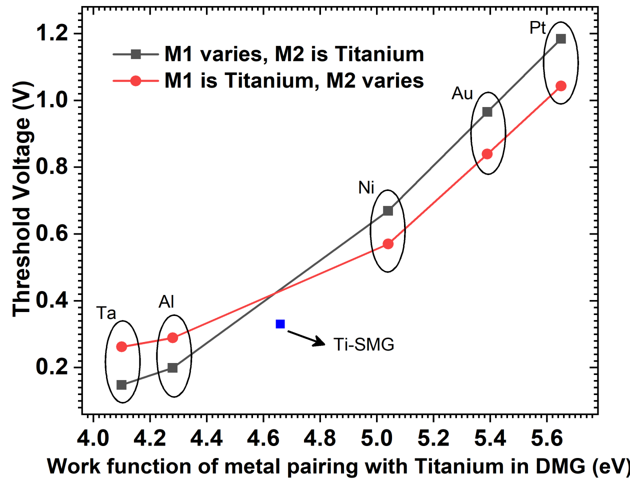


Figure 3.5: Threshold voltage of DMG JLFinFETs with (i) Ti as M1 and other metals as M2 (red) and (ii) Ti as M2 and other metals as M1 (black), at V_{DS} = 0.7 V

I_{tunn} explained in Section 3.2 should be considered while choosing gate materials for DMG in a Junctionless FinFET as it contributes to power dissipation in the OFF state. All the DMG gate pairs in Figure 3.4 are classified into two categories: $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$ and I_{tunn} for each of them is listed in Table 3.3. Figure 3.6 shows energy band diagram (conduction band-valence band versus position along x

direction) along a cutline, situated at the middle of the channel, at a distance of 2.5 nm from all three channel-gate oxide interfaces in DMG JLFinFETs with $\phi_{M1} > \phi_{M2}$ (blue) and $\phi_{M1} < \phi_{M2}$ (black). Figure 3.6 reveals that tunnel width at the channel-drain interface and potential barrier at the channel-source interface are the factors determining I_{tunn}. This is visible in Table 3.3 for the case of PtTi and AuTi both having more tunnel width as well as more potential barrier, which in turn results in reduced I_{tunn}. For TiPt and TiAu combination, comparatively narrower tunnel width and reduced potential barrier causes more I_{tunn} to flow during the OFF state of the transistor.

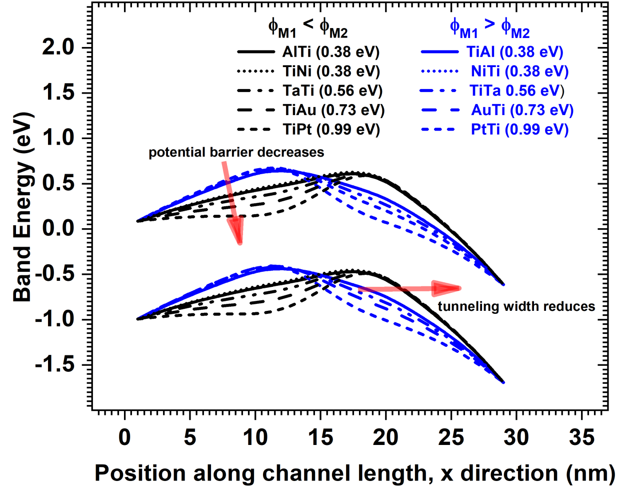


Figure 3.6: Energy band diagram along a cutline (x direction) located at the middle of channel in DMG JLFinFET with different gate metal pairs, at $V_{GS} = V_{tunn}$ and $V_{DS} =$ 0.7 V

Table 3.3: I_{tunn} for DMG JLFinFETs having gate material pairs with $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$

$\phi_{M1} < \phi_{M2}$	I_{tunn} (A/μm)	$\phi_{M1} > \phi_{M2}$	I_{tunn} (A/μm)
AlTi	2.07×10^{-14}	TiAl	3.96×10^{-15}
TiNi	2.19×10^{-14}	NiTi	4.02×10^{-15}
TaTi	2.29×10^{-14}	TiTa	2.17×10^{-15}
TiAu	2.58×10^{-14}	AuTi	1.44×10^{-15}
TiPt	2.87×10^{-14}	PtTi	1.26×10^{-15}

Key findings about I_{tunn} under all the cases of work functions of M1 and M2 and the cause for the same (referring to Figure 3.6 and Table 3.3) are listed in Table 3.4.

Table 3.4: List of observations on I_{tunn} of under situations, $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$ in DMG JLFinFET

Case	Observation	Reason	Case	Observation	Reason
$\phi_{M1} > \phi_{M2}$	I_{tunn} comparatively lower	large potential barrier, large tunnel width	$\phi_{M1} - \phi_{M2}$ increases	I_{tunn} reduces	tunnel width increases
			$\phi_{M1} - \phi_{M2}$ decreases	I_{tunn} increases	tunnel width reduces
$\phi_{M1} < \phi_{M2}$	I_{tunn} comparatively higher	small potential barrier, small tunnel width	$\phi_{M2} - \phi_{M1}$ increases	I_{tunn} increases	potential barrier reduces
			$\phi_{M2} - \phi_{M1}$ decreases	I_{tunn} reduces	potential barrier increases

3.3.2 Influence of Gate Material Length Ratio on DC Characteristics of DMG JLFinFET

In this sub-section impact of gate material length ratio ($\frac{L_{M1}}{L_g}$) on DC characteristics is explored. Rigorous simulations performed on various gate material combinations revealed that TiAl DMG JLFinFET is highly immune to SCE. Hence TiAl DMG combination was selected for analysis in this sub-section. As TiAl belongs to $\phi_{M1} > \phi_{M2}$ category, AlTi combination was also selected for analysis to investigate the influence of $\frac{L_{M1}}{L_g}$ on DMG JLFinFETs belonging to $\phi_{M1} < \phi_{M2}$ category.

Figure 3.7 shows transfer characteristics of a set of AlTi DMG JLFinFETs and TiAl DMG JLFinFETs where in each set, transistors differ from each other in the ratio of length of M1 to total gate length ($\frac{L_{M1}}{L_g}$). For all the simulations associated to variation in $\frac{L_{M1}}{L_g}$, L_g is fixed to 10 nm. For better visibility of current characteristics in the sub-threshold region, an enlarged version of characteristics is added as inset in Figure 3.7.

It is observed that when the gate material with a higher work function occupies the majority of the total gate length, there is an increase in threshold voltage due to stronger depletion of the channel. This fact is noticeable in Figure 3.7 and Figure 3.8. Threshold voltage increases by 0.17 V when the length of Ti increases from 20% to 80% of total gate length in TiAl DMG JLFinFET, while there is a decrease in threshold voltage by 0.23 V as the length of Al increases by the same amount in AlTi DMG JLFinFET. The shift in threshold voltage with $\frac{L_{M1}}{L_g}$ is lower in TiAl DMG JLFinFET ($\phi_{M1} > \phi_{M2}$). This is due to the location of gate material with higher work function (Ti in this case) being closer to source. Irrespective of variations in length of Ti, the lower work function material screens the channel region beneath Ti from drain

field. Hence the influence of V_{DS} in altering channel electrostatics with varying $\frac{L_{M1}}{L_g}$ becomes less. This in turn results in lower V_{th} variation. However for the case of AlTi DMG JLFinFET, Ti is located near the drain. So channel electrostatics beneath Ti will be heavily dependent on structural parameters. This results in more V_{th} variation for AlTi DMG JLFinFET with variation in $\frac{L_{M1}}{L_g}$.

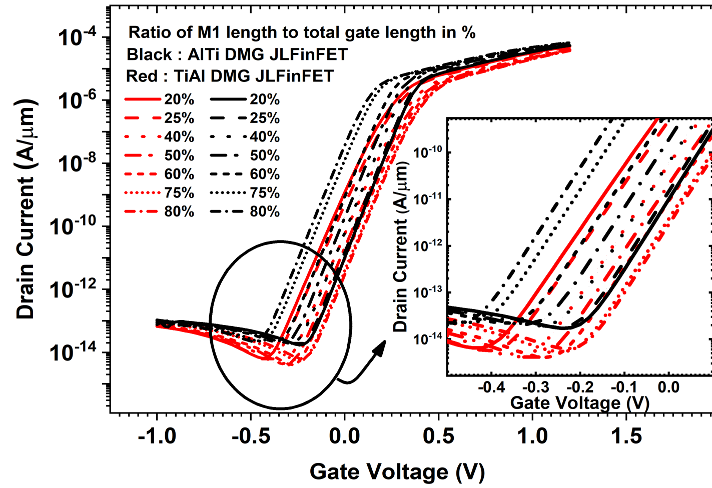


Figure 3.7: Transfer characteristics of TiAl DMG JLFinFET (red) and AlTi DMG JLFinFET (black) for varying $\frac{L_{M1}}{L_g}$ (expressed in %), at $V_{DS} = 0.7$ V

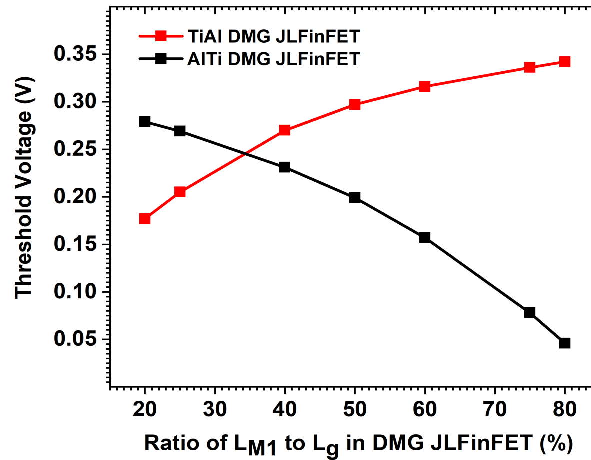


Figure 3.8: Threshold Voltage of TiAl DMG JLFinFET and AlTi DMG JLFinFET for varying $\frac{L_{M1}}{L_g}$ (expressed in %), at $V_{DS} = 0.7$ V

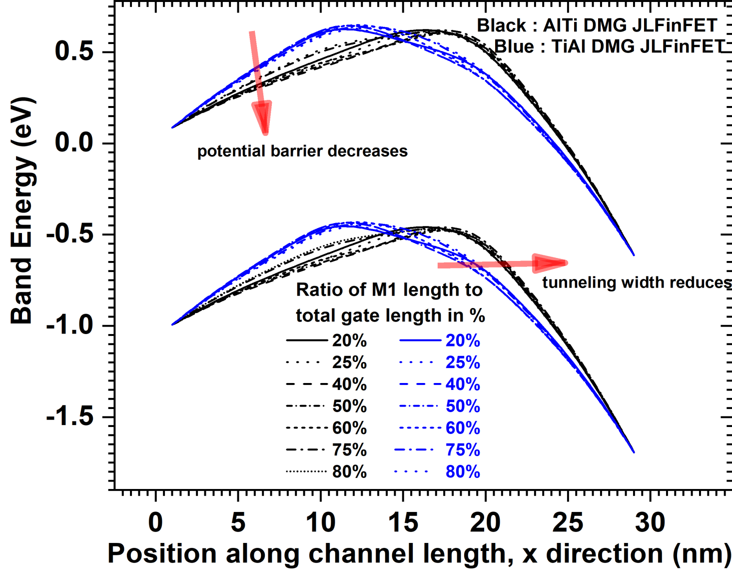


Figure 3.9: Energy band diagram along a cutline (x direction) at the middle of channel in AlTi DMG JLFinFET and TiAl DMG JLFinFET for varying $\frac{L_{\mathrm{M1}}}{L_g}$, at $\mathrm{V_{GS}} = \mathrm{V_{tunn}}$ and $\mathrm{V_{DS}} = 0.7$ V.

Table 3.5: $\mathrm{I_{tunn}}$ for DMG JLFinFETs having gate material pairs such that $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ and $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$

$\frac{L_{\mathrm{M1}}}{L_g}$ of AlTi (%)	$\mathrm{I_{tunn}}$ ($\frac{A}{\mu m}$)	$\frac{L_{\mathrm{M1}}}{L_g}$ of TiAl (%)	$\mathrm{I_{tunn}}$ ($\frac{A}{\mu m}$)
20	1.71×10^{-14}	20	6.6×10^{-15}
25	1.78×10^{-14}	25	5.67×10^{-15}
40	1.95×10^{-14}	40	4.21×10^{-15}
50	2.07×10^{-14}	50	3.96×10^{-15}
60	2.22×10^{-14}	60	4.05×10^{-15}
75	2.29×10^{-14}	75	5.34×10^{-15}
80	2.2×10^{-14}	80	6.32×10^{-15}

Figure 3.9 and Table 3.5 show that $\frac{L_{\mathrm{M1}}}{L_g}$ doesn't have a profound impact on $\mathrm{I_{tunn}}$ in TiAl DMG JLFinFET as well as AlTi DMG JLFinFET. However, $\mathrm{I_{tunn}}$ is least in TiAl DMG JLFinFET with $\frac{L_{\mathrm{M1}}}{L_g} = 50\%$. Potential barrier and tunnel width in AlTi DMG JLFinFETs and TiAl DMG JLFinFETs at $\mathrm{V_{GS}} = \mathrm{V_{tunn}}$ under varying $\frac{L_{\mathrm{M1}}}{L_g}$ is found out with the help of energy band diagram along a cutline (x direction) at the middle of channel as shown in Figure 3.9. It could be observed that reduced potential barrier

and decreased tunnel width cause an increase in I_{tunn} by one order of magnitude in AlTi devices compared to TiAl devices.

3.3.3 Short Channel Effects in DMG JLFinFETs

This sub-section handles an exclusive analysis on the influence of gate material work function difference ($\phi_{M1} \sim \phi_{M2}$) and gate material length ratio ($\frac{L_{M1}}{L_g}$) on SCE of DMG JLFinFET. $\phi_{M1} \sim \phi_{M2}$ refers to $\phi_{M1} - \phi_{M2}$, when $\phi_{M1} > \phi_{M2}$ and $\phi_{M2} - \phi_{M1}$, when $\phi_{M1} < \phi_{M2}$.

3.3.3.1 Impact of $\phi_{M1} \sim \phi_{M2}$ and $\frac{L_{M1}}{L_g}$ on DIBL and Sub-threshold Swing of DMG JLFinFET:

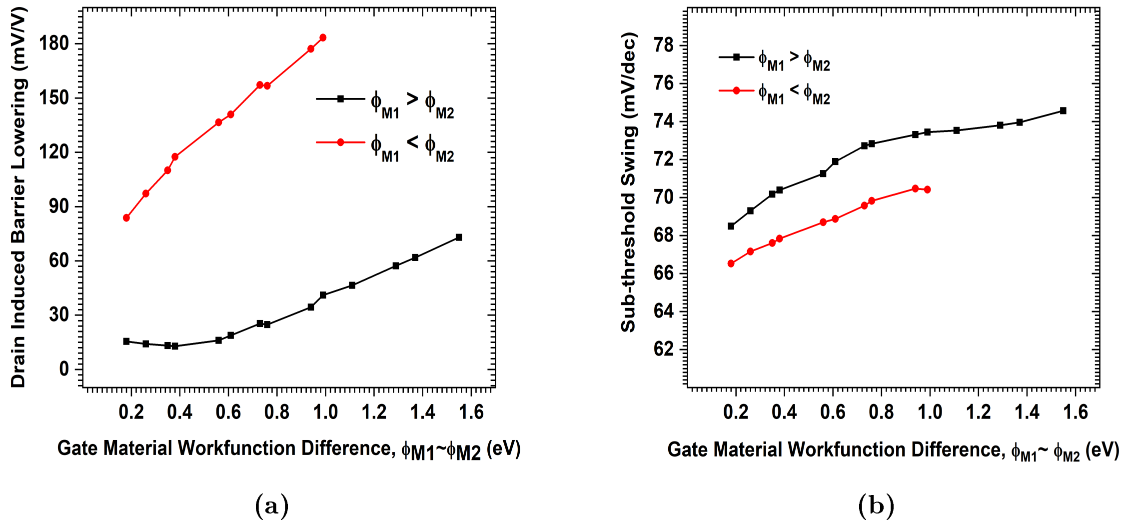


Figure 3.10: Variation in (a) DIBL and (b) SS with difference in the work function of M1 and M2.

It is observed that within a category (either $\phi_{M1} > \phi_{M2}$ or $\phi_{M1} < \phi_{M2}$), DIBL and SS depends on the difference in ϕ_{M1} and ϕ_{M2} and not on ϕ_{M1}, ϕ_{M2}. DMG JLFinFETs with Titanium-Aluminium gate and Nickel-Titanium gate both falling under same category ($\phi_{M1} > \phi_{M2}$) having same work function difference of 0.38 eV have same DIBL of 12.88 $\frac{mV}{V}$ and SS of 70.39 $\frac{mV}{decade}$. Hence to analyse SCE in DMG JLFinFET, DIBL and SS against difference in ϕ_{M1} and ϕ_{M2} is measured.

DIBL and SS variation against the difference in work function of M1 and M2 ($\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}}$) for DMG JLFinFETs with $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ and $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$ is shown in Figure 3.10. It is seen in Figure 3.10(a) that DIBL is much lower when $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ as compared to $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$. 12.88 $\frac{mV}{V}$ is the least DIBL obtained among all DMG combinations analysed. When $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$, the effect due to drain potential doesn't affect channel electrostatics under M1 significantly. This is due to M2 absorbing all the drain potential variations due to its proximity to the drain terminal. Hence V_{th} which is decided by the channel potential beneath M1 remains more immune to V_{DS} fluctuations. As a result, DIBL is considerably lower. When $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$, DIBL as well as rate of variation in DIBL with work function difference ($\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}}$) is more because the shift in drain bias could easily change the threshold voltage due to higher work function material (M2) being closer to the drain.

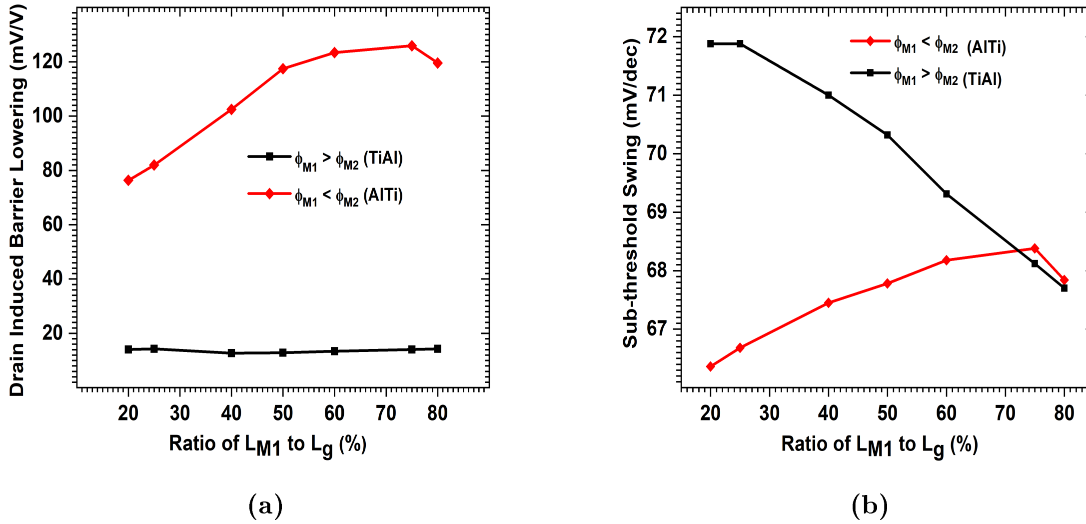


Figure 3.11: Variation in (a) DIBL and (b) SS with varying $\frac{L_{\mathrm{M1}}}{L_{\mathrm{g}}}$ keeping total gate length fixed to 10 nm

In Figure 3.10(b), SS is plotted against the difference in work functions for both cases: $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ and $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$. SS is lower (66.5 $\frac{mV}{decade}$ in the red curve as compared to the 68.4 $\frac{mV}{decade}$ in the black curve for the case of $\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}} = 0.18$ eV) for DMG JLFinFETs where $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$. This is because the channel under M2 is depleted of charge carriers due to the proximity to drain and higher work function of M2 when $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$. So when there is an increase in gate potential, DMG JLFinFETs (ϕ_{M1}

$< \phi_{M2}$) with depleted area only under M2, has a steeper rise in drain current with increase in gate potential. Hence better SS is observed for DMG JLFinFETs with $\phi_{M1} < \phi_{M2}$.

Figure 3.11 shows the variation in DIBL and SS for TiAl DMG JLFinFET and AlTi DMG JLFinFET, with varying $\frac{L_{M1}}{L_g}$ (Lg fixed to 10 nm). Figure 3.11(a) shows that when $\frac{L_{M1}}{L_g}$ increases, there is a marginal variation of DIBL in the case of TiAl DMG JLFinFET. As explained in Section 3.3.2 this is due to the location of gate material with higher work function being closer to the source. Irrespective of variations in $\frac{L_{M1}}{L_g}$, the lower work function material near the drain screens the channel region beneath Ti from the drain field. Hence V_{DS} fluctuations have a lower influence on channel electrostatics. This in turn results in lower V_{th} variation. Hence DIBL will be significantly low. However, for AlTi DMG JLFinFET, higher work function metal (Ti) constitutes M2, which is strongly influenced by the drain (due to its proximity to the drain). So channel electrostatics beneath Ti will be heavily dependent on structural parameters. This results in V_{DS} having more influence on V_{th}. Hence DIBL is more for AlTi DMG JLFinFET. For AlTi DMG JLFinFET, with increase in the length of M1 (Al), M2 confines to a smaller area (as Lg is constant), The channel region beneath M2 is also shrinks to a smaller area close to drain. Thus V_{DS} can alter the channel electrostatics easily thereby increasing DIBL up to the situation where M1 occupies 75% of the total gate length. However, when $\frac{L_{M1}}{L_g}$ is greater (for 80%, 90% etc), device becomes more of SMG structure and DIBL (which are comparatively higher for $\phi_{M1} < \phi_{M2}$) gets closer to that of SMG JLFinFET.

Examining Figure 3.11(b) reveals an interesting phenomenon that, when L_{M1} increases (and L_{M2} decreases as L_g is constant), there is improvement in SS for DMG combinations with $\phi_{M1} > \phi_{M2}$. SS degrades for $\phi_{M1} < \phi_{M2}$ as length of M1 increases. Hence, the inherent disadvantage of degradation in SS when $\phi_{M1} > \phi_{M2}$ as observed earlier could be eliminated if the length of M1 is more than 70% of total gate length in DMG JLFinFET.

3.3.3.2 Impact of $\phi_{M1} \sim \phi_{M2}$ and $\frac{L_{M1}}{L_g}$ of DMG, on Relative Change in Threshold Voltage of DMG JLFinFET

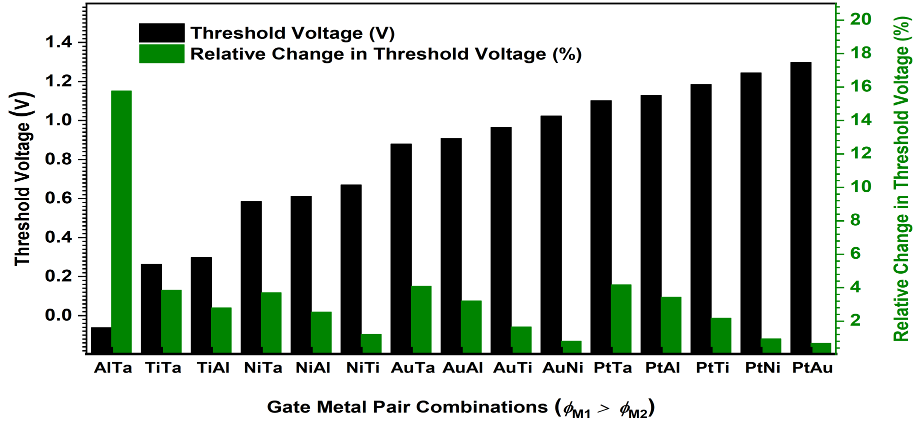
An important parameter to analyse the performance of DMG JLFinFET in short channel regime is relative threshold voltage change which is computed as $(\frac{V_{th}@V_{DS}=0.07V - V_{th}@V_{DS}=0.7V}{V_{th}@V_{DS}=0.7V} \times 100)$. This parameter is affected by the absolute value

of V_{th} at a particular drain bias unlike the case of DIBL which depends only on the difference in V_{th} at two different V_{DS}. Hence two transistors with the same DIBL can have different relative threshold voltage changes and the device with the least relative threshold voltage change is considered better as change in V_{DS} causes minimum % shift in V_{th}. To analyse the effect of gate material work function difference, on relative threshold voltage changes, all the possible DMG combinations of metals (listed in Table 3.2) are considered. These DMG combinations are classified into two categories: $\phi_{M1} > \phi_{M2}$, $\phi_{M1} < \phi_{M2}$ as shown in Table 3.6.

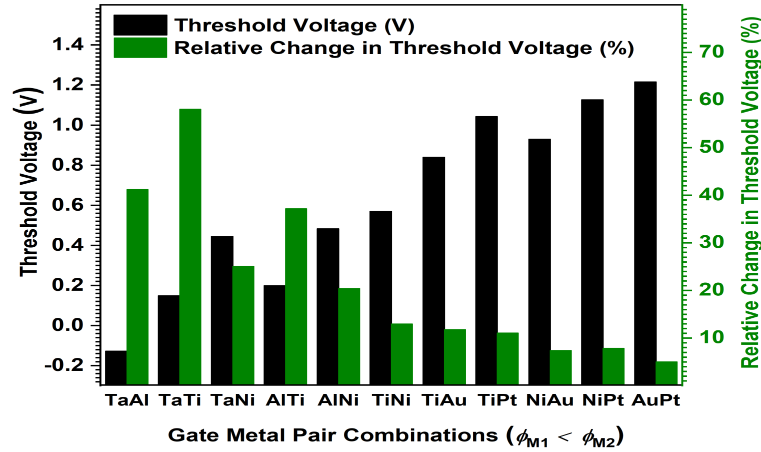
Table 3.6: List of combinations of gate metal pairs considered for DMG JLFinFET categorised based on ϕ_{M1} greater/lower than ϕ_{M2}, along with their corresponding work function difference.

$\phi_{M1} > \phi_{M2}$	$\phi_{M1} - \phi_{M2}$ (eV)	$\phi_{M1} < \phi_{M2}$	$\phi_{M2} - \phi_{M1}$ (eV)
AlTa	0.18	TaAl	0.18
PtAu	0.26	AuPt	0.26
AuNi	0.35	NiAu	0.35
NiTi	0.38	TiNi	0.38
TiAl	0.38	AlTi	0.38
TiTa	0.56	TaTi	0.56
PtNi	0.61	NiPt	0.61
AuTi	0.73	TiAu	0.73
NiAl	0.76	AlNi	0.76
NiTa	0.94	TaNi	0.94
PtTi	0.99	TiPt	0.99
AuAl	1.11	AlAu	1.11
AuTa	1.29	TaAu	1.29
PtAl	1.37	AlPt	1.37
PtTa	1.55	TaPt	1.55

Figure 3.12 presents V_{th} at drain bias of 0.7 V and the relative change in V_{th} (expressed in %) for a shift in V_{DS} from 0.7 V to 0.07 V, for DMG JLFinFETs belonging to $\phi_{M1} > \phi_{M2}$ and $\phi_{M1} < \phi_{M2}$ category. It may be noted that for the case where $\phi_{M1} < \phi_{M2}$, gate pairs with $\phi_{M1} - \phi_{M2} > 0.99$ eV gives distorted transfer characteristics proving themselves unsuitable to be used as a transistor (indicated as red entries in Table 3.6).



(a)



(b)

Figure 3.12: Threshold voltage and relative change in threshold voltage of DMG JLFinFETs belonging to (a) $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ category and (b) $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$ with gate metal pair arranged (from left to right) in the ascending order of $\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}}$.

Besides the obvious result that threshold voltage is dependent on the work function of M1 and M2 in a DMG structure, these bar charts convey some unexplored findings which are listed below. (a) Relative change in threshold voltage is lower for DMG JLFinFETs when $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$. This is due to better screening of channel region from drain bias by M2. (b) For both the cases where $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ and $\phi_{\mathrm{M1}} < \phi_{\mathrm{M2}}$, higher ϕ_{M1} and lower $\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}}$, results in lower relative change of threshold voltage. Of

all DMG pairs examined, the least relative threshold voltage change is observed for PtAu DMG JLFinFET (0.68%).

A comparative analysis among SMG JLFinFET with Au gate and Pt gate and DMG JLFinFET with PtAu gate (shown in Figure 3.13) proves that DMG transistor outperforms SMG in terms of relative change in threshold voltage.

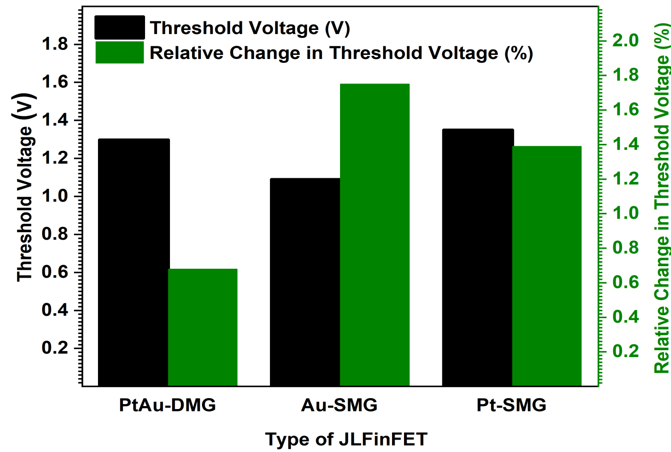
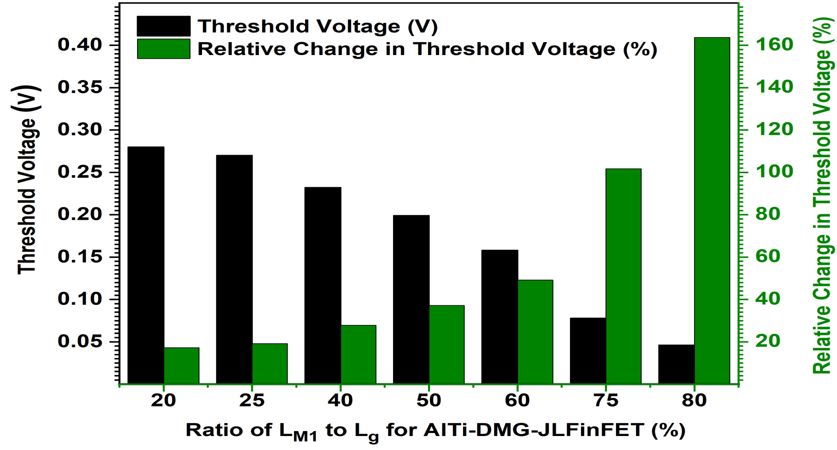
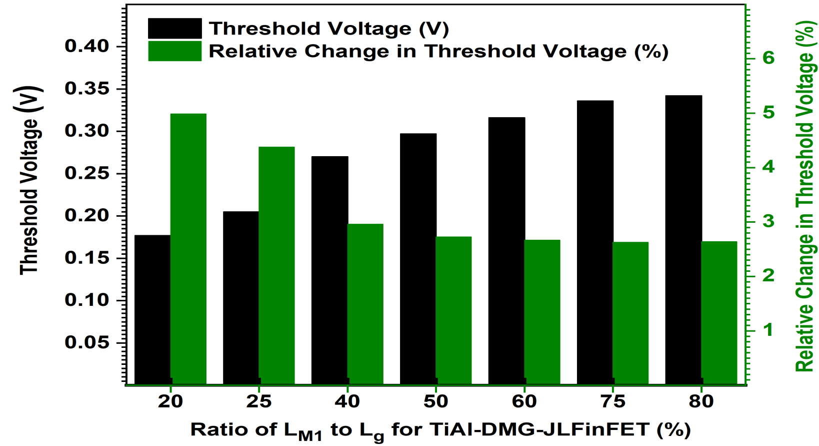


Figure 3.13: Threshold voltage and relative change in threshold voltage of PtAu DMG JLFinFET, Au SMG JLFinFET and Pt SMG JLFinFET.

Figure 3.14 depicts the threshold voltage and the relative change in threshold voltage when $\frac{L_{\mathrm{M1}}}{L_{\mathrm{g}}}$ is varied for the case of TiAl DMG JLFinFET and AlTi DMG JLFinFET. The significant findings of this analysis are: (a) when the metal with higher work function (Titanium in this case) spans over more of the gate area, irrespective of that metal being M1 or M2, the threshold voltage increases. This is obvious as the higher work function material occupies much of the gate area and strong depletion occurs in the channel region. It becomes necessary to apply more positive $\mathrm{V_{GS}}$ to bring the channel out of depletion. Hence $\mathrm{V_{th}}$ increases. (b) the rate of increase in threshold voltage with an increase in the length of higher work function metal is more prominent when the higher work function metal is M2 (c) the relative threshold voltage change is comparatively greater for AlTi DMG JLFinFETs as compared to TiAl DMG JLFinFETs. The cause for observations (b) and (c) could be attributed to the proximity of the drain electrode to M2.



(a)



(b)

Figure 3.14: Threshold voltage and relative change in threshold voltage for varying $\frac{L_{\text{M1}}}{L_g}$ in (a) TiAl DMG JLFinFET and (b) AlTi DMG JLFinFET keeping total gate length fixed to 10 nm.

Table 3.7 showcases a comparison of performance metrics of DMG transistors discussed in this chapter with existing DMG literature. Since 1999, DMG transistors are in limelight oqing to the various benefits expected in transistor by using two different gate materials. Over the years, DMG architecture got adopted in various types of transistors ranging from planar conventional FETs to non-planar junctionless FETs. From Table 3.7, it is visible that even with aggressive scaling, DMG transis-

tors (suitable multi-gate structures with DMG) are capable of having lower DIBL and nearly ideal SS.

Table 3.7: Comparison of proposed transistor with published literatures on DMG structure

Reference	Device	Total gate length	Supply voltage	Effective oxide thickness	DIBL	SS	Year of publication
Long *et al.* (1999)	DMG FET	1μm	2 V	*	23 mV/V	75 mV/dec	1999
Baruah and Paily (2013*a*)	DMG DGJLT	40 nm	1 V	1 nm	lower (not quantified)	lower (not quantified)	2013
Lou *et al.* (2012)	DMG JNT	40 nm	1 V	2 nm	35 mV/V	65 mV/dec	2012
Kusuma and Talari (2022)	DMG JLFinFET with high κ gate oxide	14 nm	0.8 V	1 nm	29.90 mV/V	62.7 mV/dec	2022
	Proposed structure in this work	10 nm	0.7 V	3 nm	12.88 mV/V	66.5 mV/dec	

* data not available

3.4 Summary

An investigation on the effects of work function and length ratio of gate materials on the performance of DMG JLFinFET is described in this chapter. DC analysis reveals that there is more shift in V_{th} with variation in ϕ_{M1} as compared to variation in ϕ_{M2}. Even though gate work function adjustment is the common practice of setting the threshold voltage of a transistor to the desired value, in DMG JLFinFET, $\frac{L_{M1}}{L_g}$ also play a major role in determining V_{th}. I_{tunn} is lower for DMG JLFinFET with $\phi_{M1} > \phi_{M2}$ with $\frac{L_{M1}}{L_g} = 50\%$ and decreases further with increase in $\phi_{M1} - \phi_{M2}$. DIBL is lower for the case when $\phi_{M1} > \phi_{M2}$. Least DIBL of 12.88 mV/V is obtained when $\phi_{M1} - \phi_{M2}$ is 0.38 eV (TiAl and NiTi gate pair). DIBL degradation with $\phi_{M1} - \phi_{M2}$ as well as $\frac{L_{M1}}{L_g}$ is less severe for DMG JLFinFET with $\phi_{M1} > \phi_{M2}$. SS is better for DMG JLFinFETs when $\phi_{M1} < \phi_{M2}$. The inherent disadvantage of SS degradation when $\phi_{M1} > \phi_{M2}$ could be eliminated by making $\frac{L_{M1}}{L_g} > 70\%$ in DMG JLFinFET. The relative change in threshold voltage is lower when $\phi_{M1} > \phi_{M2}$ and the least relative threshold voltage change of 0.68% is observed for PtAu DMG JLFinFET. Hence, a thorough analysis was conducted to explore the behaviour of DMG JLFinFET with various gate material combinations and gate length ratios. It was observed that, by combining optimal metal combinations with appropriate gate length ratios, DMG JLFinFET can be a promising candidate for VLSI circuits. Nonetheless, I_{ON} and $\frac{I_{ON}}{I_{OFF}}$ can also be enhanced by integrating appropriate technologies, hence increasing the attractiveness of DMG JLFinFET. This is discussed in Chapter 4.

Chapter 4

Performance enhancement of Dual Material Gate Junctionless FinFETs using Dielectric Spacer

4.1 Introduction

As seen in Chapter 3, using Dual Material Gate (DMG) architecture in a JLFinFET suppresses SCEs like DIBL to a great extent. There is more freedom to tune transistor characteristics as per our requirement by properly selecting the gate materials constituting DMG. However, a common drawback of all junctionless transistor types is lower ON current (I_{ON}) and $\frac{I_{ON}}{I_{OFF}}$. Therefore, by implementing strategies to address these shortcomings, the DMG JLFinFET can have greater appeal as a multi-transistor circuit contender. It is observed from literature that with proper spacer engineering, significant enhancement in junctionless transistor characteristics especially in terms of I_{ON} and $\frac{I_{ON}}{I_{OFF}}$ can be obtained (Kaur *et al.* (2022), Sreenivasulu and Narendar (2022)). Hence in this chapter, a detailed investigation is done on the effectiveness of various spacer materials having different spacer lengths (L_{SP}), in improving the performance of DMG JLFinFET. Many performance metrics like DIBL, SS, I_{ON}, I_{OFF}, $\frac{I_{ON}}{I_{OFF}}$ and I_{tunn} are closely monitored at L_g down to 10 nm. In Chapter 3 it is observed that TiAl DMG JLFinFET gave exemplary performance in terms of DIBL and SS. Hence in this chapter, rigorous analysis is done to determine the influence of dielectric constant and length of spacer on the DC and analog performance of TiAl DMG JLFinFET. The structure of the transistor simulated and particulars regarding the simulation setup

are given in Section 4.2. Section 4.3 presents the influence of dielectric constant as well as length of spacer on the performance of DMG JLFinFET using TCAD simulations followed by Section 4.4 where the key findings are summarised.

4.2 Structure of DMG JLFinFET with Spacer and Simulation Setup

(a) (b)

Figure 4.1: (a) 3-D structure and (b) 2-D cross-sectional view along A-A' cutline, of Dual Material Gate Junctionless FinFET with spacer

Figure 4.1 shows the 3-D structure as well as 2-D cross-sectional view (along the cutline A-A') of DMG JLFinFET with spacer. Device parameters used in simulations are listed in Table 4.1. It may be noted that n-type DMG JLFinFET is considered for studying the influence of spacers. The transistor under examination complies with the present IRDS standard in terms of size (Hoefflinger (2020)). Various oxides that are used as spacers along with their respective dielectric constants are listed in Table 4.2.

Simulations are performed using ATLAS, a 3-D device simulator, by Silvaco, Inc (Manual (2016*a*)). To determine the performance of DMG JLFinFET with gate lengths of 10 nm, quantum models are included in the simulation. Quantum Mechanical Drift Diffusion Mode Space model, band-to-band tunneling model, field-dependent mobility model, recombination model and impact ionization model are activated during simulation.

Table 4.1: Parameter specifications of Dual Material Gate Junctionless FinFET with spacers

Parameter	Value
Total gate length (L_g)	10 nm
Fin height (H_{fin})	5 nm
Fin thickness (T_{fin})	5 nm
Length of gate metal 1 (L_{M1})	5 nm
Length of gate metal 2 (L_{M2})	5 nm
Gate oxide thickness (t_{ox})	3 nm
Work function of metal 1 (ϕ_{M1})	4.66 eV
Work function of metal 2 (ϕ_{M2})	4.28 eV
Gate oxide material	HfO_2
Buried oxide material	SiO_2
Length of spacer (L_{SP})	2.5 nm, 5 nm, 7.5 nm
Channel doping concentration (N_d)	10^{18} cm^{-3}
Source/drain extension length (L_{ext})	9 nm

Table 4.2: Choice list of materials used as spacers along with their dielectric constants

Spacer material	Dielectric constant
Silicon Dioxide (SiO_2)	3.9
Silicon Nitride (Si_3N_4)	7.5
Aluminium Oxide (Al_2O_3)	9.3
Hafnium Oxide (HfO_2)	22
Titanium Dioxide (TiO_2)	80

4.3 Results

This section explains the effects of including spacers on both sides of the gate electrode, on the DC and analog performance of DMG JLFinFET. Dielectric constant and length of spacer materials are the prime parameters considered for various analyses throughout this section.

4.3.1 Analysing the Effect of Dielectric constant and Length of Spacer on Channel Electrostatics of TiAl DMG JLFinFET through Contour Plots

To study the effect of dielectric constant and length of spacer on the channel electrostatics of TiAl DMG JLFinFET, rigorous simulations were performed. Contour plots of electric field and electron concentration along xz cutplane at the middle of

the channel of TiAl DMG JLFinFET with different spacer materials, each of various lengths were inspected.

Figure 4.2(a) and 4.2(b) are contour plots of the electric field in TiAl DMG JLFinFET with varying spacer material and spacer length respectively. It may be noted that contour plots are taken along a plane parallel to the xz plane at y = $\frac{T_{\text{fin}}}{2}$ when $V_{GS} = V_{DS} = 0.7$ V

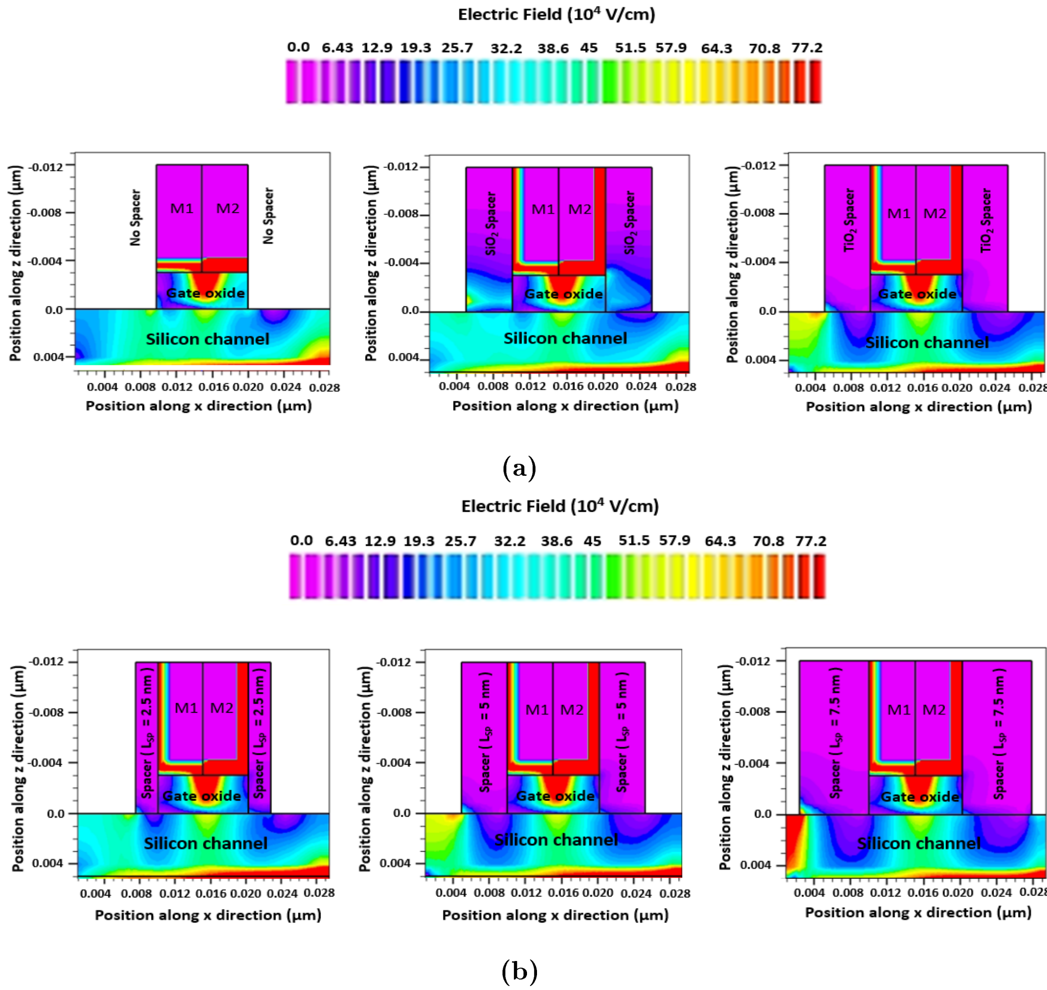
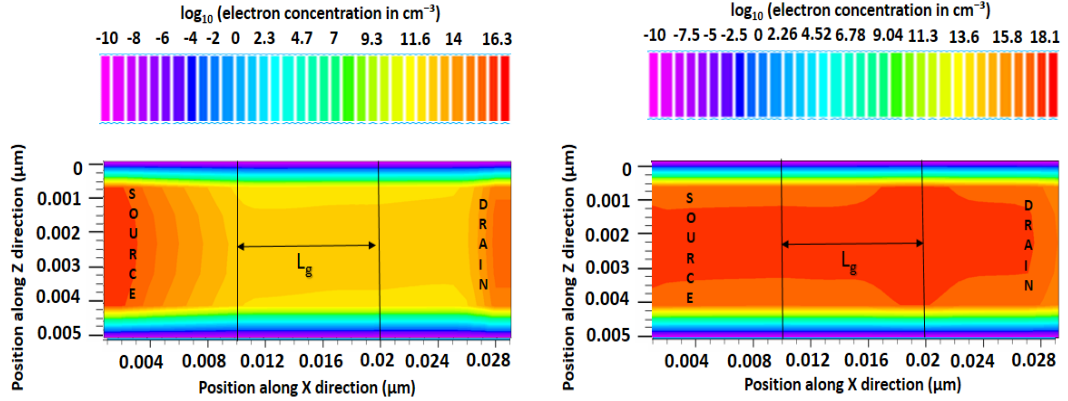


Figure 4.2: Contour plot of electric field along a cut-plane parallel to xz plane at y = $\frac{T_{\text{fin}}}{2}$ in TiAl DMG JLFinFET with (a) varying spacer materials having $L_{SP} = 5$ nm (b) TiO_2 spacer with varying L_{SP}, for $V_{GS} = V_{DS} = 0.7$ V. (x, z) = (x, 0 μm) is gate oxide-channel interface and (x, z) = (x, 0.005 μm) is buried oxide-channel interface.

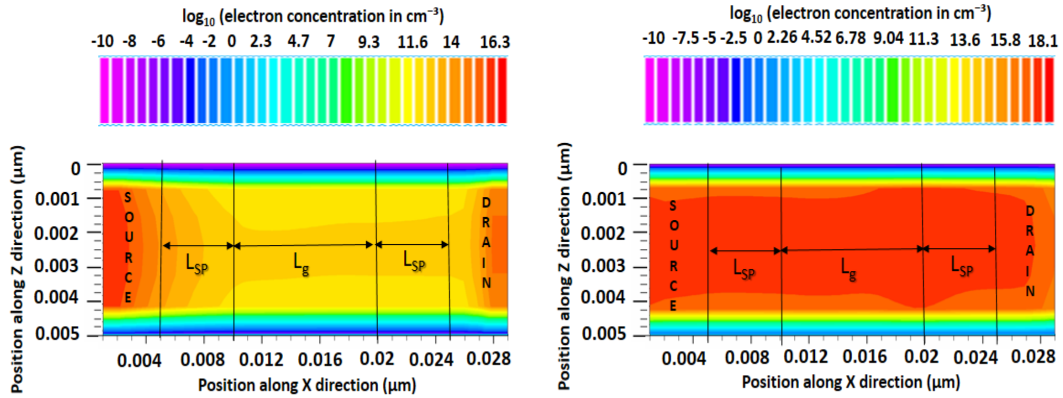
It can be observed in Figure 4.2 that, as the dielectric constant as well as length of the spacer increases, the lower electric field region in the channel (neutral region

having free charges available for conduction) near both sides of gate sidewalls extends to more area, thereby increasing I_{ON}. These contour plots give us a clear picture of the influence of spacer material and its length on the electric field profile in a DMG transistor.

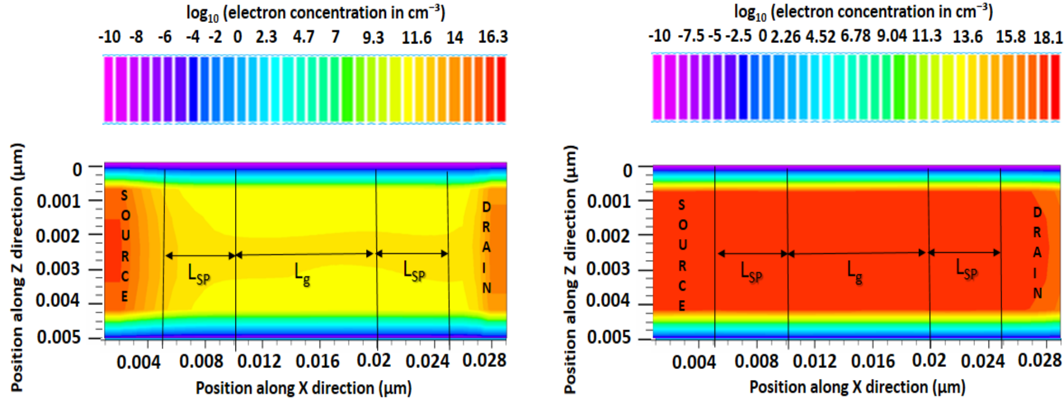
Figure 4.3 shows a set of contour plots of electron concentration in the channel of TiAl DMG JLFinFET (with no spacer, SiO_2 spacer and TiO_2 spacer) along a cut-plane parallel to xz plane at y = $\frac{T_{fin}}{2}$, in ON state as well as OFF state. It may be noted that the OFF state corresponds to V_{GS} = 0 V, V_{DS} = 0.7 V and the ON state has V_{GS} = V_{DS}= 0.7 V. A closer examination of the contour plots in Figure 4.3 shows lower electron concentration (more depletion) in the OFF state and higher electron concentration in the ON state, with high κ spacers.



(a)



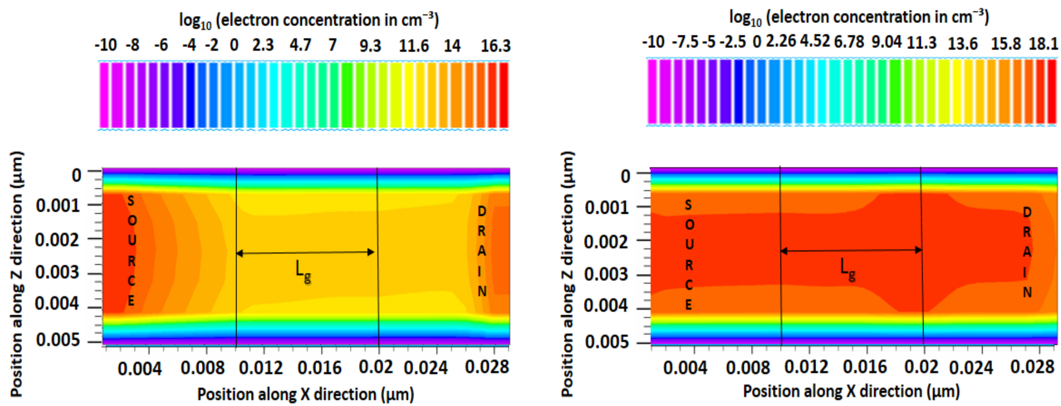
(b)



(c)

Figure 4.3: Contour plot of electron concentration along a cut-plane parallel to xz plane at y $= \frac{T_{\text{fin}}}{2}$, in TiAl DMG JLFinFET with (a) no spacer in OFF/ON state, (b) SiO_2 spacer in OFF/ON state and (c) TiO_2 spacer in OFF/ON state. L_{SP} for all these transistors is 5 nm. (x, z)=(x, 0 μm) is gate oxide-channel interface and (x, z) = (x, 0.005 μm) is buried oxide-channel interface.

Figure 4.4 shows a set of contour plots of electron concentration in the channel of TiAl DMG JLFinFET having TiO_2 spacer (with L_{SP} = 0 nm, 2.5 nm, 5 nm and 7.5 nm) along a cutline parallel to xz plane at y $= \frac{T_{\text{fin}}}{2}$, in ON state as well as OFF state. It is seen that as the spacer length increases, the depleted region (yellow region) extends to more channel area, causing a reduction in OFF current. More electrons are present in the channel as L_{SP} increases when the transistor is in the ON state. Hence, contour plots in Figure4.3 and Figure4.4 justify the trend shown by I_{OFF} and I_{ON} given in Figure 4.5.



(a)

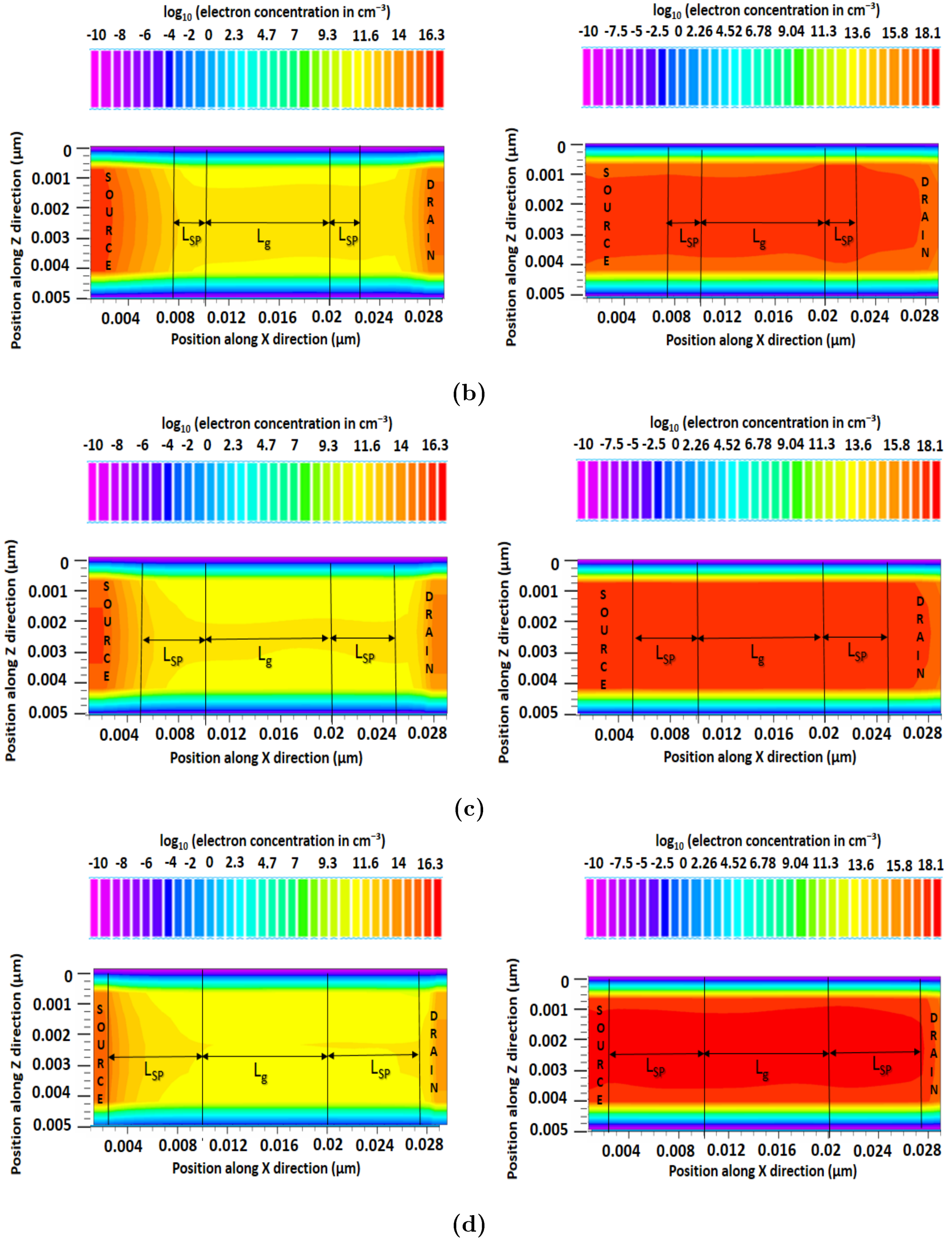


Figure 4.4: Contour plot of electron concentration along a cut-plane parallel to xz plane at y = $\frac{T_{\text{fin}}}{2}$ in TiAl DMG JLFinFET (a) with no spacer in OFF/ON state, (b) 2.5 nm TiO_2 spacer in OFF/ON state, (c) 5 nm TiO_2 spacer in OFF/ON state and (d) 7.5 nm TiO_2 spacer in OFF/ON state. (x, z)=(x, 0 μm) is gate oxide-channel interface and (x, z) = (x, 0.005 μm) is buried oxide-channel interface.

4.3.2 Effect of Dielectric Constant and Length of Spacer on DC Characteristics of TiAl DMG JLFinFET.

Figure 4.5(a) shows variation in I_{ON} and I_{OFF} with the dielectric constant of the spacer for L_{SP} of 2.5 nm, 5 nm and 7.5 nm. Here I_{ON} is the drain current at $V_{GS} = V_{DS} =$ 0.7 V and I_{OFF} is taken at $V_{GS} =$ 0 V, $V_{DS} =$ 0.7 V (Lee *et al.* (2016)). It is seen that I_{ON} increases as the dielectric constant of the spacer increases. This is due to the strong fringing field lines passing through the high κ spacer which enables more carriers available for conduction. I_{ON} also increases with increase in L_{SP}, due to the fringing field passing through a greater spacer area.

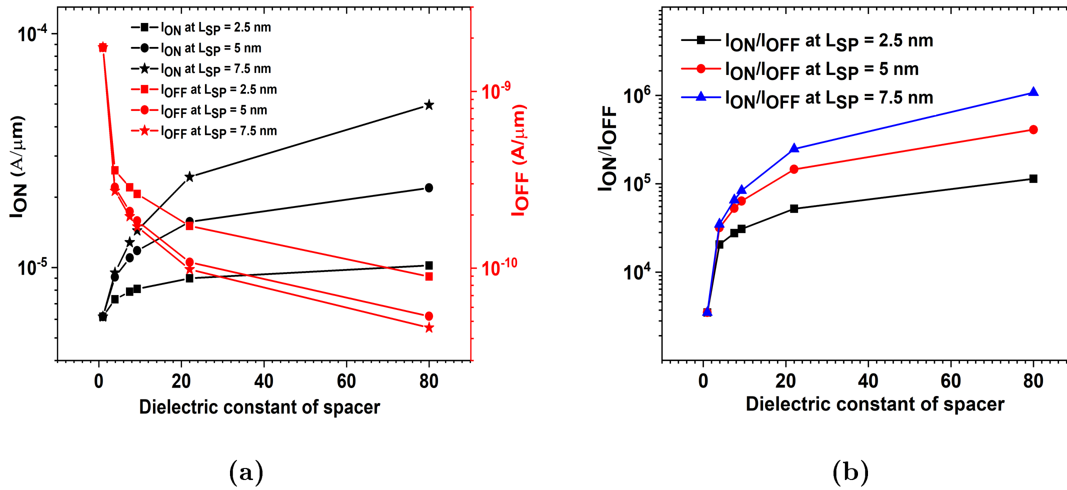


Figure 4.5: Variation in (a) ON current (black), OFF current (red) and (b) $\frac{I_{ON}}{I_{OFF}}$ with dielectric constant of spacer for L_{SP} = 2.5 nm, 5 nm and 7.5 nm.

Reduction in I_{OFF} is visible as the dielectric constant of the spacer increases due to the larger depletion of the channel area. I_{OFF} also decreases with increase in spacer length. However, the reduction in I_{OFF} is more prominent as L_{SP} increases from 2.5 nm to 5 nm. I_{OFF} reduces slightly when L_{SP} is increased above 5 nm to 7.5 nm and further. Hence dielectric constant and length of spacers play a major role in deciding $\frac{I_{ON}}{I_{OFF}}$ (performance indicator of a transistor). Enhancement in $\frac{I_{ON}}{I_{OFF}}$ is visible when the dielectric constant as well as length of spacers are increased as indicated in Figure 4.5(b).

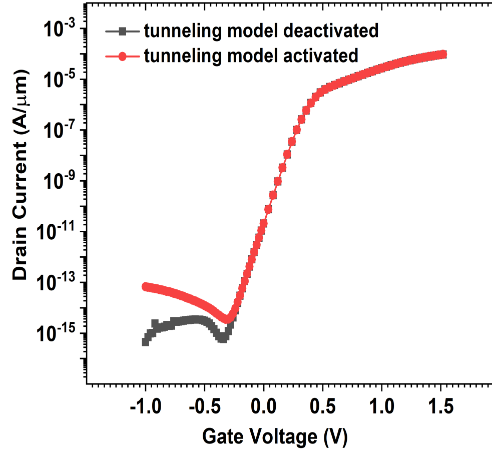


Figure 4.6: Transfer characteristics for TiAl DMG JLFinFET (having no spacer) including as well as excluding band-to-band tunneling model in the simulator at V_{DS} = 0.7 V

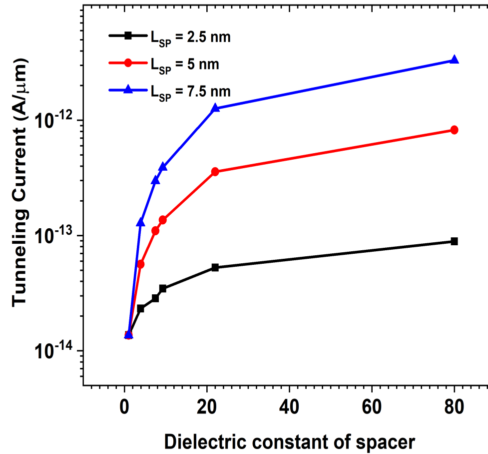


Figure 4.7: Variation in I_{tunn} with dielectric constant of spacer for L_{SP} = 2.5 nm, 5 nm and 7.5 nm.

Figure 4.6 shows the transfer characteristics of TiAl DMG JLFinFET when tunneling models are included as well as excluded in the device simulator. When the tunneling models are deactivated in the simulator, current flow in the deep sub-threshold region is lower by at least one order of magnitude compared to the drain current obtained incorporating tunneling probability. This proves the dominance of lateral

band-to-band tunneling in causing current flow through the transistor when the gate is supplied with voltages far lower than its threshold voltage. Hence an important parameter to measure current leakages in the cut-off state of the transistor, namely tunneling current (I_{tunn}) is determined with various spacer materials and spacer lengths. I_{tunn} is taken at V_{GS} = -0.5 V and V_{DS} = 0.7 V.

Figure 4.7 shows that there is an increase in I_{tunn} with increase in the dielectric constant of spacers. As spacers with a higher dielectric constant are used, there is a much stronger depletion of the channel at the negative gate bias region. Hence the band bending gets steeper aiding more electrons to tunnel from channel to drain. The same effect happens when the spacer length is increased.

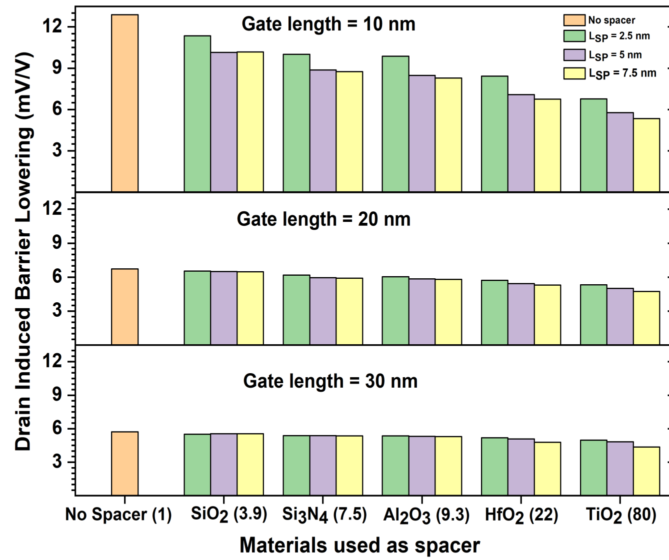
There is an enhancement in the performance of TiAl DMG JLFinFET, as the spacer length is increased from 2.5 nm to 5 nm. Increasing L_{SP} from 5 nm to 7.5 nm gives marginal improvement for most of the device metrics (except I_{ON}). Nevertheless, I_{tunn} increases tremendously when L_{SP} increases from 5 nm to 7.5 nm causing higher OFF state leakage and power dissipation. This is a demerit in DMG JLFinFET with high L_{SP}. Hence 5 nm can be chosen as a suitable L_{SP} to obtain better functioning of the transistor without serious degradation in its performance metrics.

4.3.3 Effect of Dielectric Constant and Length of Spacer on Short Channel Effects in TiAl DMG JLFinFET.

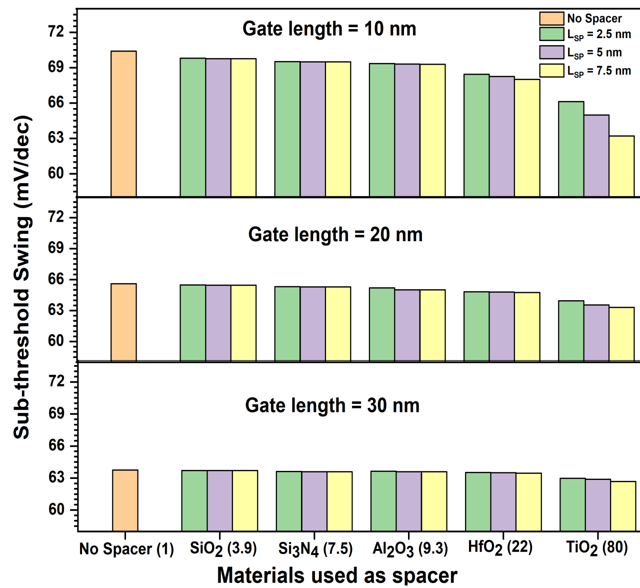
In this sub-section, the influence of dielectric constant and length of spacers on short channel performance metrics as well as carrier concentration profile in the channel of TiAl DMG JLFinFETs are explored.

Figure 4.8(a) and 4.8(b) respectively show DIBL and SS of DMG JLFinFET having spacers made of materials listed in Table 4.2 at L_{SP} of 2.5 nm, 5 nm and 7.5 nm. The bar charts in Figure 4.8 give a picture of the extent of degradation in DIBL and SS as L_g reduces from 30 nm to 20 nm and finally down to 10 nm. As expected, degradation in DIBL and SS is observed with a decrease in L_g. On average, DIBL increases by 0.62 mV/V when L_g decreases from 30 nm to 20 nm and by 3.46 mV/V as L_g decreases further to 10 nm. SS also increases by 1.42 mV/dec as L_g decreases from 30 nm to 20 nm and by 4.97 mV/dec as L_g scales down to 10 nm. It is seen that for all channel lengths, DIBL reduces as the dielectric constant of the spacer is increased irrespective of spacer length. This is because when oxides with a higher dielectric constant are

used as spacers, there will be more effective coupling of the gate to the source/drain region due to the fringing electric field. This effectively depletes more channel area on both sides of the gate. The same condition exists when the length of the spacer increases.



(a)



(b)

Figure 4.8: (a) DIBL and (b) SS variation with dielectric constant of spacer (L_{SP} = 2.5 nm, 5 nm and 7.5 nm.) for L_g = 10 nm, 20 nm and 30 nm

Under both situations, the effect of drain bias on channel potential becomes less

pronounced and its influence on threshold voltage (V_{th}) gets reduced. Thus DIBL decreases.

It is seen that as the channel length scales down to 10 nm, the depletion region formed under spacers will have dimensions comparable to the channel length. Hence the influence of the dielectric constant and length of spacer on DIBL gets more prominent at lower L_g (visible in Figure 4.8(a)).

Fringing field lines are more crowded near the gate edge than at locations farther away from the gate sidewalls. So the variation in these field lines is more between 2.5 nm and 5 nm as compared to variation in field lines near 7.5 nm which is reflected as a greater reduction in DIBL as L_{SP} is increased from 2.5 nm to 5 nm and lesser reduction as L_{SP} increases further to 7.5 nm. This phenomenon gets more pronounced as L_g decreases.

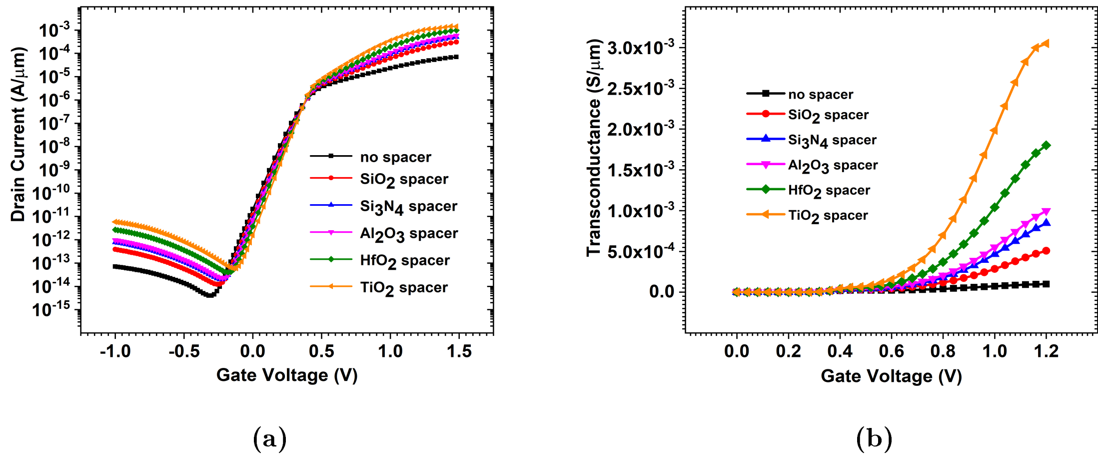
Variation of SS with the dielectric constant of spacer for L_{SP} of 2.5 nm, 5 nm and 7.5 nm is shown in Figure 4.8(b). This is explained in two cases. Case (i): As the dielectric constant of the spacer increases, there is more effective depletion of the channel in the OFF state and an increase of current in the ON state. So effective gate length increases thereby causing a reduction in SS. Case (ii): As L_{SP} increases, the presence of spacer materials spanning over more regions adjacent to gate sidewalls causes more fringing field lines to pass through these spacer dielectrics in turn resulting in more gate control over the channel, thereby reducing SS. However, case (i) and case (ii) become more visible at lower gate lengths (10 nm). This is because the spread of the depletion region beneath spacers affects the effective gate length considerably at lower device dimensions due to the comparable length of the depletion region with that of the gate. Significant improvement in DIBL and SS is observed when L_{SP} increases to 50% of source-drain extension length (around 5 nm). Considering the present-day technology requirements as well as the significant impact of spacer materials on DIBL and SS at smaller channel lengths, L_g of 10 nm is opted for further study.

4.3.4 Effects of various Spacer Materials on DC and Analog Parameters of TiAl DMG JLFinFET having Optimised Spacer Length of 5 nm

In this sub-section, an exclusive analysis is done on the effects of spacer materials on DC as well as analog performance metrics of a TiAl DMG JLFinFET. The spacer

length chosen is 5 nm due to better performance obtained in terms of I_{ON}, I_{OFF} while keeping I_{tunn} under control. Rigorous TCAD simulations were conducted on TiAl DMG JLFinFET with different spacer materials and the results are presented.

4.3.4.1 Impact of Spacer Material on the Drain Current and Transconductance



(a) (b)

Figure 4.9: (a) Transfer characteristics and (b) transconductance with respect to V_{GS}, of TiAl DMG JLFinFET with different spacer materials at V_{DS} = 0.7 V.

Figure 4.9(a) shows the transfer characteristics of TiAl DMG JLFinFET with different spacer materials at a constant drain voltage of 0.7 V. As the dielectric constant of the spacer increases, there is an increase in the current that flows through the transistor at a higher gate bias. The rate of increase of this current with gate voltage is also higher when high κ materials are used as spacers. This is reflected in the transconductance curve shown in Figure 4.9(b). The prime cause for this trend is the increase in fringe capacitance which aids more carriers in the channel, available for current conduction.

Variations of drain current with drain voltage at a constant gate voltage of 0.7 V for various spacer materials are shown in Figure 4.10(a). It is observed that the drain current increases as the dielectric constant of the spacer increases due to higher carrier concentration in the channel caused by increased coupling of the gate to the channel by high κ spacers. Figure 4.10(b) shows the increase in output conductance of TiAl DMG JLFinFET as the spacer dielectric constant increases. This is due to a higher drain current in the channel when a high κ dielectric material is used as spacer.

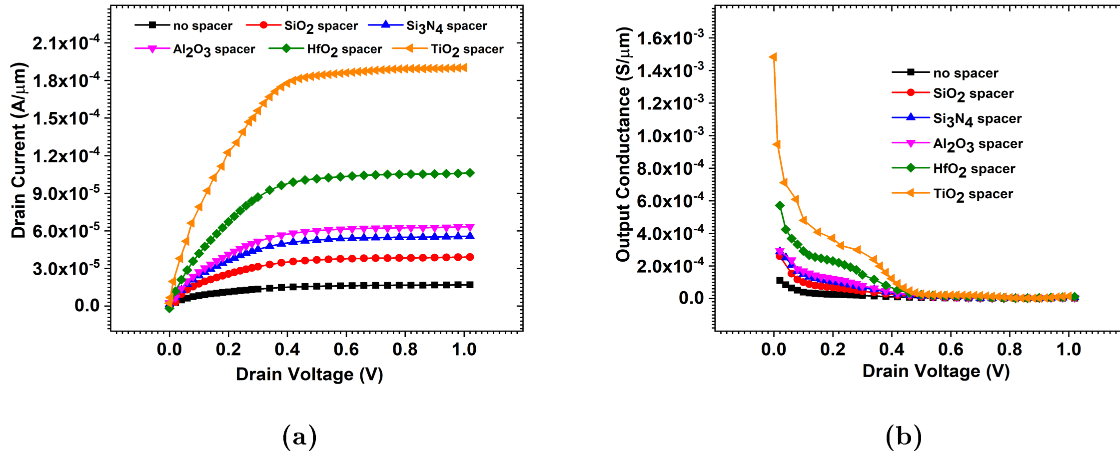


Figure 4.10: Variation of (a) output characteristics (b) output conductance with respect to V_{DS} of TiAl DMG JLFinFET with different spacer materials at V_{GS} = 0.7 V.

4.3.4.2 Influence of Spacer Material on Analog Performance Metrics

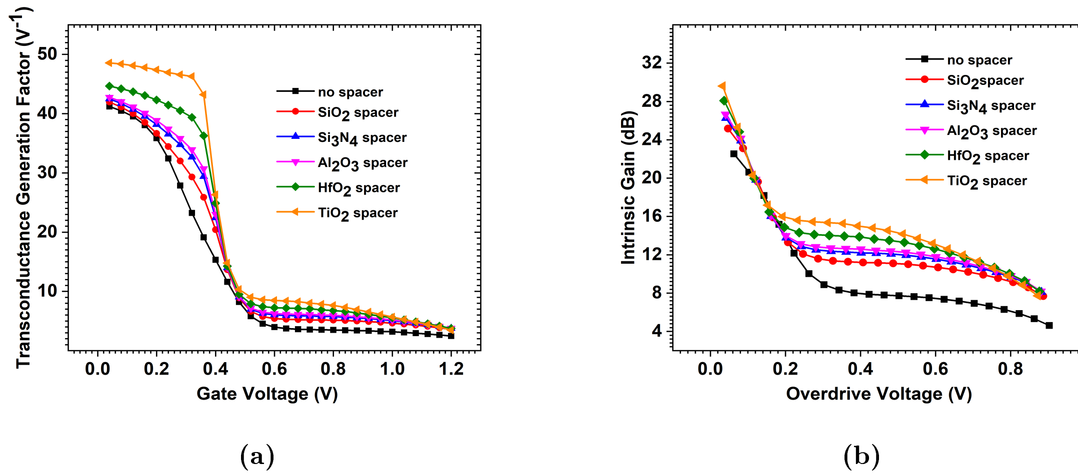


Figure 4.11: Variation of (a) transconductance generation factor (TGF) with V_{GS} and (b) intrinsic gain with overdrive voltage, of TiAl DMG JLFinFET with various spacer materials at V_{DS} = 0.7 V.

Variation of Transconductance Generation Factor (TGF), which is a figure of merit for the analog performance of a transistor, with gate voltage is shown in Figure 4.11(a). This factor which is the ratio of transconductance to drain current indicates how effectively a transistor can convert drain current to transconductance (Baruah and

Paily (2013*b*)). TGF is higher for smaller gate voltage due to the lower drain current in the channel. However, TGF reduces drastically when the channel starts conducting and gives considerable drain current. It is observed that TGF increases when high κ dielectrics are used as spacers. This increase in TGF is more prominent for lower gate voltages. For V_{GS} = 0.2 V and V_{DS} = 0.7 V, TGF increases from 36.66 V^{-1} to 42.31 V^{-1} and further to 47.4 V^{-1} when spacer materials used respectively are SiO_2 (κ = 3.9), HfO_2 (κ = 22) and TiO_2 (κ = 80). When the transistor is in ON state, TGF variation is lower (TGF = 4.63 V^{-1}, 5.52 V^{-1} and 5.68 V^{-1} for SiO_2, HfO_2 and TiO_2 respectively) due to respective increase in the transconductance as well as the drain current.

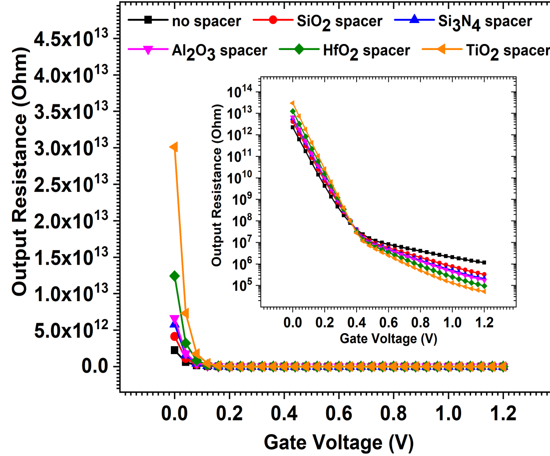


Figure 4.12: Variation of output resistance with V_{GS} of TiAl DMG JLFinFET with different spacer materials at V_{DS} = 0.7 V.

Figure 4.11(b) shows the intrinsic gain variation with overdrive voltage (V_{GS} - V_{th}) of TiAl DMG JLFinFET with various spacer materials. Intrinsic gain gives the measure of basic voltage gain that a transistor could provide and is given as the product of transconductance and output resistance (Baruah and Paily (2013*a*)). The higher transconductance of TiAl DMG JLFinFET with a high κ spacer results in higher intrinsic gain. Value of intrinsic gain obtained for TiAl DMG JLFinFET at V_{DS} = 0.7 V and V_{GS} = 1 V are 10.22 dB with SiO_2 spacer, 11.74 dB with HfO_2 spacer and 11.98 dB with TiO_2 spacer. Hence, it is visible that when high κ dielectric materials are used as spacers, transistors are a better candidate for high-gain amplifier circuits.

Figure 4.12 shows output resistance (R_{out}) variation with for TiAl DMG JLFinFETs with various spacer materials. The inset shows the variation of output resistance in the log scale. Below the threshold voltage, the channel is mostly depleted, making itself a highly resistive path for the drain current to flow. Once the device is ON and as the gate voltage is increased further, the channel becomes more conductive (R_{out} becomes lower). The phenomenon of higher R_{out} in OFF state and lower R_{out} in ON state gets more pronounced when high κ spacers are used as they promote both stronger depletion of channel in OFF state and increased availability of charge carriers in ON state.

Table 4.3: Comparison of performance metrics of DMG JLFinFET with conventional and junctionless FETs published in literature.

Reference	Device	Total gate length (nm)	Supply voltage (V)	Spacer material (with L_{SP} in nm)	V_{th} (V)	I_{OFF} A/μm	I_{ON} A/μm	DIBL ($\frac{mV}{V}$)	SS ($\frac{mV}{decade}$)
Singh and Yadav (2022)	Conventional FinFET	20	0.6	Nil	0.127	$3.5X^{-12}$	$2.48X10^{-4}$	58	69.76
Park *et al.* (2012)	IM nanowire FET	20	1	SiO_2 (5 nm)	0	10^{-7}	$1.14X10^{-3}$	80	90
Gundapaneni *et al.* (2011)	JLT	20	1	HfO_2 (15 nm)	$\sim$ 0.2	$2X10^{-10}$	$4X10^{-4}$	54	75
Baruah and Paily (2013*b*)	DGJLT	20	1	HfO_2 (20 nm)	0.25	10^{-11}	$6.6X10^{-4}$	27	65
Yang *et al.* (2018)	GAAJLT	5	0.4	HfO_2 (5 nm)	-0.15	$9.37X10^{-10}$	$5.56X10^{-3}$	15	61
Vadthiya *et al.* (2021)	JLFinFET	10	0.7	Nitride + HfO_2 (9 nm)	0.235	$6.24X10^{-11}$	$8.14X10^{-5}$	75.75	62.01
This work	DMG JLFinFET	10	0.7	HfO_2 (5 nm)	0.305	1.57_{-5}	1.08^{-10}	7	68

Table 4.3 lists a comparison in performances of various junctionless transistors having high κ spacers from existing literature as well as the transistor discussed in this article. Although better $\frac{I_{ON}}{I_{OFF}}$ among non-planar transistors is observed in Gate All Around junctionless transistor with spacer (Yang *et al.* (2018)), they have the drawback of being not fabrication-friendly for multi-transistor circuits. Whereas DMG JLFinFET has lesser fabrication complexity and has negligible DIBL and reasonably better SS. Hence, excellent performance considering overall device operation metrics, at channel length as low as 10 nm, is exhibited by DMG JLFinFET with appropriate spacer material and spacer length.

4.4 Summary

The effects of incorporating spacers in a DMG JLFinFET are explored in detail in this chapter. The extent of suppression of short channel effects of DMG JLFinFET under the influence of various spacer materials with different spacer lengths is investigated. DIBL reduces tremendously as the dielectric constant and the length of the spacer are increased. SS also reduces with an increase in the dielectric constant of the spacer but there is a marginal reduction with increase in the spacer length. A significant increase in I_{ON} and reduction in I_{OFF} is observed as the dielectric constant of the spacer increases. I_{OFF} decreases as the spacer length is increased from 2.5 nm but much impact on I_{OFF} is not visible as L_{SP} is increased above 5 nm. There is an increase in the I_{tunn} with the increase in the dielectric constant and length of the spacer. At 10 nm channel length, 5 nm may be chosen as a suitable spacer length for a transistor without serious degradation in any of its performance metrics. HfO_2 of length $\frac{L_{ext}}{2}$ is the preferred high κ spacer material for DMG JLFinFET as it improves all DC and analog performance metrics alongside keeping tunneling current reasonably lower. There is also the added advantage of fabrication easiness with HfO_2 spacer as the same material is used for gate oxide.

Chapter 5

An improved Fourier series based analytical model for threshold voltage and sub-threshold swing in SOI Junctionless FinFET

5.1 Introduction

As seen in previous chapters, junctionless transistors are a promising candidate for VLSI circuits as it exhibits exemplary performance and better immunity to SCE. They have the added merit of simpler fabrication as formation of heavily doped source and drain regions inside a substrate with dopants of opposite polarity is not needed. For analysing the behaviour of these transistors especially when they are part of various electronic circuits, mathematical models that can mimic their electrical characteristics have to be developed. These mathematical models are then used in circuit simulators to predict the nature of complex circuits containing large number of such transistors. Many models associated to junctionless planar as well as non-planar structures are available in literature. An appealing research work was published in 2016 by Hu *et al.* which gives the analytical model for channel potential, threshold voltage as well as sub-threshold swing in SOI JLFinFET by solving 3-D Poisson's equation directly (Hu *et al.* (2016)). This Fourier series based model is widely accepted by various research groups and hence an in-depth study into their model formulations is done. In this chapter,

a more accurate Fourier series based analytical models for threshold voltage (V_{th}) and Sub-threshold Swing are developed for JLFinFET on SOI substrate, taking into account the location of onset of current conduction in the channel.

Section 5.2 presents structure of SOI JLFinFET with information on device parameters and coordinates of various parts of transistor. Models used throughout device simulation are also briefed here. Section 5.3 analyses channel potential model published by Hu *et al.* (2016). This section also gives insight on the location of onset of current conduction through simulation results and put forth a more accurate model for threshold voltage and SS. Section 5.4 handles validation of developed model for threshold voltage and SS with the help of TCAD simulations. Section 5.5 concludes the work by presenting significant findings in brief.

5.2 Device Structure and Simulation Conditions

The 3-D structure of JLFinFET with SOI substrate is shown in Figure 5.1 and the default device parameters considered in this work are enlisted in Table 5.1. All the device simulations were conducted using a 3-D device simulator namely ATLAS Version: 5.2.23.R provided by Silvaco.Inc Manual (2016*a*). Dimensions of the FinFET were chosen in accordance with the current technology requirements. The study was conducted on n-type JLFinFET with a uniformly doped active region. The gate length considered in this work is 20 nm. The gate oxide spanning around the channel (top gate oxide + both side gate oxide) had same thickness of 1.5 nm making the channel strongly under control of both the top gate as well as the side gates.

Considering the physical phenomenon inherent to junctionless transistors of sub-50 nanometre dimensions, various models were activated in the simulator. As our study involves transistors with sub-10 nanometre dimensions, to accurately capture the behaviour of these miniature transistors, quantum models were incorporated too. Hence, the drift-diffusion mode space model coupled with the Schrodinger equation was used. As silicon film in JLFinFET is heavily doped, impact ionization occurs, especially in the bulk and hence impact ionization models are included in the simulation. To account for interband tunneling due to steep band bending at the channel-drain interface in a JLFinFET, particularly in the OFF state, band-to-band tunneling model is activated. On account of the mobility degradation of carriers under the influence of electric field, the field-dependent mobility model was deployed. The Shockley-

Read-Hall (SRH) Recombination model is activated to regulate carrier generation and recombination in the silicon channel.

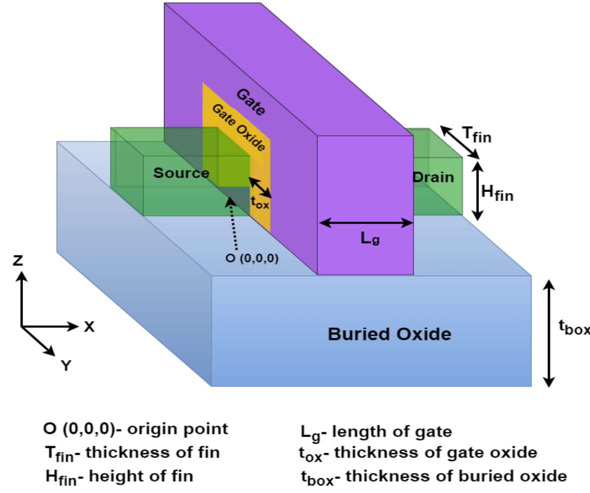


Figure 5.1: 3-D structure of JLFinFET on SOI substrate

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Table 5.2 is included to give a clear picture regarding the coordinates of various points in the channel as further discussions in the upcoming sections rely on these coordinates to a great extent. It may be noted that the channel of transistor under study spans as : $0 \leq \mathrm{x} \leq \mathrm{L_g}$; $\frac{-T_{\mathrm{fin}}}{2} \leq \mathrm{y} \leq \frac{T_{\mathrm{fin}}}{2}$; $0 \leq \mathrm{z} \leq \mathrm{H_{fin}}$. The origin point O (0,0,0) is indicated in Figure 5.1.

Table 5.1: Device Parameters

Parameter	**Value**
Temperature	300 K
Gate length	20 nm
Fin height	12 nm
Fin width	8 nm
Work function of gate	5.25 eV
Gate oxide thickness	1.5 nm
Gate oxide material	SiO_2
Buried oxide thickness	12 nm
Buried oxide material	SiO_2
Channel doping concentration	10^{19} cm^{-3}

Table 5.2: Coordinate information

Co-ordinate	Location
x = 0	source end
x = L_g	drain end
y = 0	mid-channel
y = $\frac{-T_{\text{fin}}}{2}$	channel - side gate oxide interface
y = $\frac{T_{\text{fin}}}{2}$	channel - side gate oxide interface
z = 0	channel - buried oxide interface
z = H_{fin}	channel - top gate oxide interface

5.3 Modified Model for Threshold Voltage and Sub-threshold Swing

In this section, an exclusive analysis is done on an already published channel potential model Hu *et al.* (2016). A deeper understanding of transistor physics is targeted with the help of simulations. This in turn sheds light on certain approximations that can give way for more accurate threshold voltage and sub-threshold swing models. The model formulation for SS which takes into account approximations based on transistor channel formation is also dealt with in this section.

5.3.1 Background of Channel Potential Model Formulation

To obtain an analytical expression for the channel potential of non-planar transistors like JLFinFET with dimensions in nanometre regime, 3-D Poisson's equation must be solved. 3-D Poisson's equation considering x-y-z coordinates is given by equation (5.1).

$$\frac{\partial^2\Psi}{\partial x^2}+\frac{\partial^2\Psi}{\partial y^2}+\frac{\partial^2\Psi}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}}\left[1-\exp\left(\frac{\Psi-V}{V_t}\right)\right] \tag{5.1}$$

where Ψ is electric potential, N_d is the doping concentration of channel, ε_{si} is permittivity of silicon which is the channel material, V_t is thermal voltage and V represents quasi-Fermi potential. Taking into consideration, depletion approximation that remains valid while modeling threshold voltage of a junctionless transistor, equation (5.1) simplifies to

$$\frac{\partial^2\Psi}{\partial x^2}+\frac{\partial^2\Psi}{\partial y^2}+\frac{\partial^2\Psi}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}} \tag{5.2}$$

It must be pointed out that FinFET modeling is more complex due to lack of structural symmetry and hence intelligent approximations need to be incorporated in the boundary conditions to directly solve the tough 3-D Poisson's equation analytically. The entire channel - gate oxide - buried oxide combination can be considered as a homogenous silicon block. This cuboidal silicon has an effective thickness (T_{eff}) and effective height (H_{eff}), such that symmetric cases could be incorporated in the boundary conditions. This treatment is well explained by Pei *et al.* (2002). The channel potential model by Hu *et al.* (2016) is given below as it is the base model of our study and it is needed to explain our findings in the upcoming section. Equation (5.3) to (5.9) represents the boundary conditions to compute channel potential.

$$\Psi(0, y, z) = V_R \tag{5.3}$$

$$\Psi(L_g, y, z) = V_R + V_{DS} \tag{5.4}$$

$$\Psi\left(x, T_{eff}/2, z\right) = V_{GS} - \Psi_{sch} \tag{5.5}$$

$$\Psi\left(x, -T_{eff}/2, z\right) = V_{GS} - \Psi_{sch} \tag{5.6}$$

$$\Psi\left(x, y, H_{eff}\right) = V_{GS} - \Psi_{sch} \tag{5.7}$$

$$\left.\frac{\partial \Psi}{\partial z}\right|_{z=0} = 0 \tag{5.8}$$

$$\Psi\left(x, y, -H_{eff}\right) = V_{GS} - \Psi_{sch} \tag{5.9}$$

where T_{eff} (effective channel thickness) as well as H_{eff} (effective channel height) are given by equation (5.10) and (5.11) respectively.

$$T_{eff} = \sqrt{T_{fin}\left(T_{fin} + 4t_{ox}\varepsilon_{si}/\varepsilon_{ox}\right)} \tag{5.10}$$

$$H_{eff} = \sqrt{H_{fin}\left(H_{fin} + 2t_{ox}\varepsilon_{si}/\varepsilon_{ox}\right)} \tag{5.11}$$

V_R represents the reference voltage present at the source side (source and drain extension regions are not considered in this work). V_{DS} and V_{GS} are drain voltage and gate voltage respectively. Ψ_{sch} is gate schottky barrier voltage. ε_{ox} is the permittivity of gate oxide material.

Equation (5.5), (5.6), (5.7) and (5.9) stems from the homogenous cuboidal silicon approximation explained in Pei *et al.* (2002) and equation (5.8) is from the assumption that the parabolically varying channel potential in z-direction is maximum at z = 0.

With the above mentioned boundary conditions, solution for the simplified 3-D poisson's equation is given in detail by Guangxi Hu *et al.* (Hu *et al.* (2016)). The final expression for channel potential along x-y-z direction is expressed as a Fourier series as in equation (5.12).

$$\Psi(x, y, z) = V_R + \frac{V_{DS}}{L_g} x + \sum_{n=1}^{\infty} A_n(y, z) \sin\left(\frac{n\pi}{L_g} x\right) \tag{5.12}$$

where

$$A_n(y, z) = G_n(y, z) + \Psi_n \tag{5.13}$$

$$G_n(y, z) = \sum_{m=1}^{\infty} \sum_{l=1}^{\infty} g_{ml}(n) \cos\left[\frac{(m - 0.5)\pi}{t} y\right] \cos\left[\frac{(l - 0.5)\pi}{h} z\right] \tag{5.14}$$

$$g_{ml}(n) = \frac{(-1)^{m+l+1} 4 \left(d_n + k_n^2 \Psi_n\right)}{(m - 0.5)(l - 0.5)\pi^4 \left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{{L_g}^2}\right]} \tag{5.15}$$

$$\Psi_n = \frac{2}{n\pi} \left\{(V_{GS} - \Psi_{sch} - V_R) \left[1 - (-1)^n\right] + V_{DS}(-1)^n\right\} \tag{5.16}$$

$$k_n = \frac{n\pi}{L_g} \tag{5.17}$$

$$d_n = \frac{2qN_d}{n\pi\epsilon_{si}} [(-1)^n - 1] \tag{5.18}$$

$$t = \frac{T_{eff}}{2} \tag{5.19}$$

$$h = H_{eff} \tag{5.20}$$

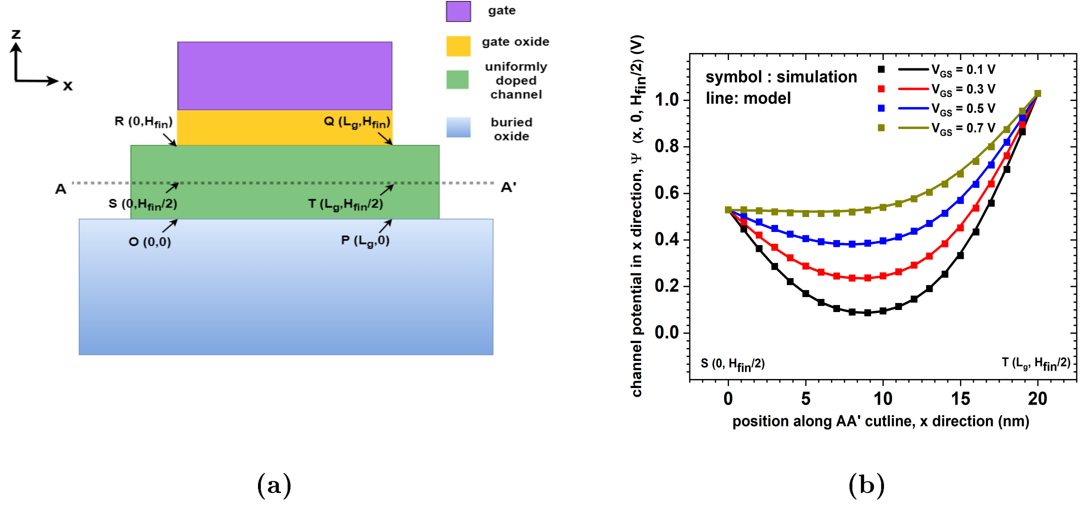
m, n, l = 1, 2, 3....

A deeper look at the results by Hu *et al.*, reveals that the analytical model for V_{th} and SS, underestimates the simulation results. Recognising the work presented in Hu *et al.* (2016), a detailed study was done to discover the source of the difference between modeled and simulated values and improve the model for threshold voltage and sub-threshold swing. This is detailed in the upcoming sub-sections.

5.3.2 Analysis of Channel Potential Variation along X, Y and Z Direction

To explore the cause of the analytical model in Hu *et al.* (2016) underpredicting V_{th} and SS values, the channel potential variation across x, y and z directions, were

examined. The channel potential variation along x and y directions presented in Hu *et al.* (2016) were reproduced and a good match was observed between the analytical model (5.12) and simulation results with varying V_{GS}. This can be seen in Figure 5.2 and Figure 5.3 respectively.



(a) (b)

Figure 5.2: (a) 2-D cross sectional view of JLFinFET in xz plane at y = 0 and (b) channel potential variation along A-A' between points 'S' and 'T' at different V_{GS}. V_{DS} taken is 0.5 V.

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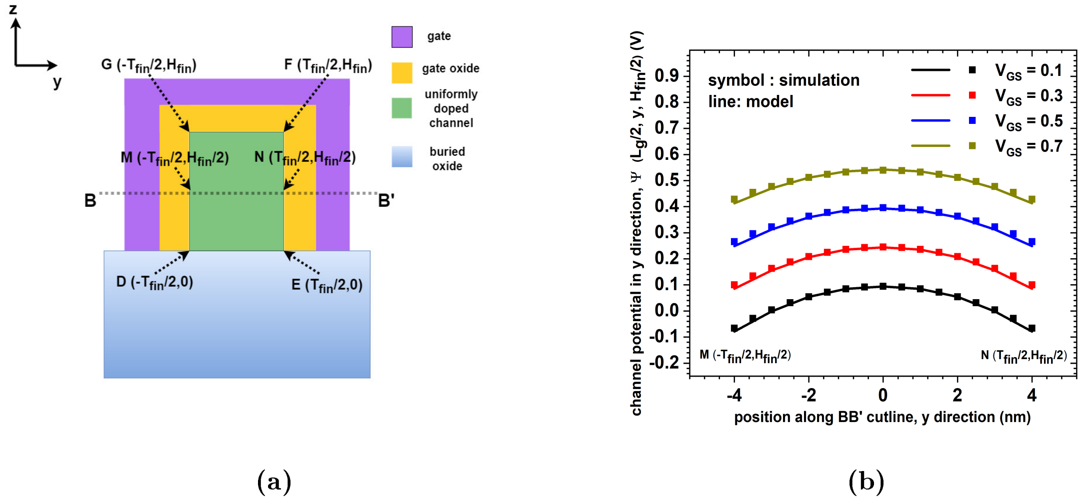

(a) (b)

Figure 5.3: (a) 2-D cross sectional view of JLFinFET in yz plane at x = $\frac{L_g}{2}$ and (b) channel potential variation along B-B' between points 'M' and 'N' at different V_{GS}. V_{DS} taken is 0.5 V.

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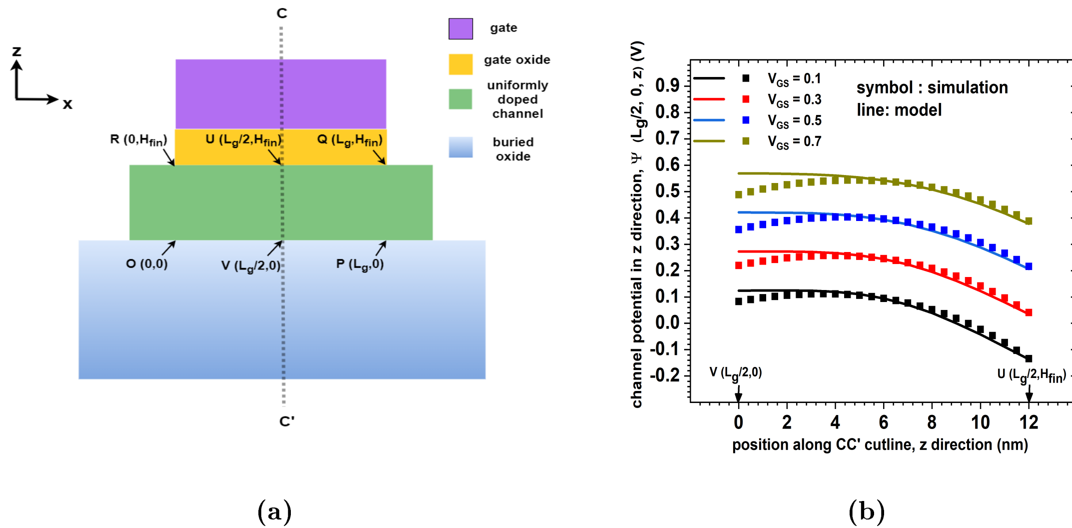
However, there is a discrepancy between the mathematical model given by equation (5.12) and the simulation results when channel potential along the z direction is considered. This is shown in Figure 5.4. It is seen that in Figure 5.4 (b), the analytical model given in equation (5.12) fails to predict the channel potential in the region closer to channel-buried oxide interface. It has to be pointed out that, to model threshold voltage in JLFinFET, determination of the location of the maximum potential point in the z direction in the channel plays a crucial role. This point of maximum potential gets undepleted first as gate voltage increases and therefore can be considered as the location where the onset of current conduction happens (Hu *et al.* (2016)).



(a) (b)

Figure 5.4: (a) 2-D cross sectional view of JLFinFET in xz plane at y = 0 and (b) channel potential variation along C-C' between points 'U' and 'V' at different V_{GS}. V_{DS} taken is 0.5 V.

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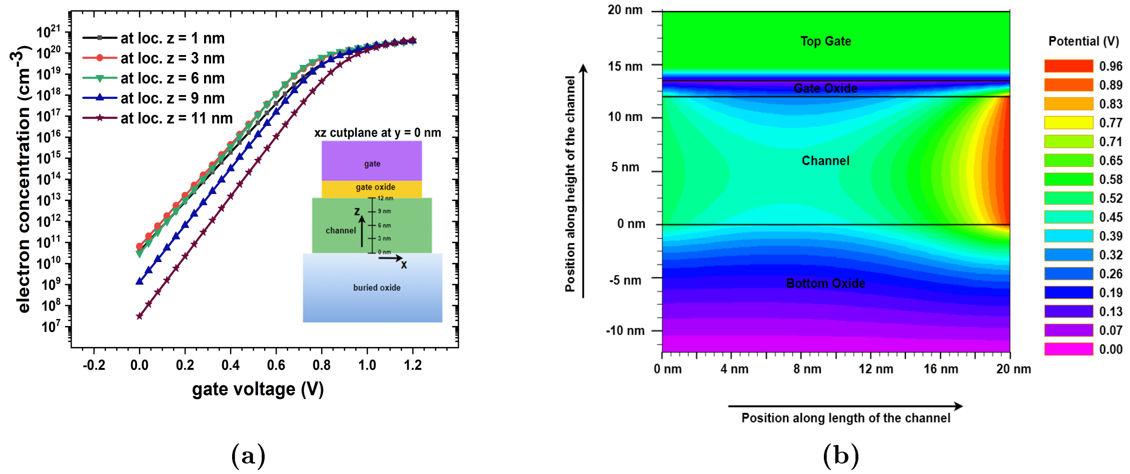
According to Hu et al. Hu *et al.* (2016), this point of maximum potential in the z direction is at the buried oxide-channel interface, i.e. z = 0. Hence while framing the analytical model for potential, the boundary condition (equation (5.8)) was set such that z = 0 was chosen as the point of maximum potential. However, the simulation results in Figure 5.4 (b) show that the maximum potential point is not at z = 0. It is near $z = \frac{H_{\text{fin}}}{2}$. Hence the difference arises between the model and simulation result near z = 0 in Figure 5.4 (b). Anticipating that this is one of the reasons for the model underpredicting V_{th} and SS, a keen investigation is done on the location of the onset of current conduction in a JLFinFET. To validate this finding, extensive simulations

were conducted and the electron concentration and potential profile of the channel of JLFinFET were scrutinized. This is explained in detail in Sub-section 5.3.3.

5.3.3 Location of Onset of Current Conduction in JLFinFET

With the motive of determining the location of onset of current conduction and its dependance on various device parameters, a careful inspection is done on the electron concentration and potential profile distribution in the channel of JLFinFETs with varying structural parameters like t_{ox}, L_g, H_{fin}, T_{fin} etc (Chennamadhavuni *et al.* (2023)). Results from Chennamadhavuni *et al.* (2023) relevant for our discussion are given in this sub-section.

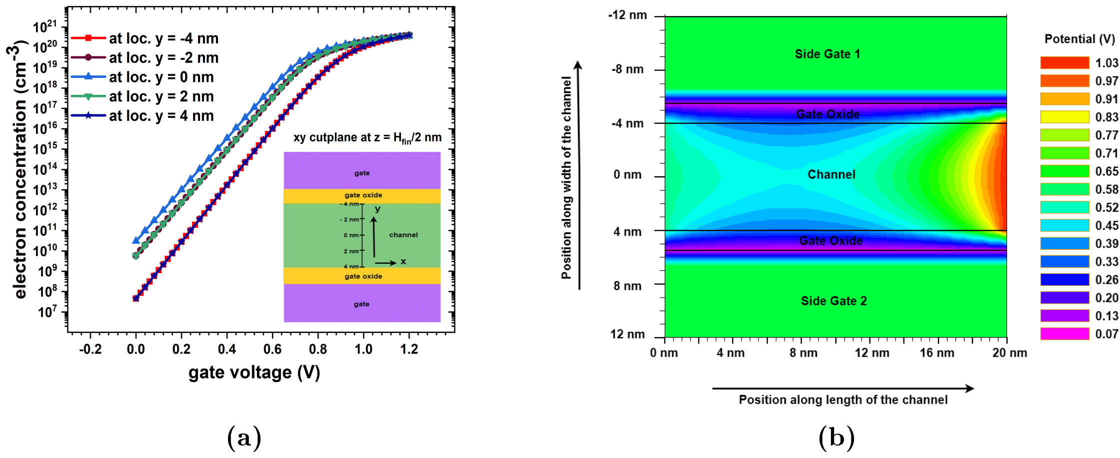


(a) (b)

Figure 5.5: (a) Electron concentration at various z locations (at x = $\frac{L_g}{2}$, y = 0) in the channel with varying gate voltage (at V_{DS} = 0.5 V) and (b) contour plot of channel potential along a cross section in xy plane of JLFinFET, at y = 0 nm (V_{DS} = 0.5 V and V_{GS} = 0.6 V).

Figure 5.5 (a) shows the electron concentration variation with V_{GS}, at z = 1 nm, 3 nm, 6 nm, 9 nm and 11 nm for y = 0 nm and x = 10 nm ($\frac{L_g}{2}$). A cross-sectional view of JLFinFET in xz plane with z locations marked is added as an inset for better clarity. It is visible from Figure 5.5 (a) that, as the gate voltage increases from 0 V and sweeps up, electron concentration towards the middle of the channel (z = 3 nm and 6 nm), is more as compared to buried oxide - channel interface as well as gate oxide - channel interface. However, at higher V_{GS}, electron concentration coincides indicating that the transistor has reached flat band condition. Even the contour plot

of potential along the xz plane located at y = 0 (shown in Figure 5.5 (b)), gives us a clear indication that conduction path formation begins near the mid channel and not at buried oxide - channel interface. Figure 5.6 completes the picture of onset of current conduction in the channel of JLFinFET by giving information on channel formation in a cross sectional cut parallel to xy plane located at z = 6 nm (at $\frac{H_{\text{fin}}}{2}$). Electron concentration at various y locations at x = $\frac{L_{\text{g}}}{2}$ is depicted in Figure 5.6(a), with varying gate voltage.



(a) **(b)**

Figure 5.6: (a) Electron concentration at various y locations (at x = $\frac{L_{\text{g}}}{2}$, z = $\frac{H_{\text{fin}}}{2}$) in the channel with varying gate voltage (at V_{DS} = 0.5 V) and (b) contour plot of channel potential along a cross section of JLFinFET, at z = $\frac{H_{\text{fin}}}{2}$ nm (V_{DS} = 0.5 V and V_{GS} = 0.6 V).

A cross-sectional view along xy cutplane with different y location markings, is added as an inset. Figure 5.6 (b) shows the contour plot of channel potential along xy cutplane at z = 6 nm for V_{DS} = 0.5 V and V_{GS} = 0.6 V. From Figure 5.6 (a) and (b), the obvious scenario of symmetric side gates undepleting the channel from the centre can be visualised. Hence certainly, y = 0 is where the onset of current conduction happens within the channel considering the xy plane. In a nutshell, the findings from Chennamadhavuni *et al.* (2023) portray that when the channel gets narrower, the effective coupling between side gates dominates in a JLFinFET. This weakens the influence of the top gate on the channel. The stronger side gates push the location of the onset of current conduction towards $\frac{H_{\text{fin}}}{2}$. Adding to this explanation from Chennamadhavuni *et al.* (2023), it is clear that for all the device dimensions and

parameters used in this work, the location of the onset of current conduction is closer to z = $\frac{H_{\text{fin}}}{2}$ and not at z = 0.

5.3.4 Model Formulation with Approximations based on the Location of Onset of Current Conduction

In this section, analytical models for threshold voltage and sub-threshold swing are presented taking into account the location where current conduction starts as the gate voltage of the transistor crosses the threshold voltage. These models are based on channel potential model described in Section 5.3.1 given by Hu *et al.* (Hu *et al.* (2016)). The location of minimum channel potential is taken at z = $\frac{H_{\text{fin}}}{2}$ based on results from simulation. This modification on the location of minimum channel potential (location of onset of current conduction) paved way for more accurate threshold voltage and sub-threshold swing model for JLFinFET. A detailed description on this aspect is given in Section. 5.3.4

5.3.4.1 Threshold Voltage

The threshold voltage condition defined in Hu *et al.* (2016, 2014) takes into account the potential at that point in the channel which comes out of depletion first and paves the way for current conduction. This point is located at (1) x = x_{min} where x_{min} is the location corresponding to the minimum most channel potential in the x direction. Hence current conduction path is expected to form between source and drain. (2) y = 0, as this is the farthest location from both side gates in the y direction. Hence undepletion in the y direction happens first at y = 0, causing the formation of a conduction channel, (3) z = z_{max}, is where potential would be maximum in the z direction, undepletion happens first at this location in z direction giving rise to the formation of conduction channel.

As explained in Section 5.3.3, the location of the onset of current conduction in the channel of a JLFinFET is not at the buried oxide - channel interface, but closer to z = $\frac{H_{\text{fin}}}{2}$. While the channel potential model given by Hu *et al.* (2016) deviates from the simulation result at z = 0, it closely predicts the simulation result at z = $\frac{H_{\text{fin}}}{2}$ (shown in Figure 5.4 (b)). This finding lets us incorporate the same channel potential model in Hu *et al.* (2016), for modeling V_{th} in this work.

The threshold voltage condition is based on the location of the onset of current conduction, $\Psi(x_{min}, y_{max}, z_{max})$ (Hu *et al.* (2016)). As per the above explanation, the threshold voltage condition is modified such that, z_{max} is approximated to $\frac{H_{\text{fin}}}{2}$ (indicated by equation (5.21)).

$$\Psi\left(x_{min}, 0, \frac{H_{fin}}{2}\right) = V - 2V_t \qquad ----- \qquad \text{(threshold voltage condition)} \tag{5.21}$$

where x_{min} as given in Ritzenthaler *et al.* (2011) is

$$x_{\text{min}} = \frac{L_{\text{g}}}{2} - \frac{1}{2\pi}\left(\frac{1}{T_{eff}^2} + \frac{0.5}{H_{eff}^2}\right)^{-1/2} \ln\left(1 + V_{DS}/V_R\right) \tag{5.22}$$

It may be noted that the threshold voltage condition given in equation 5.21 comes from the fact that, the threshold voltage is applied to the gate when the channel is in full depletion and therefore 'exp $\left(\frac{\Psi - V}{V_t}\right)$' term in equation 5.1 can be ignored if $\Psi - V = -2V_t$. This definition for threshold voltage condition was proposed in Hu *et al.* (2014). For the ease of solving rather tough equation (5.21), 'n', 'm', 'l' are chosen to be '1'. 'V', which is the quasi Fermi potential is same as the reference voltage (V_R).

Substituting equation 5.21 in equation 5.12, results in equation 5.23.

$$\Psi(x_{min}, 0, \frac{H_{\text{fin}}}{2}) = \frac{V_{DS}}{L_g} x_{min} + A_1(0, \frac{H_{\text{fin}}}{2}) \sin\left(\frac{\pi}{L_g} x_{min}\right) = -2V_t \tag{5.23}$$

where $A_1(0, \frac{H_{\text{fin}}}{2}) = G_1(0, \frac{H_{\text{fin}}}{2}) + \Psi_1$ (referring to equation 5.13).

Substituting $A_1(0, \frac{H_{\text{fin}}}{2})$ in equation 5.23 and simplifying the resulting expression paves way for equation 5.24.

$$V_{GS} - \Psi_{sch} - V_R = \left(\frac{V_{\text{DS}}}{2}\right) + \left(\frac{\frac{-B}{64} + d_1 \cos\left(\frac{0.5\pi H_{fin}}{2h}\right)}{\frac{A}{16\pi} - 4\left(\frac{{k_1}^2}{\pi}\right)\cos\left(\frac{0.5\pi H_{fin}}{2h}\right)}\right) \tag{5.24}$$

Replacing V_{GS} with V_{th} and rearranging equation 5.24, set forth the expression for

threshold voltage, given by equation 5.25.

$$V_{th} = V_R + \Psi_{sch} + \left(\frac{V_{\mathrm{DS}}}{2}\right) - \left(\left(\frac{\pi}{4}\right) * \frac{Q - 64d_1 \cos\left(\frac{0.5\pi H_{\mathrm{fin}}}{2h}\right)}{P - 64\left(k_1{}^2\right)\cos\left(\frac{0.5\pi H_{\mathrm{fin}}}{2h}\right)}\right) \tag{5.25}$$

where

$$P = \pi^4\left(\frac{1}{t^2} + \frac{1}{h^2} + \frac{4}{L_{\mathrm{g}}{}^2}\right) \tag{5.26}$$

and

$$Q = P\frac{\left[2V_t + V_{DS}\frac{x_{\mathrm{min}}}{L_{\mathrm{g}}}\right]}{\sin\left(\frac{\pi x_{\mathrm{min}}}{L_{\mathrm{g}}}\right)}, \tag{5.27}$$

5.3.4.2 Sub-threshold Swing

Sub-threshold swing (SS) is another key parameter to examine the short channel performance of a JLFinFET and hence it is also modeled in this work. SS is defined as Duksh *et al.* (2021)

$$SS = \left(\frac{\partial\left(\log_{10} I_{dsub}\right)}{\partial V_{GS}}\right)^{-1} \tag{5.28}$$

where I_{dsub} is the sub-threshold current. As I_{dsub} is proportional to exponential of potential at the leakiest path in the channel below threshold (i.e. $I_{\mathrm{dsub}} \propto e^{\frac{\Psi\left(x_{min}, 0, \frac{H_{fin}}{2}\right)}{V_{\mathrm{t}}}}$), SS in equation 5.28 becomes

$$SS = 2.3V_t\left(\frac{\partial\Psi\left(x_{min}, 0, H_{fin}/2\right)}{\partial V_{GS}}\right)^{-1} \tag{5.29}$$

After substituting $\Psi\left(x_{min}, 0, H_{fin}/2\right)$ and differentiating the resulting expression with V_{GS}, equation 5.29 simplifies to equation 5.30.

$$SS = \frac{1.81V_t}{\sin\left(\frac{\pi x_{\mathrm{min}}}{L_g}\right)\left(1 - \frac{64cos\left(\frac{0.25\pi H_{\mathrm{fin}}}{h}\right)}{\pi^2\left(\frac{L_g^2}{t^2} + \frac{L_g^2}{h^2} + 4\right)}\right)} \tag{5.30}$$

5.4 Results and Discussion

This section validates the threshold voltage model as well as the sub-threshold swing model derived in Section 5.3.4 using TCAD simulations. In addition, the accuracy of V_{th} and SS models for different channel dimensions is tested and compared with that of already existing V_{th} and SS model Hu *et al.* (2016). The threshold voltage model is then used to compute DIBL at different gate lengths for specified T_{fin} and H_{fin} pairs. Recomputation of published mathematical model as well as computation of modified models (for V_{th} and SS) were done using MATLAB Version: 9.9.0.1467703, R2020b (MathWorks. (2022)).

5.4.1 Validation of modified V_{th} model and comparison of its Accuracy with the Model in Ref. Hu *et al.* (2016)

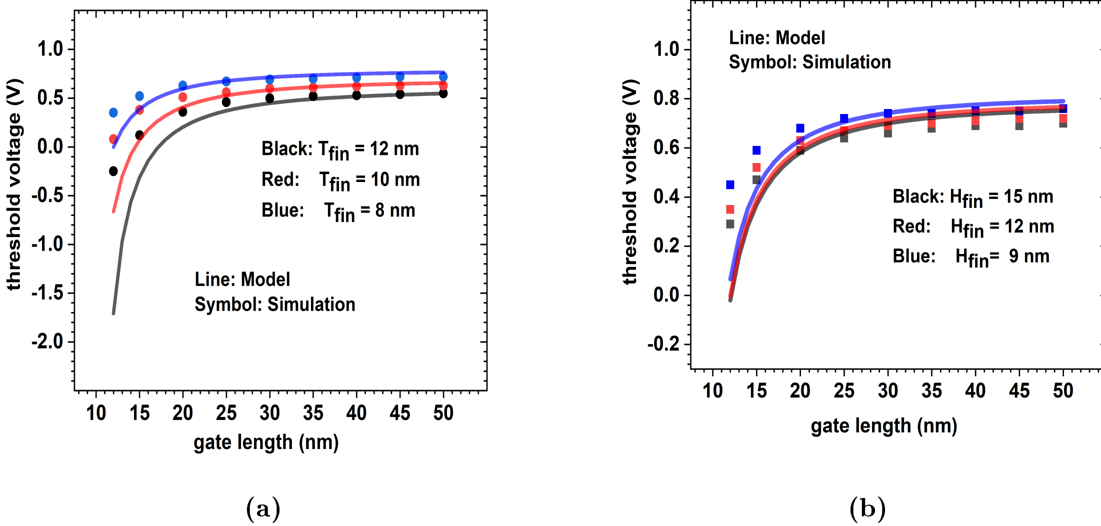


Figure 5.7: Threshold voltage variation with gate length obtained from analytical model in equation 5.25 and TCAD simulation for three different T_{fin} - H_{fin} combinations where (a) H_{fin} is fixed to 12 nm and T_{fin}=(12 nm, 10 nm and 8 nm) and (b) T_{fin} is fixed to 8 nm and H_{fin}=(15 nm, 12 nm and 9 nm), at V_{DS} = 0.5 V.

Figure 5.7 (a) and (b) show the threshold voltage variation with gate length obtained from the analytical model given in equation 5.25 and through simulations performed for devices with varying fin thickness (fixing H_{fin}) and varying fin height (fixing T_{fin})

respectively. It can be observed in Figure 5.7 (a) that the model very well predicts threshold voltage for gate lengths above 20 nm for different cases of fin thickness. However, when the transistor length is scaled down to 20 nm and less, the model underpredicts the threshold voltage. The same trend is observed in Figure 5.7 (b) also. This underprediction of threshold voltage by the analytical model is due to three reasons: (1) threshold voltage expression consists of a double Fourier series inside the coefficient of a single Fourier series. Both the double as well as single Fourier series are truncated to one term expression to reduce the complexity of obtaining closed form expression of threshold voltage. Closely inspecting the nature of the equation representing channel potential gives the idea that gate length (L_g) is in the denominator of Fourier coefficients due to which the impact of truncating Fourier series gets nullified at higher gate lengths. (2) Various physical phenomena that become dominant in lower channel dimensions are not considered while developing the model leading to the analytical model underpredicting threshold voltage at lower channel dimensions. (3) The homogenous cuboidal silicon approximation used to frame boundary conditions becomes inaccurate at very low channel dimensions (sub-20 nm).

Another observation from Figure 5.7 (a) and (b) is that, the reduction in V_{th} with an increase in T_{fin} is more prominent than V_{th} reduction with increase in H_{fin}. This trend in the model can be attributed to the nature of equation 5.25 wherein there are cosine terms dependent only on H_{fin} in the numerator and denominator that are nullifying the variation in V_{th} with H_{fin}. Physically, the dominance of side gates in depleting the thin silicon channel over the top gate is the cause for the greater impact of T_{fin} (compared to H_{fin}) in deciding V_{th}.

The motive of modifying the threshold voltage condition was to reduce the discrepancy between modeled and simulated data in Hu *et al.* (2016). So it is imperative to compare the accuracy of the model in equation (23) with that in Hu *et al.* (2016). For this purpose, the threshold voltage of JLFinFET with gate lengths from 50 nm down to 12 nm was computed using our model as well as the published model. The threshold voltage was also determined through simulations conducted on all the JLFinFETs under study. The difference between simulated threshold voltage (V_{th} sim) and modeled threshold voltage (V_{th} model) was taken and is displayed as bar charts in Figure 5.8 and Figure 5.9. It must be noted that in Figure 5.8, three cases of T_{fin}- H_{fin} were selected such that H_{fin} remains the same in all cases (12 nm) while T_{fin} varies (8 nm,

10 nm and 12 nm).

For Figure 5.9, three cases of T_{fin} - H_{fin} where chosen such that T_{fin} is fixed to 8 nm while H_{fin} varies (9 nm, 12 nm and 15 nm). It is to be pointed out that Figure 5.8 and Figure 5.9 have axis-breaks in the linear vertical axis to accommodate lone bars with values that are far higher than values corresponding to most of the bars. Also T_{fin} and H_{fin} values were chosen around 10 nm considering the present day technology requirements.

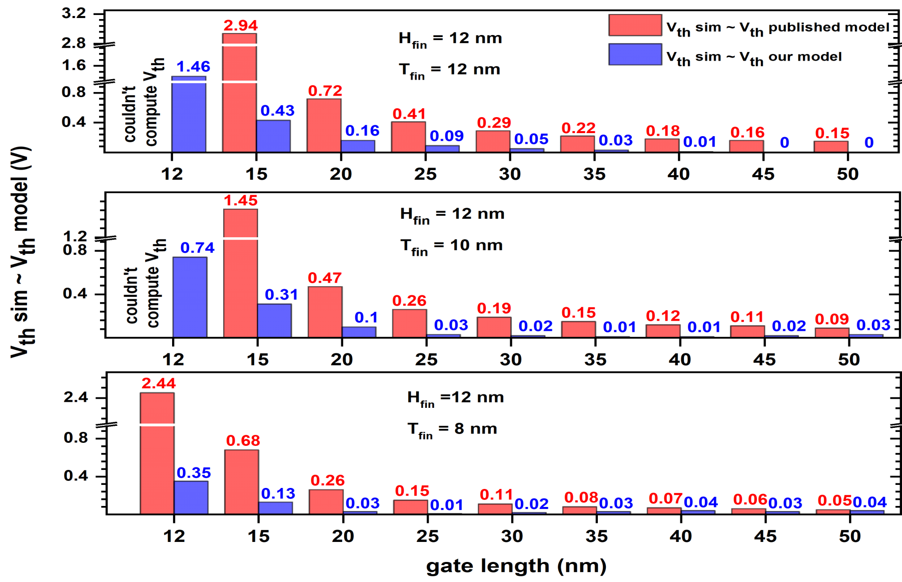


Figure 5.8: Comparison of the accuracy of the model in equation (23) and the model published in Hu *et al.* (2016) for predicting threshold voltage for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that H_{fin} in all cases is fixed to 12 nm while T_{fin} is chosen to vary (12 nm, 10 nm and 8 nm).

Common observation from Figure 5.8 and Figure 5.9 is that for all the cases, the accuracy of our threshold voltage model (blue bars) is better than that of the published model (red bars). Although this improvement in accuracy becomes less visible at higher gate lengths, significant enhancement in accuracy is observed as gate length scales down. Considering the cases in Figure 5.8, it is seen that for gate length as small as 12 nm, our model still predicts threshold voltage with highest possible error of 1.46 V while the published model couldn't compute threshold voltage for two out of three cases of specified T_{fin} - H_{fin} combinations. A point to note here is that there is a trend of improved accuracy for both the published model and our model

with a reduction in T_{fin}. This can be due to the reduction in Fourier series truncation error with decrease in T_{fin}.

Figure 5.9 also shows that our model could predict well, the threshold voltage for gate lengths as small as 20 nm. However for gate length down to 12 nm, maximum error of 0.38 V is observed with our model. Another observation from Figure 5.9 is that, for the published model, accuracy improves with the decrease in H_{fin} due to the reduction in Fourier series truncation error like the case with T_{fin}. Nevertheless, our model accuracy remains almost the same even when H_{fin} is reduced. This is due to the presence of $\cos(\frac{0.5\pi H_{fin}}{2h})$ in the expression for V_{th} which is nullifies the effect of truncation error on accuracy.

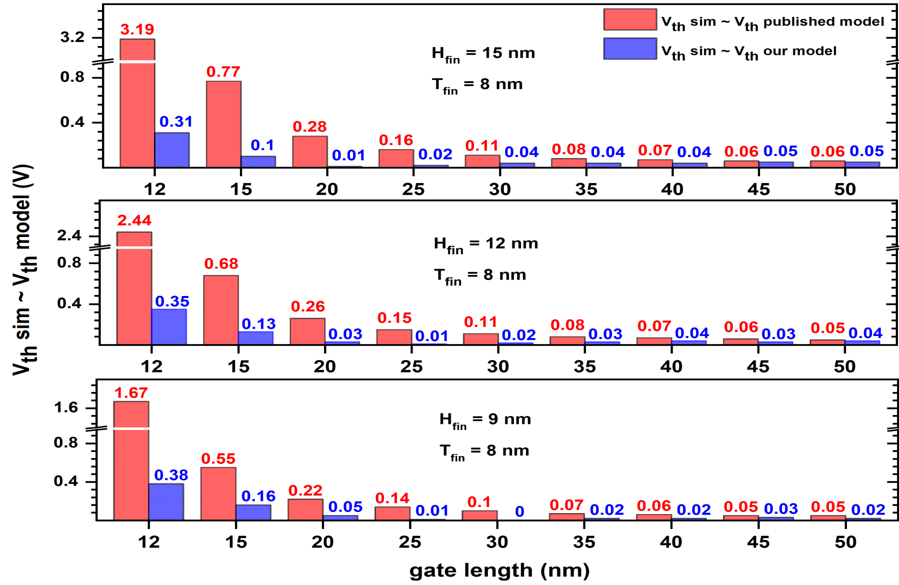


Figure 5.9: Comparison of the accuracy of the model in equation (23) and the model published in Hu *et al.* (2016) for predicting threshold voltage for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that T_{fin} in all cases is fixed to 8 nm while H_{fin} is chosen to vary (15 nm, 12 nm and 9 nm).

5.4.2 Validation of DIBL computed from V_{th} Model using TCAD Simulations

Figure 5.10 shows DIBL variation with gate length for various T_{fin} - H_{fin} combinations. DIBL in Figure 5.10 was computed by determining threshold voltage (given by equation 5.25) at two different drain bias (V_{DS} = 0.5 V and V_{DS} = 0.05 V) and then

evaluating $\frac{\Delta V_{\text{th}}}{\Delta V_{\text{DS}}}$. Degradation in DIBL with a reduction in gate length is visible for all cases in Figure 5.10. This is obvious because, for smaller gate lengths, the channel region lies in closer proximity to the drain terminal and results in greater influence of V_{DS} on threshold voltage, hence greater DIBL. Figure 5.10 (a) and (b) show a reasonably fair match between model and simulation results for $L_g \geq 20$ nm. Nevertheless for $L_g < 20$ nm, DIBL predicted analytically is greater than that obtained through TCAD simulation. This is due to the inaccuracy of the threshold voltage model given by equation 5.25 in the sub-20 nm region.

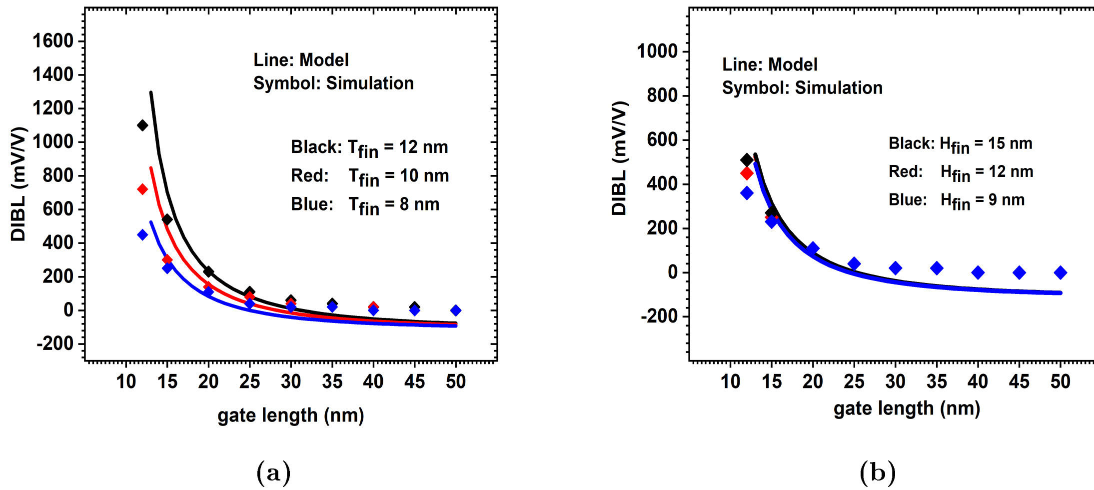


Figure 5.10: DIBL with varying gate length for three different T_{fin} - H_{fin} combinations where (a) H_{fin} is fixed to 12 nm and T_{fin}=(12 nm, 10 nm and 8 nm) and (b) T_{fin} is fixed to 8 nm and H_{fin}=(15 nm, 12 nm and 9 nm).

It is observed in Figure 5.10(a) that DIBL reduces with T_{fin} especially in lower gate lengths as smaller T_{fin} results in greater control of the channel by side gates and thereby channel potential couldn't be influenced to a greater extent by drain bias. However inspecting Figure 5.10(b) shows that, with only H_{fin} variation (i.e constant T_{fin}), there is no variation in DIBL for $L_g \geq 20$ nm while marginal variation is visible for gate length below 20 nm. This is owing to the fact that, when H_{fin} varies, only the top gate's contribution in controlling the channel varies. As the onset of current conduction is located within the bottom half of channel (away from the top gate), the effect of the top gate on channel potential is not significant. Hence reducing H_{fin} does not reduce DIBL to a comparatively greater extent unlike the case with varying T_{fin}.

5.4.3 Validation of modified SS model and comparison of its Accuracy with the Model in Ref. Hu *et al.* (2016)

Figure 5.11 presents the variation of Sub-threshold Swing (SS) with gate length for various T_{fin} - H_{fin} combinations. SS obtained from analytical model (equation (5.30)) and TCAD simulation fairly agree with a negligible error of $\sim 4\ \frac{mV}{dec}$ for $L_g > 20$ nm. Whereas below L_g of 20 nm the analytical model overestimates SS (shown in both Figure 5.11(a) and (b)). The cause of this error can be attributed to Fourier series truncation in the expression of SS in equation 5.30 as well as homogenous cuboidal silicon approximation used while solving Poisson's equation. Like DIBL, reducing T_{fin} has a significant effect in reducing SS (Figure 5.11(a)) while the influence of H_{fin} on SS is marginal (Figure 5.11 (b)). This is due to the side gates (decided by T_{fin}) having more control over the location of the onset of current conduction than the top gate which is governed by H_{fin}.

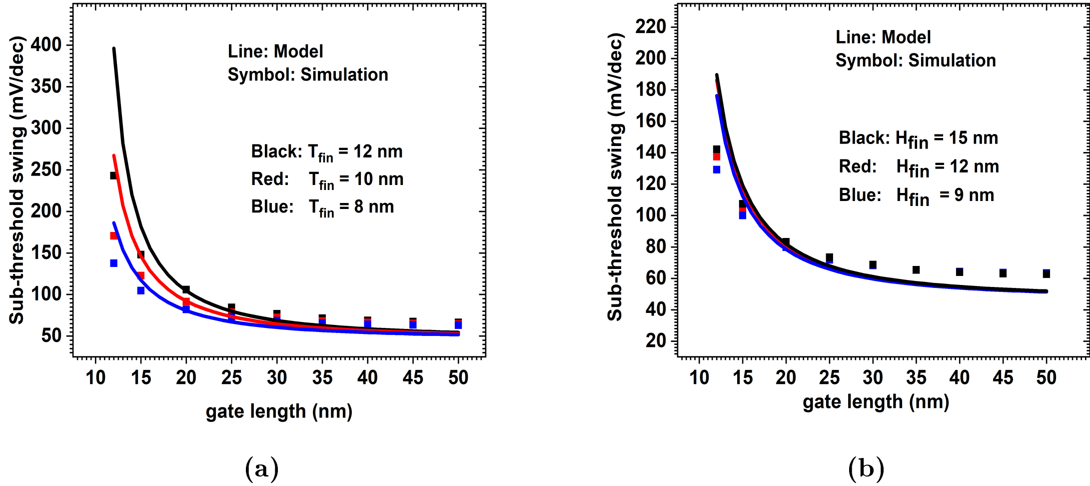


Figure 5.11: SS with varying gate length for three different T_{fin}-H_{fin} combinations where (a) H_{fin} is fixed to 12 nm and T_{fin}=(12 nm, 10 nm and 8 nm) and (b) T_{fin} is fixed to 8 nm and H_{fin}=(15 nm, 12 nm and 9 nm).

The accuracy of the model derived for SS in this work (equation 5.30) is compared with the accuracy of the SS model given in Hu *et al.* (2016). For this analysis, SS determined from equation 5.30 is compared with the equation of SS given in Hu *et al.* (2016) for L_g varying from 12 nm to 50 nm. The difference between SS obtained through TCAD simulation (SS sim) and SS from analytical model (SS model)

is determined and is displayed using bar charts as shown in Figure 5.12 and Figure 5.13. Figure 5.12, handles T_{fin} - H_{fin} combinations with fixed H_{fin} (12 nm) and varying T_{fin} (12 nm, 10 nm and 8 nm) and Figure 5.13 has T_{fin} - H_{fin} pairs with fixed T_{fin} (8 nm) and varying H_{fin} (15 nm, 12 nm and 9 nm).

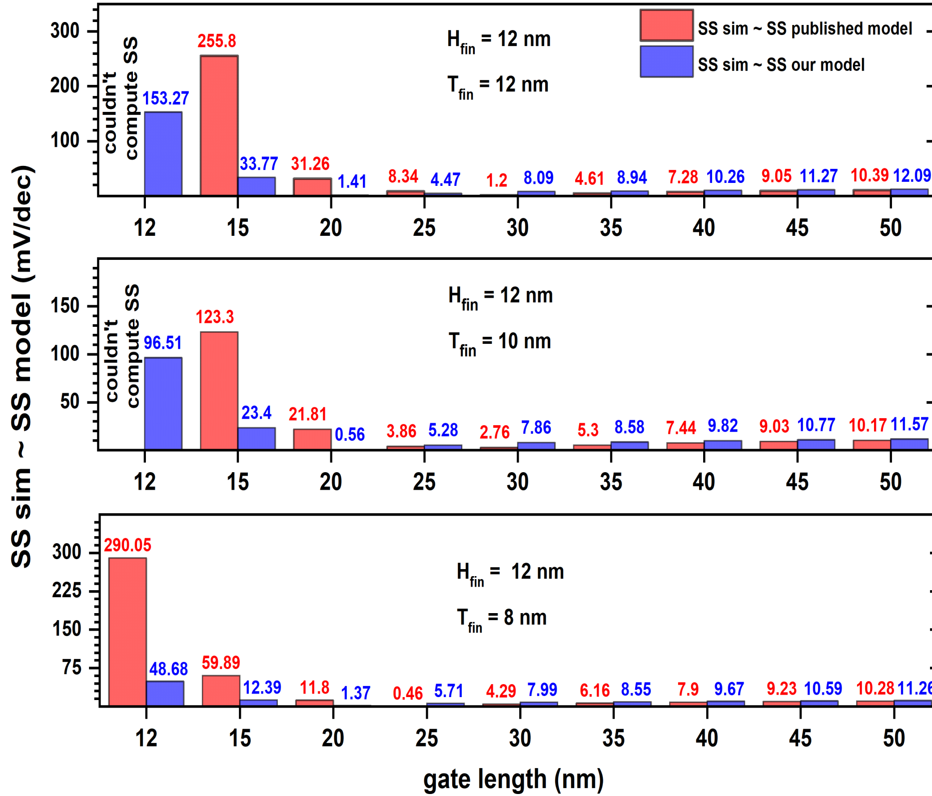


Figure 5.12: Comparison of the accuracy of the model in equation 5.30 and the model published in Hu *et al.* (2016) for predicting sub-threshold swing for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that H_{fin} in all cases is fixed to 12 nm while T_{fin} is chosen to vary (12 nm, 10 nm and 8 nm).

It is observed that for all T_{fin} - H_{fin} combinations in Figure 5.12 and Figure 5.13, our model (blue bars) is more accurate than the published SS model for $L_g \leq 20$ nm. For $L_g > 20$ nm, there is marginal difference in the accuracy of our SS model as well as the published SS model. It is also visible that for certain combinations of T_{fin} - H_{fin}, the published model is incapable of computing SS for gate length as small as 12 nm. Therefore, the model (equation 5.30) developed in this study holds greater relevance for predicting sub-threshold swing, particularly when considering

the transistor dimensions pertinent to the current era.

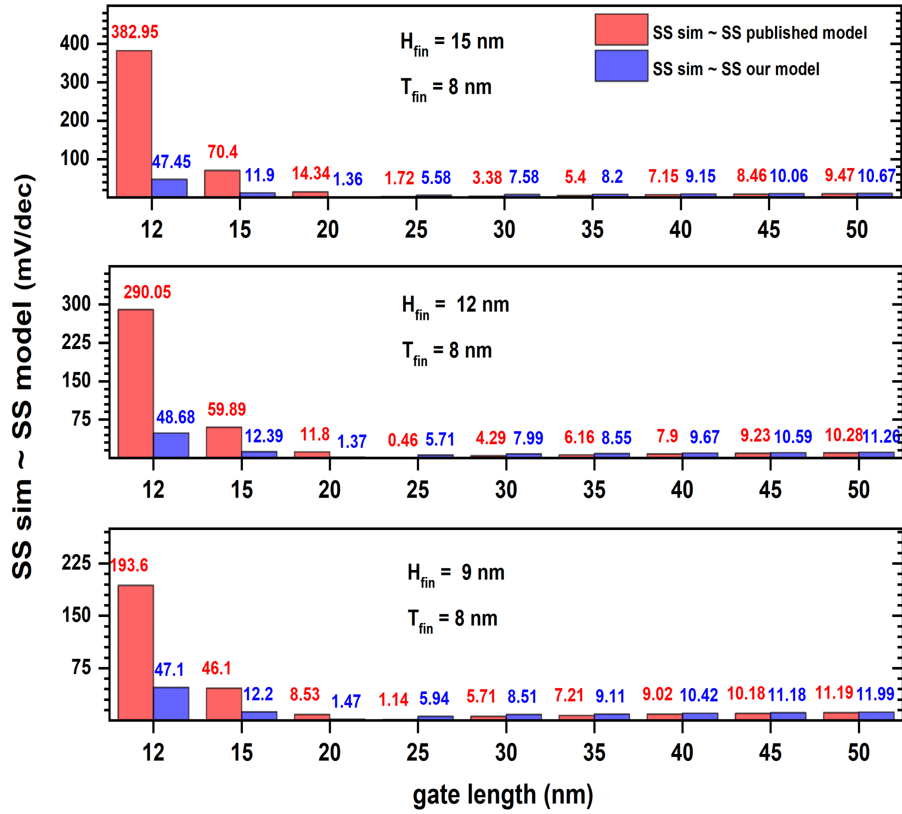


Figure 5.13: Comparison of the accuracy of the model in equation 5.30 and the model published in Hu *et al.* (2016) for predicting sub-threshold swing (SS) for different gate lengths in JLFinFET. Here three T_{fin}-H_{fin} combinations are considered such that T_{fin} in all cases is fixed to 8 nm while H_{fin} is chosen to vary (15 nm, 12 nm and 9 nm).

Validating V_{th} Model Derived in Section 5.3.4.1 with Experimental Data: To examine the trustworthiness of the developed model in determining the threshold voltage of 'real world' JLFinFETs, a comparison is made between the threshold voltage of a fabricated JLFinFET given in Ribeiro *et al.* (2021) as well as that computed by equation 5.25. For a temperature of 300 K and inserting the same parameters as in Ribeiro *et al.* (2021), equation 5.25 gave threshold voltage of 0.4508 V which closely matched with threshold voltage of the fabricated JLFinFET which is 0.45 V. Hence the model derived in Section 5.3.4.1 is capable of determining the threshold voltage of physical transistors.

5.5 Summary

In this chapter, a detailed exploration on the Fourier series based analytical model for SOI JLFinFET was done. A background research done on the location of the onset of current conduction in a SOI JLFinFET reveals that the conduction path in the transistor forms near the middle of channel (closer to $\frac{H_{\text{fin}}}{2}$ and not at the buried oxide - channel interface) for device dimensions considered in this work. While framing the threshold voltage model, the z coordinate of that point in the channel which gets undepleted first is chosen to be $\frac{H_{\text{fin}}}{2}$. The model then obtained, gave a better accuracy than the published model Hu *et al.* (2016), especially for lower gate lengths. The highest possible error with the V_{th} model derived in this article was 1.46 V as opposed to 3.19 V error from the published model. It is observed that T_{fin} has a dominant influence on V_{th}, DIBL and SS than H_{fin}. Alongside the threshold voltage model, analytical model was developed for SS as well. SS model had also shown a fair degree of match with the simulated result except at gate lengths below 20 nm. However, the SS model derived in this work could predict the simulated SS with better accuracy than the published SS model (Hu *et al.* (2016)) for gate lengths equal to or less than 20 nm.

Chapter 6

Fourier series-based analytical model for channel potential and threshold voltage in Dual Material Gate SOI Junctionless FinFET

6.1 Introduction

In Chapter 5, a robust threshold voltage model was developed for Single Material Gate Junctionless FinFET by incorporating suitable assumptions and approximations based on the location of onset of current conduction. This model could predict measured V_{th} of a fabricated SMG JLFinFET (Ribeiro *et al.* (2021)) with very good accuracy. It was observed in many articles available in the literature that Dual Material Gate Junctionless transistors outperformed Single Material Gate transistors in terms of DC characteristics, analog and RF performance metrics, and short channel effects (Baruah and Paily (2013*a*), Lou *et al.* (2012)). Hence this gave the motivation to extend the Fourier series based V_{th} model for Single Material Gate JLFinFET to Dual Material Gate JLFinFET. As per the findings of Chapter 3 better performance is exhibited by DMG JLFinFETs when the work function of gate material near the source is greater than that near the drain. Hence in this chapter, the gate materials of DMG JLFinFET

are chosen such that the material closer to the source always has greater work function compared to the material closer to the drain. The operating regions and transistor behaviour depend primarily on the gate material with higher work function, which is situated near the source. Hence this material is termed as control gate. The gate material with lower work function which is near the drain absorbs the field from the drain terminal. It screens the channel material beneath the control gate from the drain field. It is therefore termed as the screen gate.

In this Chapter, Section 6.2 presents the 3-D structure of DMG JLFinFET listing all the default device parameters used along with details of various models activated while simulating the structure. Section 6.3 presents in detail, the analytical model formulation of the channel potential of a DMG JLFinFET. Section 6.4 examines the robustness of the derived model by comparing the channel potential variation obtained through model and simulation results for multiple DMG JLFinFETs each differing from one another in terms of device parameters like $\mathrm{L_g}$, $\mathrm{H_{fin}}$, $\mathrm{T_{fin}}$, ϕ_c (work function of control gate), ϕ_s (work function of screen gate) etc. Section 6.5 discusses the location of the onset of current conduction in DMG JLFinFET and thereby derives an analytical model for $\mathrm{V_{th}}$ of DMG JLFinFET. Validation of the $\mathrm{V_{th}}$ model with the help of TCAD simulations for various DMG JLFinFETs with different device parameters is handled in Section 6.6. Section 6.7 gives a brief discussion of various sources of error that lead to the $\mathrm{V_{th}}$ model derived in this chapter mispredicting the $\mathrm{V_{th}}$ obtained through simulation for certain cases in DMG JLFinFETs. Section 6.8 summarises the chapter by presenting key findings in brief.

6.2 Device Structure and Simulation Conditions

Figure 6.1 shows the 3-D schematic view of a JLFinFET with SOI substrate having a Dual Material Gate. Table 6.1 gives the default dimensions and other device parameters chosen for DMG JLFinFET in this chapter. All device simulations were conducted using ATLAS 3-D device simulator (Version: 5.2.23.R) by Silvaco.Inc (Manual (2016*b*)). To accurately capture the electrical characteristics exhibited by DMG JLFinFET various models relevant to sub-50 nanometre transistors were included during simulations. Schockley-Read-Hall (SRH) recombination model, field-dependent mobility model, band-to-band tunneling model and impact ionization model were activated. As this study involves transistors with sub-10 nanometre dimensions as

well, quantum model namely the Drift Diffusion Mode Space model coupled with Schrodinger-Poisson's equation was used. The calibrated simulation set-up used in Chapter 5, was used for this chapter also.

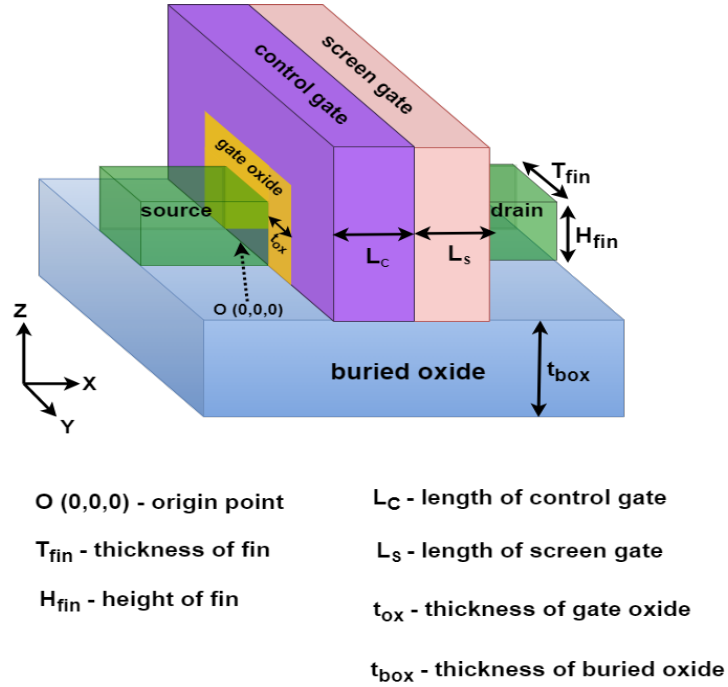


Figure 6.1: 3-D structure of DMG JLFinFET on SOI substrate.

Table 6.1: Device Parameters

Parameter	Value
Temperature	300 K
Channel length of control gate	15 nm
Channel length of screen gate	15 nm
Fin height	12 nm
Fin width	8 nm
Work function of control gate	5.25 eV
Work function of screen gate	4.6 eV
Gate oxide thickness	1.5 nm
Gate oxide material	SiO_2
Buried oxide thickness	12 nm
Buried oxide material	SiO_2
Channel doping concentration	10^{19} cm^{-3}

Table 6.2: Co-ordinate information

Coordinate	Location
x = 0	source end
x = L_g	drain end
x = L_c	control gate/screen gate interface
y = 0	mid-channel
y = $\dfrac{-T_{\text{fin}}}{2}$	channel/side gate oxide interface
y = $\dfrac{T_{\text{fin}}}{2}$	channel/side gate oxide interface
z = 0	channel/buried oxide interface
z = H_{fin}	channel/top gate oxide interface

Table 6.2 enlists the coordinate points corresponding to various parts of the transistor. The cuboidal channel spans across $0 \leq x \leq L_g$; $\dfrac{-T_{\text{fin}}}{2} \leq y \leq \dfrac{T_{\text{fin}}}{2}$; $0 \leq z \leq H_{\text{fin}}$. The origin point O (0,0,0) is marked in Figure 6.1. The coordinates of the y-z plane that cuts the cuboidal channel into two regions (region 'C': below control gate, region 'S': below screen gate) are $x = L_C$; $\dfrac{-T_{\text{fin}}}{2} \leq y \leq \dfrac{T_{\text{fin}}}{2}$; $0 \leq z \leq H_{\text{fin}}$.

6.3 Model for channel potential of DMG JLFinFET

In this section, an analytical expression for the channel potential of Dual Material Gate Junctionless FinFET is derived. To obtain an analytical expression for the channel potential of DMG JLFinFET in the sub-50 nm range, solving 3-D Poisson's equation in the channel is necessary. 3-D Poisson's equation for the channel of DMG JLFinFET in Cartesian x-y-z coordinate system is given by equation 6.1.

$$\frac{\partial^2\Psi(x,y,z)}{\partial x^2}+\frac{\partial^2\Psi(x,y,z)}{\partial y^2}+\frac{\partial^2\Psi(x,y,z)}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}}\left[1-\exp\left(\frac{\Psi(x,y,z)-V}{V_t}\right)\right] \quad (6.1)$$

The channel region of a DMG JLFinFET can be divided into two regions, region 'C' which is the cuboidal region beneath the control gate and region 'S' which is the cuboidal region beneath the screen gate. Channel potential corresponding to each of these regions will be different owing to the difference in the work function of the gate materials located above them. In this work, the channel potential function for region 'C' and region 'S' is denoted as $\Psi_c(x,y,z)$ and $\Psi_s(x,y,z)$ respectively. This chapter focuses on deriving closed form channel potential model in the sub-threshold

and near-threshold region of operation leading to a closed form of expression for V_{th}. Hence depletion approximation remains valid and equation 6.1 simplifies to equation 6.2.

$$\frac{\partial^2\Psi(x,y,z)}{\partial x^2}+\frac{\partial^2\Psi(x,y,z)}{\partial y^2}+\frac{\partial^2\Psi(x,y,z)}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}} \tag{6.2}$$

Boundary conditions to solve the 3-D differential equation given in equation 6.2 are discussed below. It has to be noted that for the DMG JLFinFET modeled in this chapter, the source as well as drain extension regions are not considered.

Boundary conditions for region 'C':

$$\Psi_c(0,y,z)=V_R \tag{6.3}$$

where V_R is the reference voltage present at the source terminal.

$$\Psi_c(L_c,y,z)=V_m(y,z) \tag{6.4}$$

where V_m is the voltage across y-z interface plane between region 'C' and region 'S' in the channel.

Owing to the asymmetrical structure of FinFET an approximation well explained in Pei *et al.* (2002) is incorporated for framing the boundary conditions for DMG JLFinFET. This homogenous silicon cuboidal approximation) is adopted for Single Material Gate JLFinFET and is discussed in detail in Chapter 5. With homogenous silicon cuboidal approximation, the cuboidal silicon block has an effective thickness (T_{eff}) and effective height (H_{eff}) such that symmetric cases could be included in boundary conditions.

$$\Psi_c\left(x,T_{eff}/2,z\right)=V_{GS}-\Psi_{sch_c} \tag{6.5}$$

$$\Psi_c\left(x,-T_{eff}/2,z\right)=V_{GS}-\Psi_{sch_c} \tag{6.6}$$

$$\Psi_c\left(x,y,H_{eff}\right)=V_{GS}-\Psi_{sch_c} \tag{6.7}$$

$$\left.\frac{\partial\Psi_c}{\partial z}\right|_{z=0}=0 \tag{6.8}$$

$$\Psi_c\left(x,y,-H_{eff}\right)=V_{GS}-\Psi_{sch_c} \tag{6.9}$$

Equation 6.5, 6.6, 6.7 and 6.9 denotes the potential at four faces of silicon cuboidal channel beneath the control gate, considering the homogenous silicon cuboidal approx-

imation. Ψ_{sch_c} is the control gate Schottky barrier voltage. T_{eff} and H_{eff} expressions from Pei *et al.* (2002) are given in equation 6.10 and 6.11 respectively.

$$T_{eff} = \sqrt{T_{fin}\left(T_{fin} + 4t_{ox}\varepsilon_{si}/\varepsilon_{ox}\right)} \tag{6.10}$$

$$H_{eff} = \sqrt{H_{fin}\left(H_{fin} + 2t_{ox}\varepsilon_{si}/\varepsilon_{ox}\right)} \tag{6.11}$$

Equation 6.8 stems from the assumption that the parabolically varying channel potential in z-direction is maximum at z = 0.

Solution for $\Psi_c(x, y, z)$

With the above mentioned boundary conditions for region 'C', 3-D Poisson's equation (6.2) is solved and channel potential for region 'C' is given by equation 6.12. Technique of directly solving 3-D Poisson's equation, adopted in this chapter is taken from Hu *et al.* (2016).

$$\Psi_c(x, y, z) = V_R + \left(\frac{V_m - V_R}{L_c}\right)x + \sum_{n=1}^{\infty} A_{n_c}(y, z)\sin\left(\frac{n\pi x}{L_c}\right) \tag{6.12}$$

where

$$A_{n_c}(y, z) = G_{n_c}(y, z) + \Psi_{n_c} \tag{6.13}$$

$$G_{n_c}(y, z) = \sum_{m=1}^{\infty}\sum_{l=1}^{\infty} g_{ml_c}(n)\cos\left[\frac{(m-0.5)\pi}{t}y\right]\cos\left[\frac{(l-0.5)\pi}{h}z\right] \tag{6.14}$$

$$g_{ml_c}(n) = \frac{(-1)^{m+l+1}4\left(d_n + k_{n_c}^2\Psi_{n_c}\right)}{(m-0.5)(l-0.5)\pi^4\left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{L_c{}^2}\right]} \tag{6.15}$$

$$\Psi_{n_c} = \frac{2}{n\pi}\left\{(V_{GS} - \Psi_{sch_c} - V_R)\left(1 - (-1)^n\right) + (V_m - V_R)(-1)^n\right\} \tag{6.16}$$

$$k_{n_c} = \frac{n\pi}{L_c} \tag{6.17}$$

$$d_n = \frac{2qN_d}{n\pi\epsilon_{si}}[(-1)^n - 1] \tag{6.18}$$

$$t = \frac{T_{eff}}{2} \tag{6.19}$$

$$h = H_{eff} \tag{6.20}$$

m, n, l = 1, 2, 3....

Boundary conditions for region 'S':

$$\Psi_s(L_c + L_s, y, z) = V_R + V_{DS} \tag{6.21}$$

Equation 6.21 represents boundary condition at drain terminal.

$$\Psi_s(L_c, y, z) = V_m \tag{6.22}$$

as V_m is the voltage at the interface plane between region 'C' and region 'S' in the channel.

$$\Psi_s\left(x, T_{eff}/2, z\right) = V_{GS} - \Psi_{sch_s} \tag{6.23}$$

$$\Psi_s\left(x, -T_{eff}/2, z\right) = V_{GS} - \Psi_{sch_s} \tag{6.24}$$

$$\Psi_s\left(x, y, H_{eff}\right) = V_{GS} - \Psi_{sch_s} \tag{6.25}$$

$$\left.\frac{\partial \Psi_s}{\partial z}\right|_{z=0} = 0 \tag{6.26}$$

$$\Psi_s\left(x, y, -H_{eff}\right) = V_{GS} - \Psi_{sch_s} \tag{6.27}$$

Equation 6.23, 6.24, 6.25 and 6.27 denotes the potential at four faces of silicon cuboidal channel beneath the screen gate, considering the homogenous silicon cuboidal approximation. Ψ_{sch_s} is the screen gate Schottky barrier voltage.

Solution for $\Psi_s(x, y, z)$

With the boundary conditions for region 'S', 3-D Poisson's equation (6.2) is solved and the channel potential for region 'S' is given by equation 6.28.

$$\Psi_s(x,y,z) = V_m + \left(\frac{V_R + V_{DS} - V_m}{L_\mathrm{s}}\right)(x - L_\mathrm{c}) + \sum_{n=1}^{\infty} A_{n_s}(y,z)\sin\left(\frac{n\pi}{L_\mathrm{s}}(x - L_\mathrm{c})\right) \tag{6.28}$$

where

$$A_{n_s}(y,z) = G_{n_s}(y,z) + \Psi_{n_s} \tag{6.29}$$

$$G_{n_s}(y,z) = \sum_{m=1}^{\infty}\sum_{l=1}^{\infty} g_{ml_s}(n)\cos\left[\frac{(m-0.5)\pi}{t}y\right]\cos\left[\frac{(l-0.5)\pi}{h}z\right] \tag{6.30}$$

$$g_{ml_s}(n) = \frac{(-1)^{m+l+1}4\left(d_n + k_{n_s}^2\Psi_{n_s}\right)}{(m-0.5)(l-0.5)\pi^4\left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{{L_\mathrm{s}}^2}\right]} \tag{6.31}$$

$$\Psi_{n_s} = \frac{2}{n\pi}\left\{(V_{GS} - \Psi_{sch_s} - V_m)\left(1 - (-1)^n\right) + (V_R + V_{DS} - V_m)(-1)^n\right\} \tag{6.32}$$

$$k_{n_s} = \frac{n\pi}{L_\mathrm{s}} \tag{6.33}$$

where d_n, t and h are given by equation 6.18, 6.19 and 6.20 respectively.
m, n, l = 1, 2, 3....
It must be noted that V_m term in both $\Psi_c(x,y,z)$ and $\Psi_s(x,y,z)$ is unknown. Inorder to obtain a complete model for channel potential of a DMG JLFinFET, it is crucial to derive an expression for the interface voltage V_m. In a DMG JLFinFET, additional boundary conditions are available which can be used to derive V_m. These additional boundary conditions stem from the fact that
(a) channel potential is continuous at region 'C' - region 'S' interface (equation 6.34),
(b) electric flux is continuous at region 'C' - region 'S' interface (equation 6.35),

$$\Psi_c(L_c,y,z) = \Psi_s(L_c,y,z) \tag{6.34}$$

$$\left.\frac{\partial \Psi_c(x,y,z)}{\partial x}\right|_{x=L_c} = \left.\frac{\partial \Psi_s(x,y,z)}{\partial x}\right|_{x=L_c} \tag{6.35}$$

Hence, from equation 6.34 and 6.35, $\mathrm{V_m}$ can be derived.

Determination of $\mathrm{V_m}$

$\mathrm{V_m}$(y,z) is the potential along y-z plane in the channel located at x = $\mathrm{L_c}$. Equation 6.34 can also be written as equation 6.36.

$$V_{\mathrm{m}} = \Psi_c(L_c, y, z) = \Psi_s(L_c, y, z) \tag{6.36}$$

Substituting $\Psi_c(x,y,z)$ from equation 6.12 and $\Psi_s(x,y,z)$ from equation 6.28 into equation 6.35, we obtain equation 6.37

$$\frac{V_m - V_R}{L_{\mathrm{c}}} + \sum_{n=1}^{\infty} A_{n_c}(y,z)\left(\frac{n\pi}{L_{\mathrm{c}}}\right)(-1^n) = \frac{V_R + V_{DS} - V_m}{L_{\mathrm{s}}} + \sum_{n=1}^{\infty} A_{n_s}(y,z)\left(\frac{n\pi}{L_{\mathrm{s}}}\right) \tag{6.37}$$

Rearranging equation 6.37, we obtain equation 6.38.

$$V_m = \frac{V_R + V_{DS}}{L_s} + \frac{V_R}{L_c} + \frac{\sum_{n=1}^{\infty}\left(A_{n_s}(y,z)\dfrac{n\pi}{L_s} - A_{n_c}(y,z)\dfrac{n\pi}{L_c}(-1^n)\right)}{\dfrac{1}{L_c} + \dfrac{1}{L_s}} \tag{6.38}$$

Substituting the expression for $A_{n_c}(y,z)$ and $A_{n_s}(y,z)$ in 6.38 and rearranging gives the expression for $\mathrm{V_m}$ given by equation 6.39

$$V_m = \frac{\dfrac{V_R + V_{DS}}{L_s} + \dfrac{V_R}{L_c} + N_s - N_c}{\dfrac{1}{L_c} + \dfrac{1}{L_s} + D_c + D_s} \tag{6.39}$$

where

$$N_c = \sum_{n=1}^{\infty}\left[(\beta_c + \alpha_c)(-1^n)\frac{n\pi}{L_c}\right] \tag{6.40}$$

$$N_s = \sum_{n=1}^{\infty}\left[(\beta_s + \alpha_s)\frac{n\pi}{L_s}\right] \tag{6.41}$$

$$D_c = \sum_{n=1}^{\infty} \left[\left(\frac{2}{n\pi} + \Gamma_c \right) \frac{n\pi}{L_c} \right] \tag{6.42}$$

$$D_s = \sum_{n=1}^{\infty} \left[\left(\frac{2}{n\pi} + \Gamma_s \right) \frac{n\pi}{L_s} \right] \tag{6.43}$$

$$\beta_c = \frac{2}{n\pi} \left\{ \left(V_{GS} - \Psi_{sch_c} \right) \left(1 - (-1)^n \right) + \left(-V_R \right) \right\} \tag{6.44}$$

$$\beta_s = \frac{2}{n\pi} \left\{ \left(V_{GS} - \Psi_{sch_s} \right) \left(1 - (-1)^n \right) + (V_R + V_{DS})(-1^n) \right\} \tag{6.45}$$

$$\alpha_c = \sum_{m=1}^{\infty} \sum_{l=1}^{\infty} \frac{(-1)^{m+l+1} 4 \left(d_n + k_{n_c}^2 \beta_c \right) \cos[\frac{(m-0.5)\pi}{t} y] \cos[\frac{(l-0.5)\pi}{h} z]}{(m-0.5)(l-0.5)\pi^4 \left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{{L_c}^2} \right]} \tag{6.46}$$

$$\alpha_s = \sum_{m=1}^{\infty} \sum_{l=1}^{\infty} \frac{(-1)^{m+l+1} 4 \left(d_n + k_{n_s}^2 \beta_s \right) \cos[\frac{(m-0.5)\pi}{t} y] \cos[\frac{(l-0.5)\pi}{h} z]}{(m-0.5)(l-0.5)\pi^4 \left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{{L_s}^2} \right]} \tag{6.47}$$

$$\Gamma_c = \sum_{m=1}^{\infty} \sum_{l=1}^{\infty} \frac{(-1)^{m+l+1} 4 (\frac{2}{n\pi})(k_{n_c})^2 \cos[\frac{(m-0.5)\pi}{t} y] \cos[\frac{(l-0.5)\pi}{h} z]}{(m-0.5)(l-0.5)\pi^4 \left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{{L_c}^2} \right]} \tag{6.48}$$

$$\Gamma_s = \sum_{m=1}^{\infty} \sum_{l=1}^{\infty} \frac{(-1)^{m+l+1} 4 (\frac{2}{n\pi})(k_{n_s})^2 \cos[\frac{(m-0.5)\pi}{t} y] \cos[\frac{(l-0.5)\pi}{h} z]}{(m-0.5)(l-0.5)\pi^4 \left[\frac{(m-0.5)^2}{t^2} + \frac{(l-0.5)^2}{h^2} + \frac{n^2}{{L_s}^2} \right]} \tag{6.49}$$

Closed form of solution for $\Psi(x, y, z)$

V_m from equation 6.39 is substituted in equation 6.12 and equation 6.28 to obtain exclusive expressions for $\Psi_c(x, y, z)$ and $\Psi_s(x, y, z)$ respectively. The final expression

for channel potential $\Psi(x, y, z)$ is obtained by substituting the resultant $\Psi_c(x, y, z)$ and $\Psi_s(x, y, z)$ in equation 6.50.

$$\Psi(x, y, z) = \begin{cases} \Psi_c(x, y, z) & \text{for } 0 \leq x \leq L_c \\ \Psi_s(x, y, z) & \text{for } L_c \leq x \leq L_c + L_s \end{cases} \tag{6.50}$$

6.4 Validation of Channel Potential Model with TCAD simulation

Results presented in this section, validates the analytical model derived for channel potential in Section 6.3 with TCAD simulation. The models derived are coded and results are generated using MATLAB Version: 9.9.0.1467703, R2020b (MathWorks. (2022)). To examine the robustness of the derived channel potential model in equation 6.50, the degree of match between the channel potential model and potential from simulation for varying device parameters and at various locations in the channel was analysed. Default values of V_{GS} and V_{DS} taken throughout the analysis are 0.3 V and 0.5 V respectively. These values were selected to ensure that all the DMG JLFinFETs considered in this section are either in the sub-threshold or near-threshold region of operation. This is because the channel potential model discussed in this article is applicable for the sub-threshold as well as near-threshold regions of operation only.

6.4.1 Channel Potential Variation along X Direction with Device Parameter Change

In this sub-section channel potential variation along x direction (source to drain) in the middle of channel (y = 0 and z = $\frac{H_{\text{fin}}}{2}$) is analysed for different groups of DMG JLFinFETs where in each group, one of the device parameters vary across the transistors. This gives us an insight into the capability of the derived model in predicting channel potential in DMG JLFinFETs with different device parameters. These results also give an idea of the range of these parameters within which the model is suitable.

Figure 6.2 presents the variation in channel potential from source to drain along a cutline in the middle of the cuboidal channel (along x direction at y = 0, z = $\frac{H_{\text{fin}}}{2}$) of DMG JLFinFETs with L_g of 20 nm, 30 nm and 50 nm. Figure 6.2 shows fair match between model and simulation results for three different channel lengths.

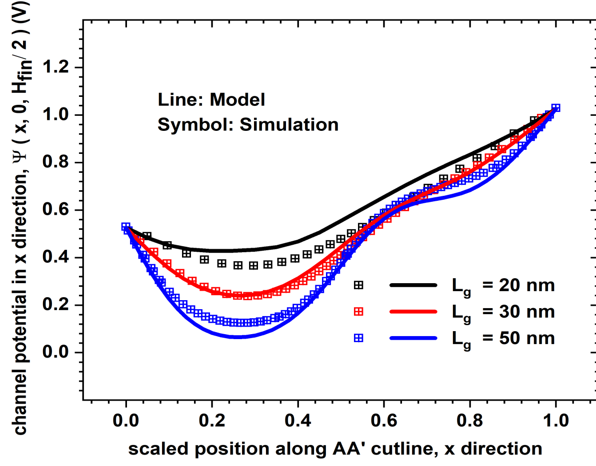


Figure 6.2: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different channel lengths, L_g = 20 nm, 30 nm and 50 nm.

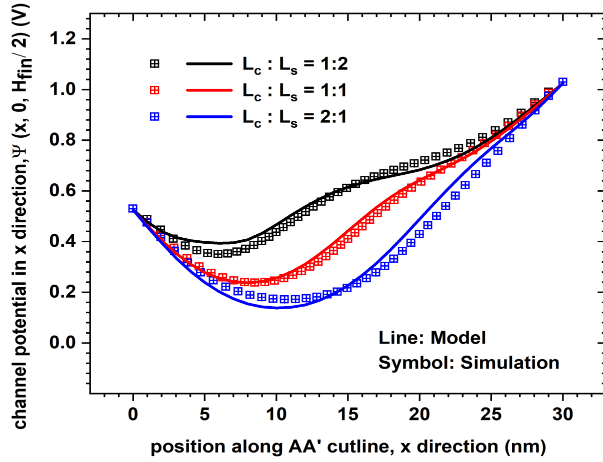


Figure 6.3: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$) in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different channel length ratios, L_c : L_s = 1:2, 1:1 and 2:1.

Figure 6.3 shows the channel potential variation from source to drain in DMG JLFinFETs, each having different L_c : L_s ratios. The channel potential model derived in this chapter shows a good match with simulation results when the control gate-screen gate length ratio is varied. As expected when the region 'C' - region 'S' interface

moves away from the drain, step change in potential at the interface becomes more visible (black curve representing L_c:L_s is 1:2).

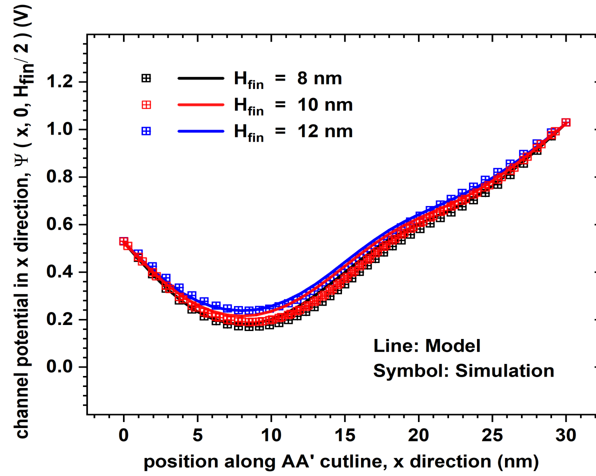


Figure 6.4: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different fin heights, H_{fin} = 8 nm, 10 nm and 12 nm.

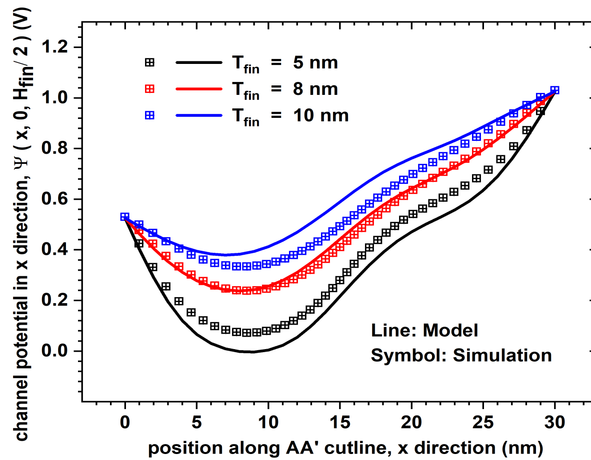


Figure 6.5: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different fin widths, T_{fin} = 5 nm, 8 nm and 10 nm.

Figure 6.4 puts forth the variation of channel potential along x direction (from

source to drain) in DMG JLFinFETs having different fin heights (H_{fin} = 8 nm, 10 nm and 12 nm). It is evident from Figure 6.4 that there is a close match between the channel potential values calculated using analytical model and numerical simulation. As the height of the fin increases, the influence of the top gate on the channel reduces and the channel gets undepleted fast when V_{GS} increases. Hence the curve shifts up closer to reference voltage (V_R) as H_{fin} increases.

Potential variation from source to drain in the mid-channel for DMG JLFinFETs with three different fin width (T_{fin} = 5 nm, 8 nm and 10 nm) is shown in Figure 6.5. As the width of the fin increases, the effect of side gates on the channel reduces. Hence channel comes out of depletion faster in wider channel transistors (T_{fin} = 10 nm) and channel potential rises towards reference voltage (V_R).

Figure 6.6 shows the variation of channel potential in x direction from source to drain in DMG JLFinFETs having three different gate voltages (V_{GS} = 0.1 V, 0.3 V and 0.5 V). V_{DS} for all these transistors is fixed to 0.5 V. With increase in V_{GS} the potential curve shifts upwards indicating that the entire channel is coming out of depletion. There is an excellent match between the mathematical model and TCAD simulation data for channel potential as shown in Figure 6.6.

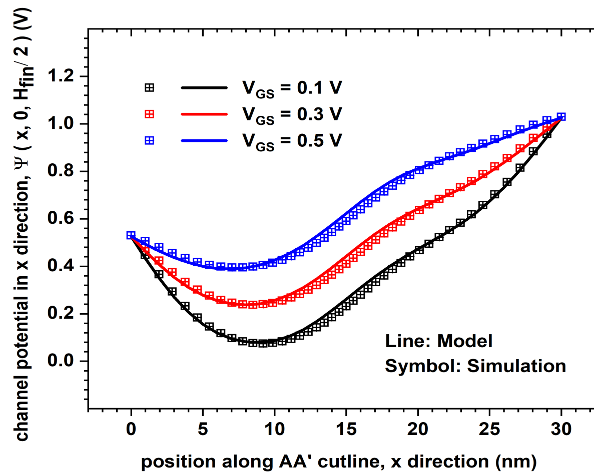


Figure 6.6: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{fin}}{2}$ in DMG JLFinFET with V_{DS} = 0.5 V, for three different gate voltages ,V_{GS} = 0.1 V, 0.3 V and 0.5 V.

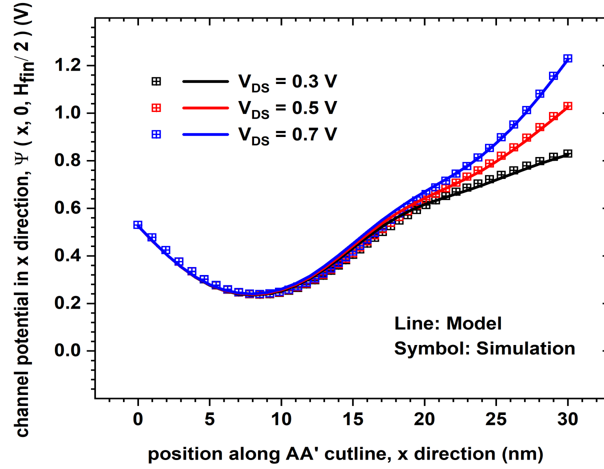


Figure 6.7: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V, for three different drain voltages, V_{DS} = 0.3 V, 0.5 V and 0.7 V.

Channel potential of DMG JLFinFETs in the x direction (from source to drain) under three different V_{DS} is shown in Figure 6.7. It can be observed that as drain bias increase, minimum channel potential is almost equal. This indicates that the screen gate is able to suppress the effect of drain bias on minimum potential point.

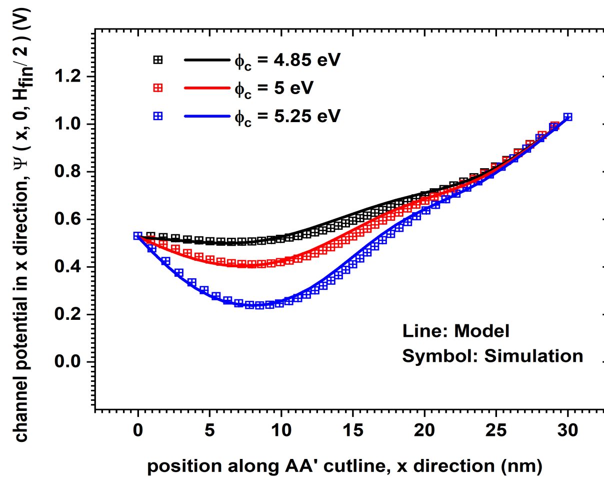


Figure 6.8: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different control gate work functions, ϕ_c = 4.85 eV, 5 eV and 5.25 eV.

Figure 6.8 portrays the change in the channel potential curve with varying work functions of the control gate. Three work functions were chosen (ϕ_c = 4.85 eV, 5 eV and 5.25 eV) for control gate and potential along the length of the active region (source to drain) was plotted using the model equations as well as through TCAD simulations. There is a good match between model-simulation results. It is seen that, as the work function of control gate increases, keeping the screen gate work function constant, there is a greater dip in the parabolic potential beneath the control gate. This is because there is stronger depletion in region 'C' when the control gate work function is higher.

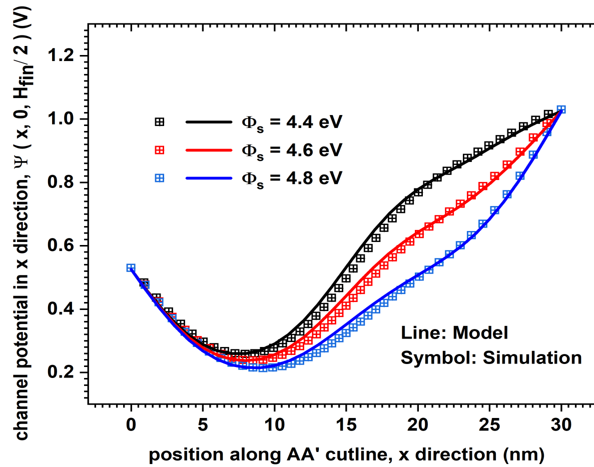


Figure 6.9: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different screen gate work functions, ϕ_s = 4.4 eV, 4.6 eV and 4.8 eV.

Channel potential variation for source to drain for DMG JLFinFETs with three different screen gate work functions (ϕ_s = 4.4 eV, 4.6 eV and 4.8 eV) is shown in Figure 6.9. With the increase in ϕ_s, the region 'S' gets more depleted for the same gate voltage, thereby shifting the channel potential down as shown in Figure 6.9.

Figure 6.10 presents channel potential variation from source to drain in DMG JLFinFETs with three different channel doping concentrations ($N_d = 10^{18}$ cm^{-3}, 5X10^{18} cm^{-3} and 10^{19} cm^{-3}). For fixed work function combinations of gate materials in a DMG, an increase in channel doping concentration reduces the magnitude of depletion in the channel. Hence overall channel potentials shift up with increase in doping

concentration. There is a fair match between model results and simulation results as shown in Figure 6.10.

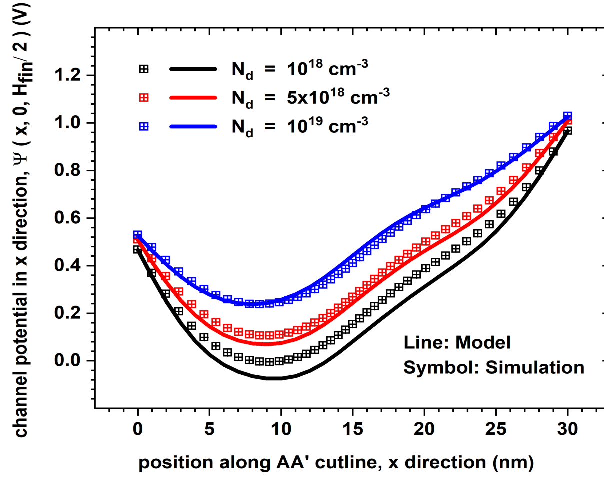


Figure 6.10: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$) in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different channel doping concentrations, $N_d = 10^{18}$ cm^{-3}, 5X10^{18} cm^{-3} and 10^{19} cm^{-3}.

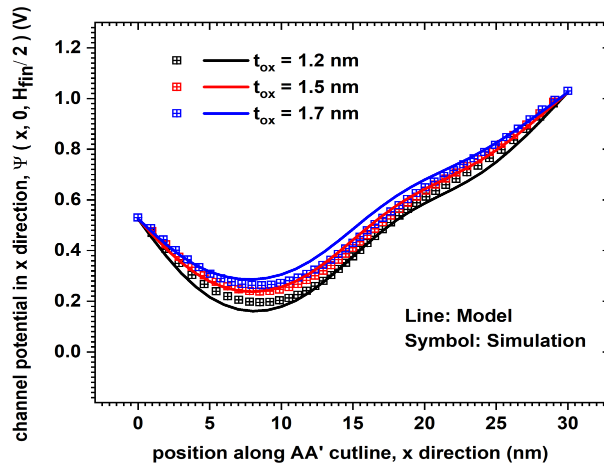


Figure 6.11: Potential variation from source to drain along x direction at y = 0 and z = $\frac{H_{\text{fin}}}{2}$ in DMG JLFinFET with V_{GS} = 0.3 V and V_{DS} = 0.5 V, for three different gate oxide thickness, t_{ox} = 1.2 nm, 1.5 nm and 1.7 nm.

Figure 6.11 gives the potential variation from source to drain in DMG JLFinFETs

with three different gate oxides (t_{ox} = 1.2 nm, 1.5 nm and 1.7 nm). There is a slight increase in channel potential throughout with an increase in gate oxide thickness. This is due to the lesser gate control over the channel with increasing t_{ox}. Hence channel depletion reduces with an increase in t_{ox}, thereby shifting the potential curve up as shown in Figure 6.11. A fair degree of match is visible between model-simulation data as shown in Figure 6.11.

6.4.2 Channel Potential Variation in All Directions

In Section 6.4.1, channel potential variation was analysed for DMG JLFinFETs with change in device parameters in the x direction. However, to determine the accuracy of the channel potential derived in equation 6.50 throughout the cuboidal channel, it is necessary to explore the degree of model - simulation match for channel potential in y as well as z direction.

To analyse the channel potential variation in the y direction, channel potential between two side gates of DMG JLFinFET is obtained through the model given in equation 6.50 and TCAD simulator. Figure 6.12 (a) shows the 3-D structure of DMG JLFinFET with xy cutplane, dissecting the structure at z = $\frac{H_{\text{fin}}}{2}$. The resulting 2-D structure with two side gates is shown in Figure 6.12(6.13b). The channel potential along y direction from one side gate to the other at x = 6 nm (in region 'C') and x = 24 nm (in region 'S') is shown in Figure 6.12(c). Along the y direction, there is a good match between the mathematical model and simulation result for channel potential at both x = 6 nm and 24 nm. However, near both the side gates, there is a slight model - simulation mismatch which stems out of homogenous silicon cuboidal approximation used while modeling channel potential.

To analyse channel potential variation in the z direction, a 3-D view of SOI DMG JLFinFET with xz cutplane located at y = 0 is shown in Figure 6.13(a). The resultant 2-D cross-sectional view of DMG JLFinFET with two channel regions marked is shown in Figure 6.13(b). Variation of channel potential along z direction is analysed at two different x locations, x = 6 nm which falls in region 'C' and x = 24 nm which is in region 'S'. Figure 6.13(c) shows the variation of channel potential both in region 'C' and 'S' spanning from z = 0 (buried oxide - channel interface) and z = 12 nm (gate oxide - channel interface). It is observed that the channel potential model matches well for 4 nm $\leq$ z $\leq$ 12 nm with the simulated data.

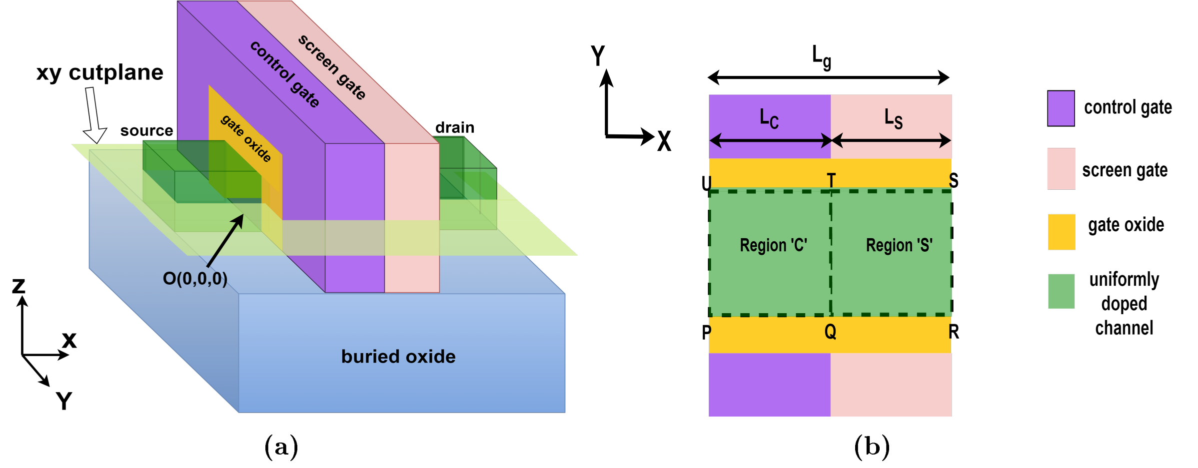
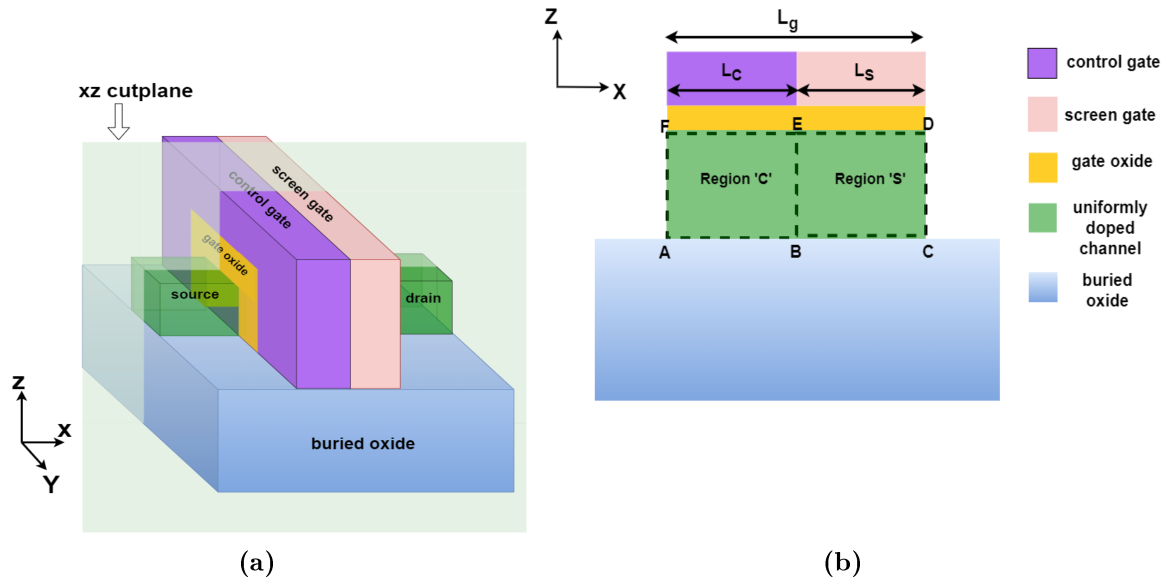


Figure 6.12: (a) DMG JLFinFET structure with xy cutplane located at z = $\frac{H_{\text{fin}}}{2}$ (b) 2-D cross-sectional view of DMG JLFinFET with channel bounded by the points P, Q, R, S, T and U and (c) potential variation between two side gates (in y direction) at z = $\dfrac{H_{\text{fin}}}{2}$ for V_{GS} = 0.3 V and V_{DS} = 0.5 V, at two different x locations (x = 6 nm belonging to region 'C' and 24 nm belonging to region 'S'.)

However, there is a mismatch between the model and simulation result for $0 \leq z <$ 4 nm. This model - simulation mismatch is attributed to the fact that while solving Poisson's equation, one of the boundary conditions for both regions 'C' (equation 6.8) and 'S' (equation 6.26) considers that potential maximum in the z direction is at z = 0 nm. This is not true as simulation results prove that the channel formation point is closer to z = $\dfrac{H_{\text{fin}}}{2}$ and not z = '0' which is explained in detail in Section 6.5.1.



(a) **(b)**

(c)

Figure 6.13: (a) DMG JLFinFET structure with xz cutplane located at y = 0 (b) 2-D cross sectional view of DMG JLFinFET with channel bounded by the points A, B, C, D, E and F and (c) potential variation along z direction at y = 0 for V_{GS} = 0.3 V and V_{DS} = 0.5 V, at two different x locations (x = 6 nm belonging to region 'C' and 24 nm belonging to region 'S').

6.5 Model for Threshold Voltage of DMG JLFinFET

This section details the modeling of threshold voltage in DMG JLFinFET. Various approximations adopted while solving equations for threshold voltage and reasons

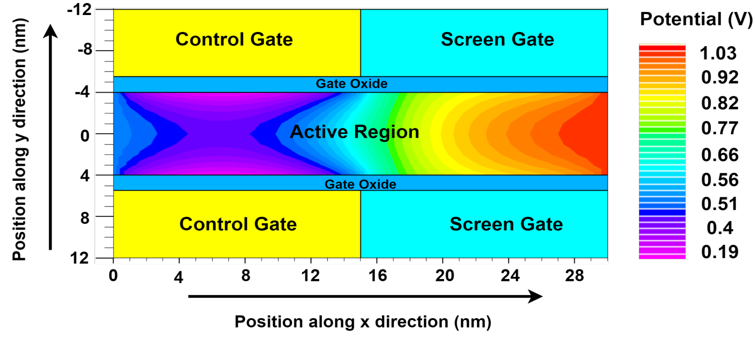
behind using these approximations are discussed. A closer picture of the location of the onset of the current conduction path in a DMG JLFinFET is obtained with the help of TCAD simulations. This in turn aids in choosing suitable approximations while modeling V_{th}.

6.5.1 Location of Onset of Current Conduction in DMG JLFinFET

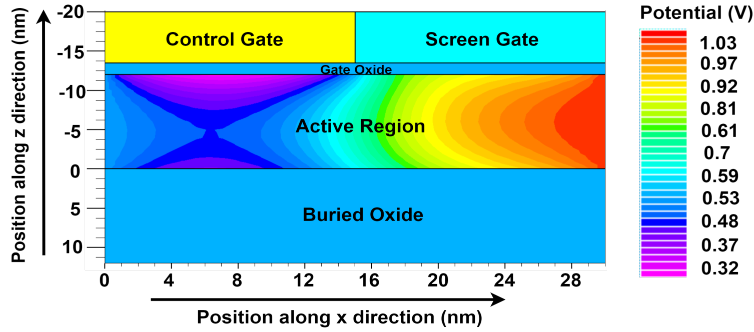
The method adopted in this chapter to model V_{th} is explained in Hu *et al.* (2016). This is described in detail in Section 5.3 of Chapter 5 as well. The threshold voltage is modeled by evaluating potential at a point (named 'K') in the channel which when undepleted, causes current flow through the transistor. Locating this point 'K' is a necessary step towards developing a model for V_{th}. The point 'K' in the channel is that point which
(a) undepletes last in the x direction (located at x = x_{min}),
(b) undepletes first in the y direction (located at y = y_{max}) and
(c) undepletes first in the z direction (located at z = z_{max}),
when V_{GS} is incremented, keeping V_{DS} fixed.

To give an insight on the location of onset of current conduction in a DMG JLFinFET, contour plots of potential in both xy plane and xz plane through the middle of the channel are given in Figure 6.14 (a) and 6.14 (b) respectively. For V_{th} modeling of DMG JLFinFET, x_{min} is chosen to be $0.4 \times L_c$. This approximation is taken from the findings of Hu *et al.* (2016) where they conclude that 0.4 times the channel length can be a probable x_{min} for SMG JLFinFET. As in a DMG JLFinFET, the threshold voltage is decided by the electrostatics in the channel region 'C', and only L_c is considered for x_{min}. Contour plots of potential in DMG JLFinFETs at threshold voltage, shown in Figure 6.14 (a) justifies this approximation. In this figure, there is a dip in potential near $0.4 \times L_c$. Thus x = x_{min} can be considered as the minimum potential point which undepletes last as V_{GS} is increased. y_{max} is certainly '0', due to the symmetric side gates in a JLFinFET having the least influence at y = 0. This is visible in Figure 6.14 (a) where y = 0 is the maximum potential point in the y direction. Therefore undepletion happens first at the middle of the channel in y direction when V_{GS} is increased. It could be observed from Figure 6.14 (b) that z_{max} is close to $\frac{H_{fin}}{2}$. Prior studies by our team show that z_{max} depends on many device parameters (Chennamadhavuni *et al.*

(2023)). As the accurate location of z_{max} is mostly near $\frac{H_{\text{fin}}}{2}$, z_{max} is approximated to $\frac{H_{\text{fin}}}{2}$ in this study.



(a)



(b)

Figure 6.14: Contour plot of potential from source to drain along (a) xy cutplane located at z = $\frac{H_{\text{fin}}}{2}$ and (b) xz cutplane located at y = 0, in a DMG JLFinFET with $\text{V}_{\text{GS}} = \text{V}_{\text{th}}$ and $\text{V}_{\text{DS}} = 0.5$ V.

In Section 6.4.2 the degree of match between the channel potential model derived in this chapter (for DMG JLFinFET), in the z direction with the simulated results was examined. However for a deeper understanding of the location of z_{max} at threshold voltage, variation in channel potential along z direction at x = x_{min} and y = 0, for different V_{GS} was analysed. V_{th} measured (using ϕ_{min} method described by Hu *et al.* (2016)) for the DMG JLFinFET considered in Figure 6.15 is 0.61 V. Figure 6.15

was plotted to observe the trend followed by channel potential in z direction as V_{GS} approaches V_{th}. It is observed in Figure 6.15 that conduction path formation is near $\frac{H_{fin}}{2}$ (Potential maximum point of simulated data is near $\frac{H_{fin}}{2}$). At z = $\frac{H_{fin}}{2}$, there is a good match between the model and the simulation result. Hence despite the mismatch between the channel potential model and simulation results seen in Figure 6.15, the channel potential model could still be used to model threshold voltage.

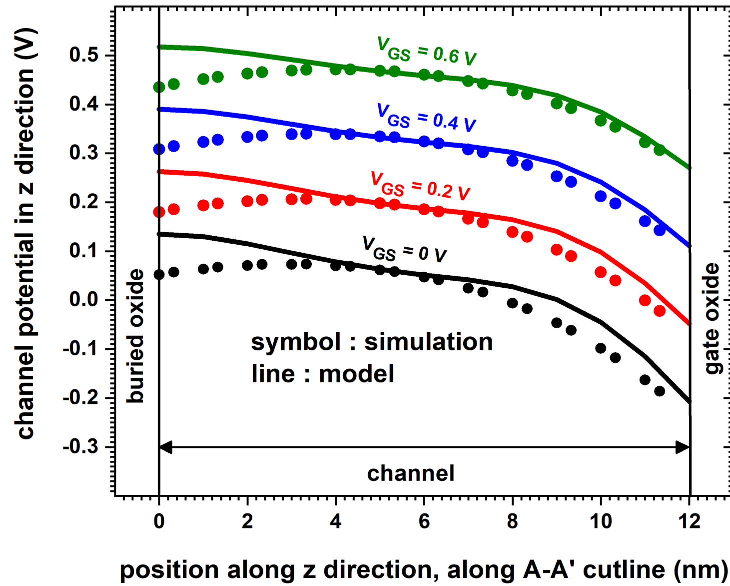


Figure 6.15: Potential variation in a DMG JLFnFET along A-A' cutline (A-A' cutline is along z direction at x = x_{min}, y = 0) for different V_{GS}, V_{DS} is fixed to 0.5 V.

6.5.2 Analytical Model Formulation for Threshold Voltage of DMG JLFinFET

As per Hu *et al.* (2014, 2016), threshold voltage condition is given as in equation 6.51

$$\Psi_K = \Psi\left(x_{min}, y_{max}, z_{max}\right) = V - 2V_t \qquad - - - - - \qquad \text{(threshold voltage condition)} \tag{6.51}$$

As per the discussion in Section 6.5.1, $x_{min} = 0.4 \times L_c$, $y_{max} = 0$ and $z_{max} = \frac{H_{fin}}{2}$. It may be noted that $y_{max} = 0$ is substituted while x_{min} and z_{max} are retained as such

while solving equation 6.51. x_{min} and z_{max} are substituted only in the final solution of V_{th}. The threshold voltage condition is then expressed by equation 6.52.

$$\Psi_K = \Psi\left(x_{min}, 0, z_{max}\right) = V - 2V_t \qquad ----- \qquad \text{(threshold voltage condition)} \tag{6.52}$$

Equation 6.52 is solved for V_{GS} to obtain V_{th}. n, m and l in the Fourier series are chosen to be '1' while solving equation 6.52. This is due to the complexity of solving equations increasing multifolds if higher harmonics of Fourier series are considered. As the point 'K' which is defined in Section 6.5.1 is under control gate, region 'C' only needs to be considered while modeling threshold voltage in a DMG structure. Hence equation 6.52 modifies to equation 6.53.

$$\Psi_c\left(x_{min}, 0, z_{max}\right) = V - 2V_t \qquad ----- \qquad \text{(threshold voltage condition in DMG transistor)} \tag{6.53}$$

Incorporating equation 6.12 in equation 6.53, equation 6.54 is obtained.

$$\Psi(x_{min}, 0, z_{max}) = \left(\frac{V_m - V_R}{L_c}\right) x_{min} + A_{1_c}(0, z_{max}) \sin\left(\frac{\pi}{L_c} x_{min}\right) = -2V_t \tag{6.54}$$

where $A_{1_c}(0, z_{max}) = G_{1_c}(0, z_{max}) + \Psi_{1_c}$.

Referring to equations 6.14 - 6.20, $G_{1_c}(0, z_{max})$ and Ψ_{1_c} are substituted into A_{1_c} and is then used in equation 6.54. The resultant equation is simplified and rearranged to obtain equation 6.55.

$$V_{GS} - \Psi_{sch_c} - V_R = \left(\frac{V_m - V_R}{2}\right) + \left(\frac{\frac{-Q}{64} + d_1 \cos\left(\frac{0.5\pi z_{max}}{h}\right)}{\frac{P}{16\pi} - 4\left(\frac{(k_{1_c})^2}{\pi}\right)\cos\left(\frac{0.5\pi z_{max}}{h}\right)}\right) \tag{6.55}$$

where

$$Q = P\frac{\left[2V_t + \frac{(V_m - V_R)x_{min}}{L_c}\right]}{\sin\left(\frac{\pi x_{min}}{L_c}\right)}, \tag{6.56}$$

and

$$P = \pi^4 \left(\frac{1}{t^2} + \frac{1}{h^2} + \frac{4}{{L_c}^2} \right) \tag{6.57}$$

As V_m is also dependent on V_{GS}, V_m from equation 6.39 is substituted in equation 6.55. The resultant equation is solved for V_{GS} which in turn is V_{th}. The analytical model for threshold voltage is given by equation 6.58.

$$V_{th} = \frac{W_1 - R_1 + 2\Psi_{sch_c} + V_R}{W_2 - R_2 + 2} \tag{6.58}$$

where

$$W_1 = \frac{0.5\pi T_2 - \dfrac{0.5\pi P \left(2V_t - \dfrac{x_{min}\,(R_1 + V_R)}{L_c} \right)}{\sin\left(\dfrac{\pi x_{min}}{L_c}\right)}}{T_1} \tag{6.59}$$

$$W_2 = \frac{0.5\pi P R_2 x_{min}}{L_c T_1 \sin\left(\dfrac{\pi x_{min}}{L_1}\right)} \tag{6.60}$$

$$R_1 = \frac{C_1 + S_1 - \dfrac{V_{DS} + V_R}{L_s} - \dfrac{V_R}{L_c}}{C_2 + S_2 + \dfrac{1}{L_c} + \dfrac{1}{L_s}} \tag{6.61}$$

$$R_2 = \frac{2C_2 + 2S_2}{C_2 + S_2 + \dfrac{1}{L_c} + \dfrac{1}{L_s}} \tag{6.62}$$

$$T_1 = -64\cos\left(\frac{0.5\pi z_{max}}{H_{eff}}\right)(k_{1_c})^2 + P \tag{6.63}$$

$$T_2 = 64 d_1 \cos\left(\frac{0.5\pi z_{max}}{H_{eff}}\right) \tag{6.64}$$

$$C_1 = \frac{\pi\left(\frac{4\,\Psi_{sch_1}+2\,V_R}{\pi}+\frac{4cosml\left(4d_1-\frac{8{k_{1_c}}^2\left(2\,\Psi_{sch_1}+V_R\right)}{\pi}\right)}{\pi^4\left(\frac{1}{{L_c}^2}+\frac{0.25}{{H_{eff}}^2}+\frac{1}{{T_{eff}}^2}\right)}\right)}{L_c} \tag{6.65}$$

$$S_1 = \frac{\pi\left(\frac{4\,\Psi_{sch_2}+2\,V_{DS}+2\,V_R}{\pi}+\frac{4cosml\left(4d_1-\frac{8(k_{1_s})^2\left(2\,\Psi_{sch_2}+V_{DS}+V_R\right)}{\pi}\right)}{\pi^4\left(\frac{1}{{L_s}^2}+\frac{0.25}{{H_{eff}}^2}+\frac{1}{{T_{eff}}^2}\right)}\right)}{L_s} \tag{6.66}$$

$$C_2 = \frac{\pi\left(\frac{2}{\pi}-\frac{32cosml\,(k_{1_c})^2}{\pi^5\left(\frac{1}{{L_c}^2}+\frac{0.25}{{H_{eff}}^2}+\frac{1}{{T_{eff}}^2}\right)}\right)}{L_c} \tag{6.67}$$

$$S_2 = \frac{\pi\left(\frac{2}{\pi}-\frac{32cosml\,{k_{1_s}}^2}{\pi^5\left(\frac{1}{{L_s}^2}+\frac{0.25}{{H_{eff}}^2}+\frac{1}{{T_{eff}}^2}\right)}\right)}{L_s} \tag{6.68}$$

where

$$cosml = \cos\left(\frac{2\,(m-0.5)\,\pi y}{T_{eff}}\right)\cos\left(\frac{(l-0.5)\,\pi z}{H_{eff}}\right) \tag{6.69}$$

6.6 Validation of threshold voltage model with TCAD simulation

In this section, threshold voltage computed from the analytical model given by equation 6.58 is compared with V_{th} obtained from the TCAD simulator. The effectiveness

of equation 6.58 in predicting V_{th} for DMG JLFinFETs with L_g spanning from 20 nm to 40 nm were examined for different
(a) fin thickness (T_{fin}),
(b) fin height (H_{fin}),
(c) control gate to screen gate length ratio ($L_c : L_s$),
(d) control gate work function (ϕ_c),
(e) screen gate work function (ϕ_s).
It must be noted that for all the results explained in this section, default values for unspecified parameters are listed in Table 6.1.

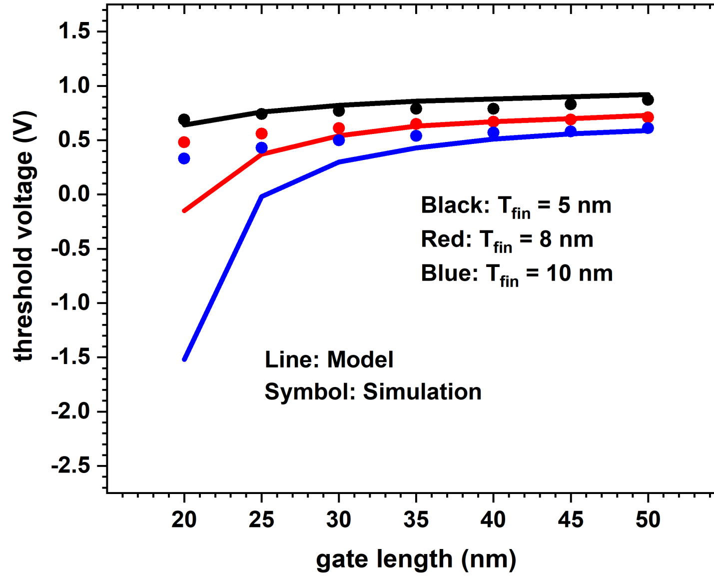


Figure 6.16: Threshold voltage variation with gate length for DMG JLFinFETs with three different fin thickness (T_{fin} = 5 nm, 8 nm and 10 nm).

Figure 6.16 gives the variation in V_{th} with L_g for DMG JLFinFETs with three different T_{fin} (T_{fin} = 5 nm, 8 nm and 10 nm). It can be observed that the V_{th} model derived in this chapter matches well with V_{th} obtained from the TCAD simulator for the case of T_{fin} = 5 nm (for all values of L_g). However, as T_{fin} increases, V_{th} predicted through the model matches well with simulation results for $L_g > 30$ nm while for lower gate lengths, the model underpredicts the threshold voltage. The difference between model and simulation results increases as T_{fin} is increased to 10 nm. One of the reason for mismatch between model and simulation is truncating both the double Fourier

series coefficients and single Fourier series coefficients by fixing indices to '1' (Fourier series truncation error). This process of Fourier series truncation while solving for V_{th} causes error that magnifies at lower channel lengths. Another important aspect is that homogenous silicon cuboidal approximation tends to give inaccurate results as fin thickness increases, as this results in T_{eff} value sliding away from T_{fin}. Also in the initial model work by our team, it is observed that as T_{fin} increases, the location of the onset of current conduction moves away from $\frac{H_{fin}}{2}$ (Chennamadhavuni *et al.* (2023)). Hence taking the approximation that $z_{max} = \frac{H_{fin}}{2}$ in threshold voltage condition is also a source of error for higher values of T_{fin}.

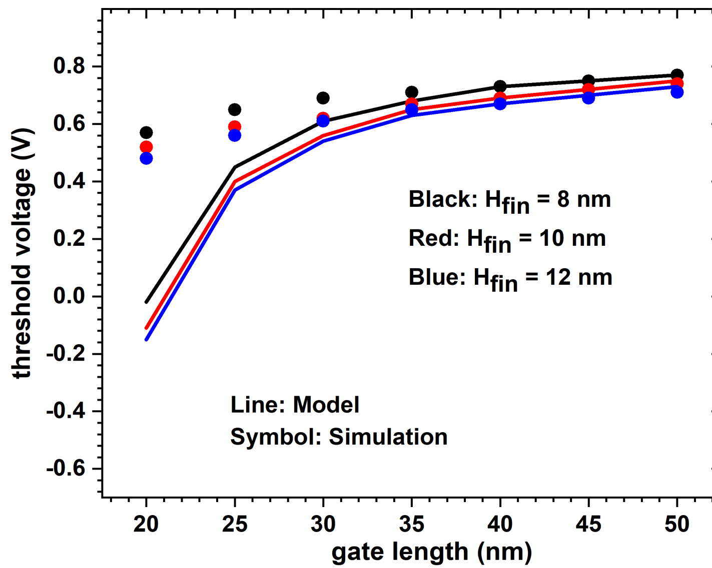


Figure 6.17: Threshold voltage variation with gate length for DMG JLFinFETs with three different fin height (H_{fin} = 8 nm, 10 nm and 12 nm).

A similar case study with V_{th} variation under different H_{fin} is presented in Figure 6.17. It can be observed that there is a fair model - simulation match for V_{th} for L_g > 30 nm, for all cases of H_{fin}. Nevertheless, as the channel scales down, the analytical model from equation 6.58 under predicts threshold voltage for all cases of H_{fin}. This is due to various short channel effects being ignored while modeling V_{th} as well as due to magnification of Fourier series truncation error for lower channel dimensions. It is observed from the article Chennamadhavuni *et al.* (2023) that variation of H_{fin}

doesn't have a significant impact on the location of the onset of current conduction at V_{th}. Hence the rate of mismatch between modeled and simulated data is mostly the same for all H_{fin} values considered. However, this is not true for the case of T_{fin}. Varying T_{fin} significantly alter the location of the onset of current conduction such that our assumption of $z_{max} = \frac{H_{fin}}{2}$ is more suitable as t_{fin} decreases. Hence model - simulation mismatch increases as T_{fin} increases as shown in Figure 6.16.

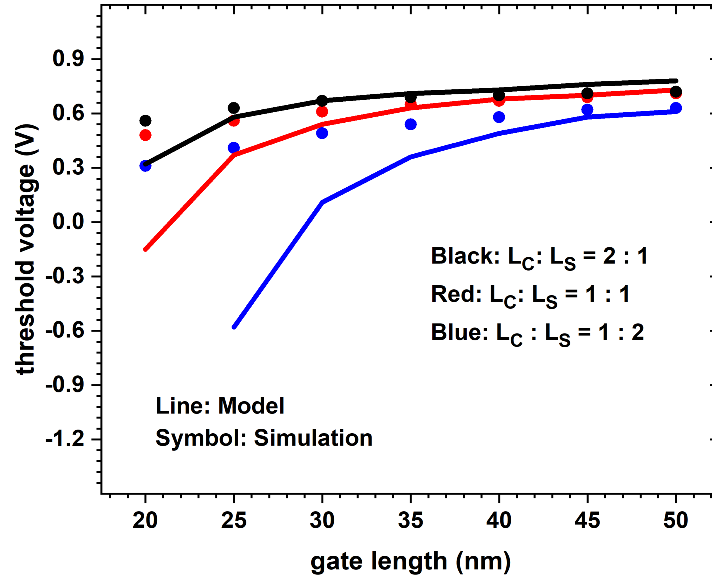


Figure 6.18: Threshold voltage variation with gate length for DMG JLFinFETs with three different $L_c : L_s$ ratio ($L_c : L_s$ = 2:1, 1:1 and 1:2).

Figure 6.18 shows the comparison between V_{th} obtained from the model as well as through simulation for DMG JLFinFETs whose control gate to screen gate length ratio varies. The best match was observed for $L_c : L_s = 2 : 1$ case. While for $L_c : L_s = 1 : 1$, good model - simulation match exists except for $L_g < 30$ nm. However, for $L_c : L_s = 1 : 2$, model - simulation mismatch is present for all L_g and error increases by a large amount when L_g decreases. Hence the threshold voltage model derived in this work is more suitable for DMG JLFinFET with $\frac{L_c}{L_s} \geq 1$

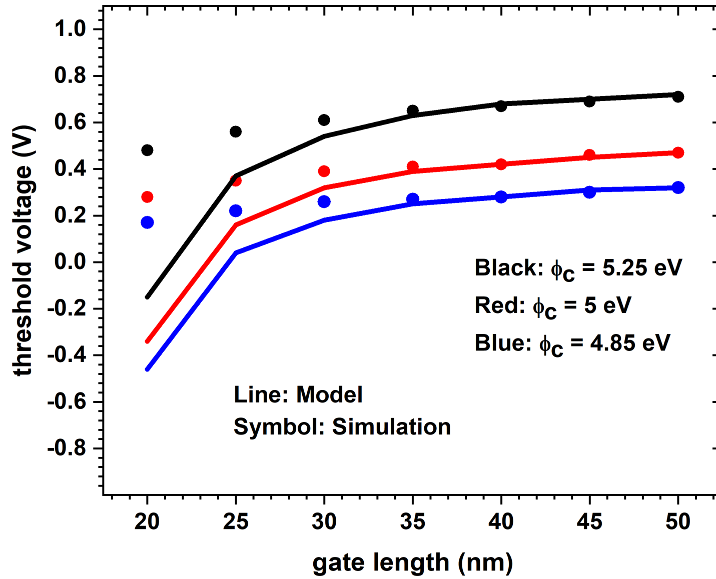


Figure 6.19: Threshold voltage variation with gate length for DMG JLFinFETs with three different control gate work function (ϕ_c = 4.85 eV, 5 eV and 5.25 eV).

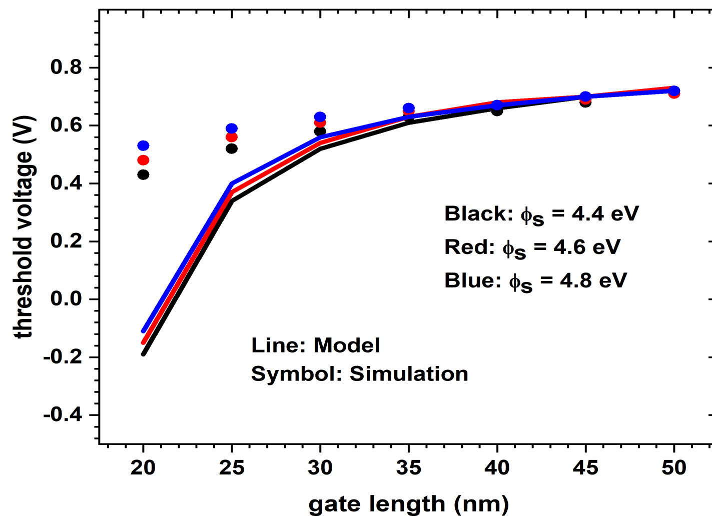


Figure 6.20: Threshold voltage variation with gate length for DMG JLFinFETs with three different screen gate work function (ϕ_s = 4.4 eV, 4.6 eV and 4.8 eV).

Figure 6.19 and Figure 6.20 show the V_{th} variation with L_g for three different

control gate work function and screen gate work function respectively. In both the figures for $L_g > 30$ nm, there is a good match between V_{th} obtained from the model as well as through TCAD simulation. However, from $L_g = 30$ nm, the model starts deviating from simulated data. The rate of increase of model - simulation difference with decrease in L_g is the same for all the cases of ϕ_c. The same trend is observed for ϕ_s also. It must be observed that the model correctly captures the increased influence of ϕ_c on V_{th} for all gate lengths analysed as compared to the influence of ϕ_s.

6.7 Brief of Errors that cause V_{th} Model - Simulation Mismatch

Developing analytical model for the 3-D channel potential of a transistor with asymmetric structure like FinFET is a laborious task. Hence many approximations are incorporated to reduce the complexity in solving tough equations and bring about a closed form of expression for the parameter modeled. However, these approximations are well suited in certain situations but can be a cause for model underpredicting/overpredicting the parameter in some other conditions. In this section, various errors that cause the V_{th} model derived in this chapter to underpredict simulation results are listed. They are

1. Fourier series truncation: For modeling threshold voltage, n, m, l indices are truncated to 1 as the complexity involved in solving equations spirals up if higher Fourier series harmonics are considered.

2. Homogenous silicon cuboidal approximation: To have symmetric boundary conditions so that solving 3-D Poisson's equation becomes easier, homogenous silicon cuboidal approximation calculates effective fin thickness (T_{eff}) and effective fin height (H_{eff}). For higher values of fin widths and fin heights, the difference of T_{eff}, H_{eff} values with their corresponding T_{fin} and H_{fin} values will be more giving way for more mismatch in V_{th} obtained from model and TCAD simulation.

3. Approximating z_{max} to $\frac{H_{fin}}{2}$: Structural parameters like T_{fin} have a profound impact on z_{max} location. z_{max} moves away from $\frac{H_{fin}}{2}$ for wider channel transis-

tors and hence this approximation can cause V_{th} model - simulation mismatch for higher T_{fin} devices.

4. Physical phenomena that dominate channels at lower channel lengths: Various phenomena like quantum effects that have a negligible effect on long channel transistor characteristics become dominant as channel length scales down. Hence ignoring these phenomena while modeling can be a potential cause of model - simulation error in smaller channel dimensions.

6.8 Summary

This chapter focuses on deriving analytical model for channel potential as well as threshold voltage of DMG JLFinFET. A Fourier series-based model was developed for the entire channel region of DMG JLFinFET. The derived channel potential model matched very well with channel potential obtained from the simulator for different groups of DMG JLFinFETs where in each group, one of the device parameters is varied. The channel potential model worked well in the y direction and z direction as well, except for z locations closer to the buried oxide - channel interface. Exploration of the location of the onset of current conduction in a DMG JLFinFET is done before framing the model for V_{th}. It is observed that current conduction starts near $\frac{H_{fin}}{2}$ and hence z_{max} point in the threshold voltage condition is approximated to $\frac{H_{fin}}{2}$. Analytical model for V_{th} was derived and a fair match is obtained between V_{th} obtained from the simulator as well as the derived model for DMG JLFinFETs with $L_g \geq 30$ nm. However, the derived V_{th} model in general underpredicted V_{th} for $L_g < 30$ nm. The cause of model - simulation mismatch for lower gate lengths could be attributed to incorporating Fourier series truncation, homogenous silicon cuboidal approximation, $z_{max} = \frac{H_{fin}}{2}$ approximation while modeling V_{th}.

Chapter 7

CONCLUSIONS AND FUTURE WORK

7.1 Summary and Conclusions

This research work was conducted in two parts. In the first part, an elaborate investigation of DMG JLFinFET is done through exhaustive device simulations which in turn put forth certain important findings that are crucial while designing the transistor. The findings from the initial part of the research proved that DMG JLFinFET is a suitable candidate for multi-transistor circuits. This motivated to mathematically model the characteristics of DMG JLFinFET as it paves way for their usage in commercial circuit simulators. Hence the second part of the research work focuses on developing analytical models for DMG JLFinFET. As SMG JLFinFET is the precursor of DMG JLFinFET, the development of models with better accuracy was first targeted for SMG JLFinFET. The same approach was extended to model channel potential and threshold voltage of DMG JLFinFET.

It was observed that in a DMG JLFinFET, two important parameters that can be tuned to obtain exemplary performance are difference in the work function of gate materials ($\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}}$) and length ratio of gate materials ($\frac{L_{\mathrm{M1}}}{L_{\mathrm{g}}}$). It is evident from DC analysis that gate material closer to source (M1) has more control over current characteristics than gate material closer to drain (M2). Better suppression of SCE like DIBL and sub-threshold swing is possible by proper selection of $\phi_{\mathrm{M1}} \sim \phi_{\mathrm{M2}}$ and $\frac{L_{\mathrm{M1}}}{L_{\mathrm{g}}}$. By having $\phi_{\mathrm{M1}} > \phi_{\mathrm{M2}}$ in a DMG JLFinFET, DIBL reduces tremendously whereas SS increases. Inorder to reduce both DIBL and SS simultaneously in a DMG JLFinFET,

$\frac{L_{M1}}{L_g}$ must be greater than 70% with ϕ_{M1} greater than ϕ_{M2}. Significant enhancement in DC characteristics and analog performance metrics alongside suppressing SCE is possible by incorporating high κ spacer materials with suitable spacer lengths. For DMG JLFinFETs with channel length of 10 nm, choosing HfO_2 as spacer material with a length of 5 nm gives optimum performance.

Rigorous simulations performed on JLFinFET revealed that for both Single Material Gate as well as Dual Material Gate architecture, the location of the onset of current conduction is closer to the middle of channel ($\frac{H_{fin}}{2}$). Hence incorporating this finding resulted in a more accurate threshold voltage and sub-threshold swing model than the already published model which considers the location of onset of current conduction to be at the channel-buried oxide interface. The highest possible error with the V_{th} model derived in this work is 1.46 V whereas peak error of 3.19 V is obtained from the published model. SS model derived in this work gave a maximum error of 153.27 mV/dec whereas with published model, the highest error was 382.95 mV/dec. Using the same approach adopted for SMG JLFinFET, efficient models were created for channel potential and threshold voltage for DMG JLFinFET in sub-50 nm regime. The outcomes of this research work are listed below.

- The dependence of DC characteristics and SCE on the work function as well as the length ratio of gate materials are explored and findings shed light on the guidelines to design a DMG JLFinFET according to the requirement.

- The influence of the dielectric constant and length of spacer materials on the channel electrostatics of a DMG JLFinFET is investigated. Significant enhancement in transistor characteristics is observed by selecting suitable spacers with proper spacer lengths.

- An accurate analytical model for threshold voltage and sub-threshold swing of SMG JLFinFET is derived taking into consideration, the location of onset of current conduction.

- A robust channel potential and threshold voltage model is derived for DMG JLFinFET.

However, for lower channel lengths (below 20 nm), the model underpredicts the threshold voltage of DMG JLFinFETs obtained through simulation due to various errors that become dominant when channel length scales down. Extensive research

on the cause of these errors and employing suitable techniques to mitigate them can open way for a powerful model for minute DMG JLFinFETs with dimensions of a few nanometres.

7.2 Scope of Future Work

The analytical model for channel potential and threshold voltage derived in this work can be extended for DMG JLFinFETs with spacers by properly choosing the boundary conditions while solving 3-D Poisson's equation. The discrepancy between the model and simulated threshold voltage of DMG JLFinFET for channel length lower than 30 nm can be minimised by considering higher indices of the Fourier series also while developing the mathematical model. Avoiding the use of homogenous silicon cuboidal approximation while solving Poisson's equation can bring forth a more accurate threshold voltage model in sub-30 nm. However suitable techniques to tackle the complexity involved in deriving the model without homogenous silicon cuboidal approximation should be invented. Developing a DMG JLFinFET structure with dimensions in accordance with current market trends through process simulation followed by fabricating it, is also a future scope of this work.

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Publications based on the thesis

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