INVESTIGATION OF CONTROL STRATEGIES FOR MULTIMODE OPERATION OF SERIES INTERFACING CONVERTER

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled Investigation of Control Strategies for Multimode Operation of Series Interfacing Converter which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me.* The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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CERTIFICATE

This is to *certify* that the Research Thesis entitled Investigation of Control Strategies for Multimode Operation of Series Interfacing Converter submitted by D.G.Abhilash Krishna (Register Number: EE16F01) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

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Abstract

The upcoming use of sensitive and critical equipments in the distribution system has resulted in the awareness of the power quality (PQ) issues. The PQ problems are not only concerned by end users of the electric power but also became major concern for electric utilities. Among all the PQ problems voltage related issues viz., voltage sag, unbalance and harmonic distortion are more prominent. The devices which are employed for power quality improvement are technically termed as *Custom Power Devices* (CPDs). The CPD includes shunt connected , series connected and a combination of series-shunt active devices. Among these the main focus of thesis is series connected converter as are considered to be more economical to compensate voltage disturbances. This thesis investigates control schemes for multifunctional operation of series converter in distribution and hybrid microgrid systems. When installed in distribution system the series converter acts as Dynamic Voltage Restorer (DVR) for compensation of symmetric and asymmetric voltage sags and harmonics, and also compensates faults at load side (downstream faults). Later the control schemes for operating the series converter as interlinking converter in hybrid microgrid system are investigated.

For the effective utilization of DVR control strategy plays significant role. This thesis proposes a dual role Cascaded Delay Signal Cancellation (CDSC) based Dual Vector Control (DVC) for DVR to compensate the symmetrical and asymmetrical voltage sags and harmonics. Based on the numerical analysis it is found that CDSC prefilter is promising solution when grid voltage is distorted by symmetric, asymmetric harmonics and voltage sag. The compensation voltage injected by DVR includes both fundamental and nonfundamental component. The proposed dual role CDSC has a feature of generating both components simultaneously. First, the prefilter extracts ISC of grid voltage and is given to the controller to generate fundamental component. Apart from that, to achieve the harmonic mitigation of load voltages, an extractor based on the modified CDSC strategy is designed which generates nonfundamental component of compensation voltage and added in 180^0 phase opposition to the DVC

algorithm. Intially simulation studies are carried out for different cases in PSCAD/EMTDC platform to validate the system. Later experimental studies are conducted on scaled down (100 V, 0.5 kVA) laboratory prototype DVR to verify the effectiveness of the proposed control algorithm under unbalanced and distorted grid conditions. Further in this thesis a Pseudo Derivative Feedback (PDF) based voltage control of DVR is proposed. The issues in the conventional P and PI based voltage controllers with and without feedforward path is studied. The efficacy of the PDF based DVR voltage control is demonstrated by comparative study with aforementioned conventional controllers using time response and relative stability analysis. The comparative study is validated through simulation (PSCAD/EMTDC) and experimental studies (on aforementioned scale down laboratory prototype system)

To protect the PCC voltages of the system during faults on load side, a Virtual Impedance (VI) based Downstream Fault Current Limiter (DFCL) for DVR is proposed. By employing the DFCL the fault current is suppressed as the DVR act as virtual impedance in series to the system during the downstream fault conditions. The main advantages of proposed DFCL is no extra passive devices are required to be installed such that the DVR is bypassed during the fault condition and moreover these devices introduce additional losses to the system. In this thesis apart from VI-based DFCL the limitations of other DFCL methods are discussed in detail to show the robustness of proposed DFCL. The proposed DFCL model is simulated using PSCAD/EMTDC and the respective results prove its efficacy.

Apart from the conventional DVR topology (with injection transformer) this thesis work also proposes a control algorithm for Transformerless DVR (TDVR) topology. Due to its reduced cost weight, size, and losses the TDVR topology is more efficient than conventional topology but the main challenge with this topology is design of control structure. Different control algorithms are investigated for TDVR topology and finally Uncertainty and Disturbance Estimator (UDE) based control algorithm is proposed. The UDE based control algorithm overcomes the parameter variation issue in addition to the voltage sag compensation. It posses simple structure for implementation compared to other control algorithms

mentioned in literature. Simulation (MATLAB/SIMULINK) and experimental studies are carried out for evaluation of system under symmetric and asymmetric voltage sags.

Finally the operation of series converter as *Interlinking Converter* (IC) is discussed in the present thesis. The hybrid AC/DC systems with DC and AC sources/loads are considered to be the most likely future distribution or even transmission structures. This is achieved by an IC. The IC can act as a rectifier or an inverter depending on the direction of power flow needed at each instant. IC topology selection depends primarily on the control objectives needed to be fulfilled by it. The IC typically controls the DC bus voltage when HMG is in grid conneccted mode. There is an increasing demand for executing additional functions other than the primary function of power management using a single IC rather than employing multiple ICs or additional active/passive components. Additional control objectives include, storage coordination, stability improvement, managing power and voltage unbalances among phases, grid current control, harmonics mitigation, islanding detection, synchronization, fault limiting, etc. This demand for multi-functional ICs has led to an investigation of various modes of operation in hybrid microgrid which mainly focus on AC side and DC side voltage control, bidirectional power flow. In this approach DC subgrid is integrated with main utility grid via single interlinking converter. The control strategy adopted ensures the multimode operation of proposed single IC which includes the bi-directional operation also. Furthermore, the control strategy allows the IC to provide stable DC bus voltage for dc subgrid during transients and exchange power between the ac and dc buses.A hybrid ac/dc MG is simulated using PSCAD/EMTDC software and simulation studies of various modes are presented to validate the effectiveness of the proposed single multifunctional IC.

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Nomenclature

AC	Alternating current
ACMG	AC Microgrid
A/D	Analog to Digital
BPF	Band-Pass Filter
CDSC	Cascaded Delayed Signal Cancellation
CPD	Custom Power Devices
D/A	Digital to Analog
DC	Direct current
DCMG	DC Microgrid
DFT	Discrete Fouruer Transform
DG	Distributed Generation
*dq*PLL	Synchronous *dq*-Frame Phase Locked Loop
DSC	Delayed Signal Cancellation
DSP	Digital Signal Processor/Processing
DVR	Dynamic Voltage Restorer
EMTDC	Electromagnetic Transients including DC
FC	Fuel Cell
FCL	Fault Current Limiter
FFL	Frequency Feedback Loop
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
HMG	Hybrid Microgrid
HPF	High Pass Filter
IC	Interlinking (Interfacing) Converter
I/O	Input/Output
LF	Loop Filter
LPF	Low Pass Filter
LV	Low Voltage
MATLAB	MATrix LABoratory
MG	Microgrid
MV	Medium Voltage
PD	Phase Detection

PDF	Pseudo Derivative Controller
PF	Passive Filter
PI	Proportional Integral
PLL	Phase Locked Loop
PSCAD	Power System Computer Aided Design
PWM	Pulse width modulation
SOGI	Second Order Generalized Integrator
SRF	Synchronous Reference Frame
SSC	Static Series Compensator
TDVR	Transformerless Dynamic Voltage Restorer
THD	Total Harmonic Distortion
VCO	Voltage Controlled Oscillator
VI	Virtual Impedance
VOC	Vector Oriented Control
VSI	Volatge Source Inverter
ZCD	Zero Crossing Detection

Chapter 1

INTRODUCTION

Contents

1.1 Background

In the past, equipment used to control industrial process was mechanical in nature, which are tolerant of voltage disturbances, such as voltage sags, spikes, harmonics, etc. In order to improve the efficiency and to minimize costs, modern industrial equipment typically uses a large amount of electronic components, such as programmable logic controllers (PLC), adjustable speed drives (ASD), power supplies in computers, and optical devices. Nevertheless, such pieces of equipment are more susceptible to

malfunction in the case of a power system disturbance than traditional techniques based on electromechanical parts(Wagner et al., 1990). Minor power disruptions, which once would have been noticed only as a momentary flickering of the lights, may now completely interrupt whole automated factories because of sensitive electronic controllers or make all the computer screens at an office go blank at once. In order to restart the whole production, computers, etc, a considerable time might be necessary (in the range of some hours), implying on significant financial losses to an industry (Warren et al., 1999),(Davis et al., 1996). Further on the other hand due to this power disturbances utilities faces increased Transmission and Distribution losses, Overloading of Cables, Transformers and Switchgears, Tripping of Circuit Breakers and residual current devices etc.,

From the electric utility point of view power quality events viz., voltage sags, swells, flicker and harmonics originate from the faults in the distribution system, which are caused due to starting of heavy loads or load dynamics. In general, an unbalanced supply voltage leads to the generation of harmonics into the system which increases the losses of the system and disturb the operation of AC machines. Moreover, the low negative sequence impedance of the distribution system leads to generation of high negative sequence currents which exaggerate the grid losses(Bollen, 2000).

It is quite common for the power consumers that they become more worried about the power quality in the distribution system. The expression power quality has become the current buzz word among the power generating companies for the past few years (Dugan et al., 1996), (iee, 1995). The term includes numerous phenomena observed in power systems. Although the power grids have always been affected by such disruptions, considerable care was taken to mitigate their impact on end users, in particular large industrial plants (gol, 1998).

As per transmission systems are concerned, they were over dimensioned in the past, with large stability margins. As a result, dynamic compensators, viz., synchronous condensers were hardly needed. But during the last two decades, building-up of generation facilities and fresh transmission lines became unworkable owing to budgetary and environmental concerns. Hence, making effective use of the available power systems became obligatory (Stahlkopf and Wilhelm, 1997). Although integration of separate power systems fosters improved and effective harnessing of power generation capability, such integrated systems should be capable of regaining from failures and supply the needed power during variations in load.

From the economic stand point, one of the significant developments has been the gradual liberalization of power transmission/distribution market worldwide. The utilities very well know the value of delivering "good quality" of supply voltage to their consumers with a view to gratify and in turn retain them.

In addition to the modifications in the operations and needs of transmission and distribution systems, the power semi-conductor technology has undergone quick transformations. The only semiconductor device applied to high power applications up to the early 1990s, was the thyristor, engaged in High Voltage Direct Current (HVDC) transmission systems and Static Var Compensators (SVC)(Ekstrm, 1992), (Gyugyi, 1988).However, the voltage and current ratings of commercially available power semiconductor devices have continually escalated, enhancing the attainment levels and lowering the need of series and parallel connections for obtaining the intended rating, causing their utilizations more compact with reducing expenditures(Carroll, 1999),(Akagi, 1998).

1.2 Motivation of the work

The great majority of voltage variations affecting customers are caused by faults on the power system, being often result from weather conditions, e.g. lightning, wind, and ice hitting overhead lines (Dugan et al., 1996), (Taylor and Burden, 1997). On underground cables, typically used at urban areas, insulation problems and operation of excavators are the main causes of voltage interruptions.

Conventional protection equipment used in distribution systems, e.g. reclosers and breakers, are based on mechanical parts. Typical fault clearing times vary from 3 to 30 cycles, depending on fault current magnitude and the type of overcurrent protection (Becker et al., 1994). The components of the distribution system have thus to be over dimensioned in order to withstand high fault currents before the protection system actuation and transient overvoltages at the opening of breakers. In addition to that, such type of electrical stress results in the reduction of the life expectancy of the equipment.

Remote faults in the system can cause a voltage reduction (referred as voltage sag or dip), where a critical customer is connected. If the current magnitude is relatively large compared to the available fault current at that point (i.e. the short-circuit capacity/power), the resulting voltage sag can be significant.

According to some surveys, voltage sags have become a major power quality problem, resulting in large financial losses to industries (Gunther and Mebta, 1995), (Mcgranaghan et al., 1991), (Bollen, 2000). Although the duration of a voltage sag resulted from a remote fault is only a few cycles and the voltage can totally be recovered a few cycles afterwards, the process equipment often cannot keep continuing its normal operation during these sags and will trip or shut down.

Many customers with sensitive loads have installed their own uninterruptible power supplies (UPS) to provide ride-through capability (i.e. continuing the process operation during a disturbance in the supply network) against voltage interruptions and sags. However, UPS systems are not economically feasible at high power ratings (MVA order), besides being energy inefficient and requiring maintenance that may exceed the owners available resources (Davis et al., 1996). Space constraints and necessity of changing facility requirements can also make the installation of UPS systems more difficult. In fact, a trend indicates that the majority of industrial and commercial customers would prefer a utility-provided solution to power systems disturbances, with the cost included in their power bill, as an alternative to the purchase, installation and operation of their own-site equipment.

In an effort to address power disturbances such as voltage sags on electronic equipment, a general guidance for equipment tolerances to power disturbances is established by the Information Technology Industry Council (ITIC) curve. The ITIC curve, which is formerly known as the Computer Business Equipment Manufacturers Association (CBEMA) curve, illustrates the equipment tolerances in terms of percent nominal voltage versus duration. Originally, the ITIC curve defined the tolerance of main frame computer equipment to withstand disturbances in terms of voltage magnitude and duration, hence its former name Computer Business Equipment Manufacturers Association (Dugan et al., 1996). This curve has been adopted by other industries and has been evolved into a standard for measuring power quality performance for a variety of electronic equipment. The ITIC curve is shown in Figure 1.1. To understand the region of interest in this dissertation, the voltage sag region is overlaid in blue on the ITIC curve figure.

Figure 1.1 shows that much of the voltage sag region (shown in blue) falls within the No Damage Region of the ITIC curve. Although equipment conforming to the curve may survive operation in the No Damage Region, sensitive pieces of equipment such as those in industrial facilities are susceptible to voltage sags, accounting for a

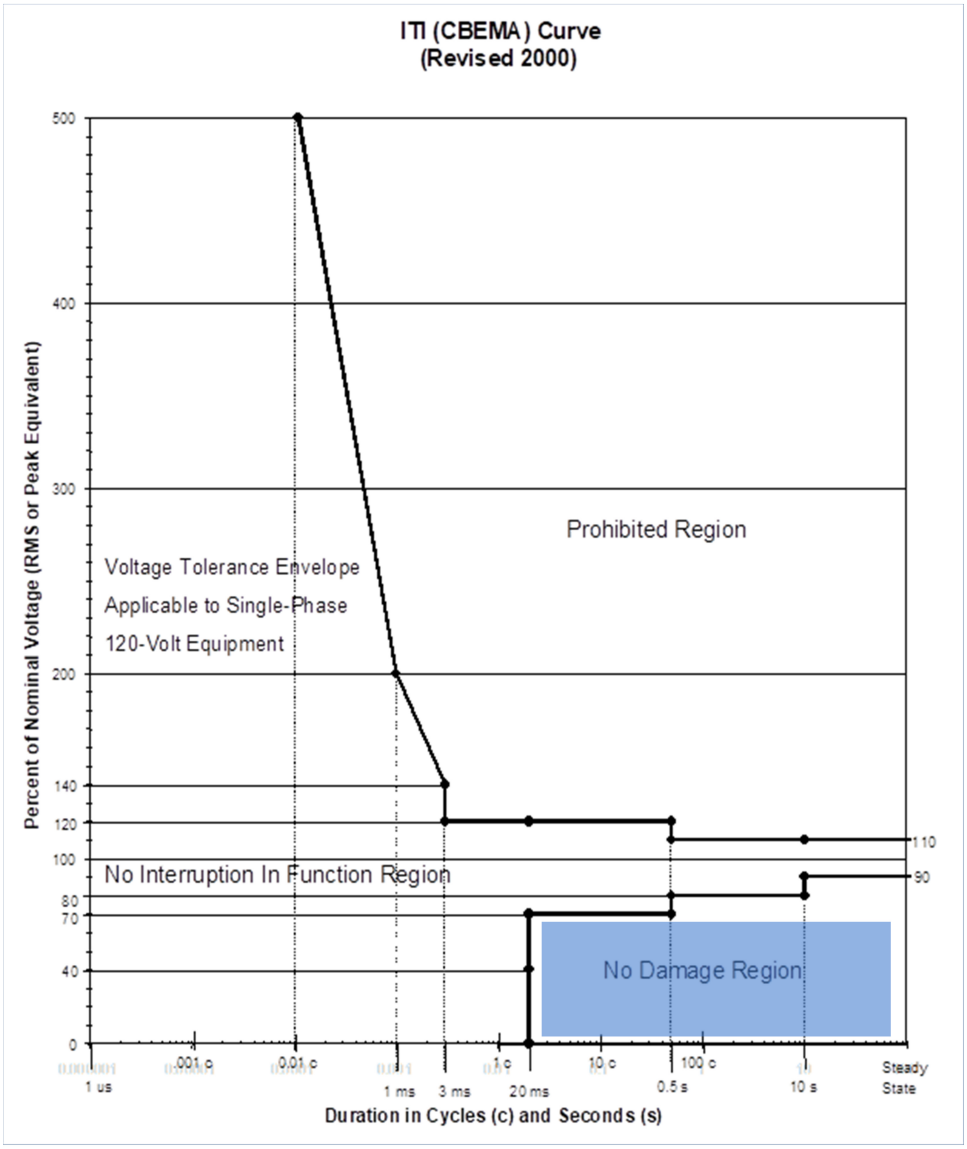


Figure 1.1: ITI Curve

large percentage of power quality events at these types of facilities. This is shown in Figure 1.2. The red dots in the figure represent voltage events collected at one hundred large manufacturing plants in the United States over a period of one year (Stahlkopf and Wilhelm, 1997), (Douglas, 1996). The blue dashed lines in the figure outline the ITIC curve.

The impact of voltage sags on sensitive equipment varies. It ranges from load disruption to equipment damage. It has been found that in some industrial equipment,

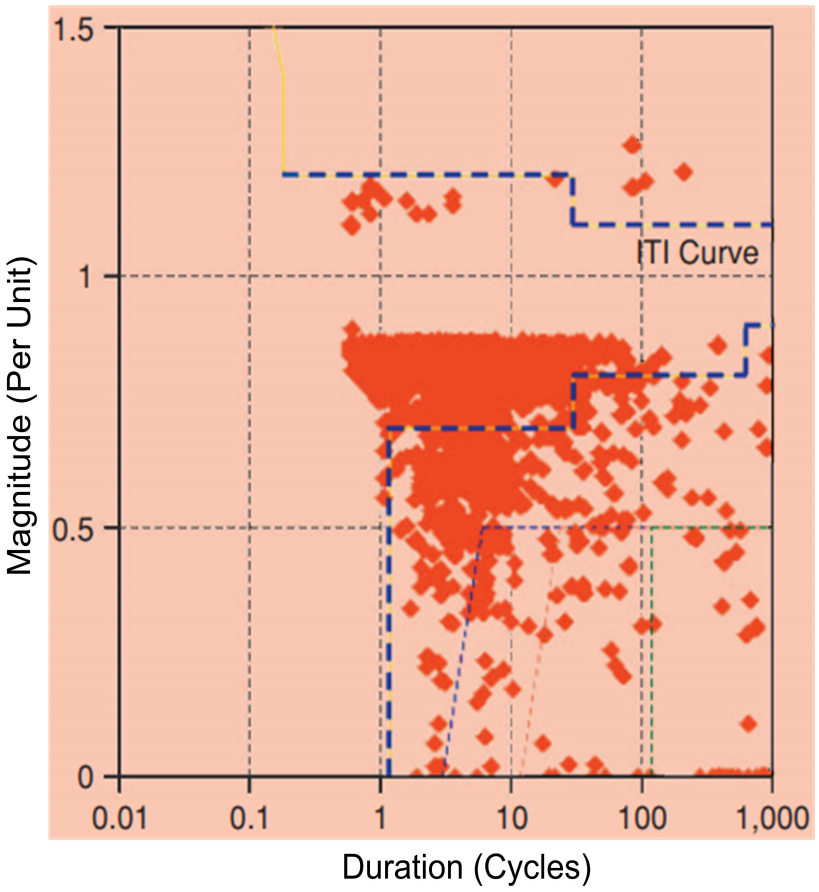


Figure 1.2: Voltage Events at Manufacturing Plants

the current surge which occurs after a voltage sag is the actual cause of the equipment damage (Stahlkopf and Wilhelm, 1997).

The impact of voltage sags on sensitive equipment is not limited to the load or the equipment alone. Usually, these pieces of equipment are an integral part of an industrial or manufacturing process, such that any disruption to the process may cost extensive down time and repairs. An example of such a sensitive process is the area of semiconductor fabrication and manufacturing (Chan et al., 1998). In summary, voltage sags account for a significant percentage of power disturbances, but they are not addressed in the ITIC curve in terms of tolerance levels. This is because they have minimal impact on general electronic equipment. Their greatest impact is on sensitive equipment, and the impact ranges from load disruptions to economic losses. To overcome this, it is evident that there is a need for methods to mitigate voltage sags.

To avert any adverse impact of the voltage fluctuations on the sensitive loads, various remedies are available. The most pliable and potent remedy is to utilize the power electronic devices as compensators which comprise series and parallel and series-parallel which are termed as custom power devices (Hingorani, 1995), (Douglas, 1996),(Ghosh and Ledwich, 2002). The series compensators, viz., Static Series Compensator (SSC), Dynamic Voltage Restorers (DVR) are contemplated to be the most cost-effective remedies to compensate voltage in distribution systems. Although, the control strategies and purposes of these compensators may differ from each other, but their operation principle and power circuit architecture are the same.

Apart from distribution system the power quality problems are prevailed in microgrid systems. The new concepts of smart grids have been extensively developed in recent years. Hybrid Microgrid (HMG) is one among them which interlinks two distinct ac and dc subgrids via Interlinking Converter (IC). Though this technology has many advancements still the PQ problem avails. The presence of unbalanced faults in the AC grid affects the operation of HMG, especially ICs. For ICs under grid faults, active power and reactive power oscillations are important problems, which may result in DC link oscillation and instability (Sun et al., 2017). Also, overcurrent might occur when grid voltage becomes unbalanced, which restrict power transfer capability of ICs (Sun et al., 2017). Thus to avoid all the voltage power quality problems the interfacing converter should be controlled in such a way that it act as compensator to mitigate these disturbances in the HMG system.

1.3 Custom Power Devices

The section gives a short survey of two main types of controllers to mitigate voltage dips (Gyugyi, 1976), (Akagi, 1992)(Sannino et al., 2000). Initially, shunt controllers are treated followed by series controllers and combined series/shunt controllers.

1.3.1 Shunt Controllers

Shunt controllers are extensively used for voltage stabilization at a certain point and in case the controllers are connected with a VSC, the devices are called Static Compensators (STATCOM), Static Condensers (STATCON) or Advance Static Var compensators (ASVC) (Hingorani, 2000),(Wang et al., 1998).

Shunt devices are effective to compensate small voltage variation, which can be controlled by reactive power injection. The ability to control the fundamental voltage at a certain point depends on the impedance to the supply and the power factor of the load. The compensation of a voltage dip by current injection is very difficult to achieve, because the supply impedance are usually low and the injected current has to be very high to increase the load voltage. Compensation of a voltage dip with a shunt controller is illustrated in Figure 1.3. Considering a case with a supply voltage with 1 p.u. voltage and a supply impedance of 0.1 p.u. inductively. If the active load varies from 0 to 1 p.u. the load voltage vary from 1 - 0.995 p.u. Inserting a shunt converter with 1 p.u. current injection the load voltage can be controlled in the range of approximately 0.9 - 1.1 p.u. At a 0.5 p.u. voltage dip the shunt converter must inject a high reactive current to stabilize the load voltage at 1 p.u.

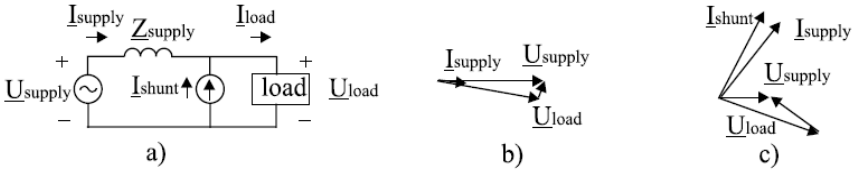


Figure 1.3: The use of shunt converter to compensate for voltage dip. (a) circuit diagram (b) vector diagram for normal condition and (c) vector diagram for compensation of voltage dip

By injecting proximately 5 p.u. reactive current, it is practicable to compensate a 0.5 p.u. voltage drop. Injecting active power by the shunt converter will hardly have any effect on the load voltage. In case the shunt controller supplies the load with active power, it still has to inject proximately 5 p.u. reactive current to sustain the load voltage. This process demands stored energy and a minimum of 5 p.u. rated shunt converter.

Breaking the connection to the supply during a voltage dip can keep the rating of the shunt converter to approximately 1 p.u. and deliver all the active and reactive power needed by the supply and resynchronize with the grid, when the voltage dip is over. This simple example indicates the poor effectiveness to compensate voltage dips with shunt controllers.

1.3.2 Series Controllers

The series controllers for the control of the fundamental voltage are called as a series connected PWM regulator in (Campos et al., 1996), a static series regulator in (Haddad and Joos, 1997), (Joos, 1999), but usually the devices are called as dynamic voltage restorers. In the case where the device only injects reactive power, such devices can be called as series VAR compensators (Joos et al., 1998) .

Taken the same simplified model of a supply and a load, by inserting a series controller to support the load a 0.5 p.u. voltage dip can be restored by a 0.5 p.u. DVR (series device). Only 0.5 p.u. of the energy which is absorbed by the load has to be supplied by the DVR. The supply continues to be connected and no resynchronization is necessary as it is the case with the shunt connected converter.

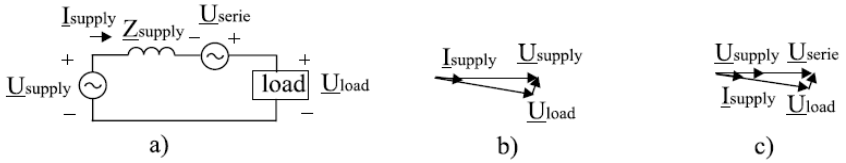


Figure 1.4: The use of series controller for a voltage dip (a) circuit diagram (b) vector diagram for normal conditions (c) vector diagram for compensation of voltage dip

1.3.3 Combined Controllers

Combining the series and shunt controllers to manage the load voltage are usually cited as a Unified Power Quality Conditioner (UPQC) (Fujita and Akagi, 1998) or line-interactive uninterruptible power supply (UPS) (Oliveira da Silva et al., 2002).

Figure 1.5 illustrates the two possible connection methods. The installed rating tends to increase with unified approaches, but the performance can also be improved and some of the benefits with both shunt and series controllers can be utilized. Both controllers can exchange reactive power with the grid and active power can be transferred between the controllers. Most important the energy storage can be significantly reduced with unified approaches.

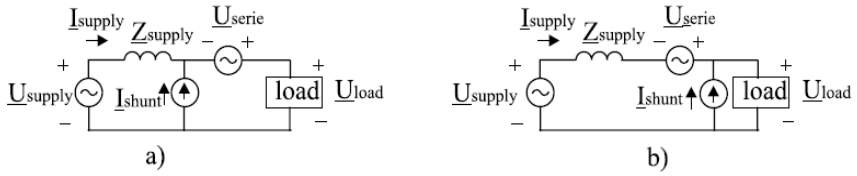


Figure 1.5: Unified controllers (a) shunt-series controllers and (b) series-shunt controllers

1.4 Interfacing Converter

Interfacing Converter (IC) is a power electronic device which interlinks two distinct ac and dc subgrids to form a hybrid microgrid (HMG). The IC can act as a rectifier or an inverter depending on the direction of power flow needed at each instant. IC topology selection depends primarily on the control objectives needed to be fulfilled by it. The functions of IC in HMG are power management, voltage unbalances (viz., sags, swells), fault limiting, harmonics mitigation etc. Earlier multiple ICs were used in HMG to achieve aforementioned functions.

At present there is an increasing demand for executing additional functions other than the primary function of power management using a single IC rather than employing multiple ICs or additional active/passive components. Thus in this thesis a single IC is employed for achieving the multifunctional operation in HMG. As mentioned in the preceding section shunt controllers, as shown in Fig.1.3, are recommended mainly for mitigation of the causes of disturbances, and not their effects in distanced nodes of a power-electronics system (Kazmierkowski, 2007). In the case when reduction of disturbances effects is required, which leads to protection of sensitive loads from the deterioration in the supply-side voltage, series voltage PE quality controllers are employed (Kazmierkowski, 2007). Such controllers, operating as a synchronous voltage source, are included in the feeder in series between the supply voltage and the load, which is illustrated in Fig.1.4 . Thus in this thesis a series interfacing converter is employed to achieve the desired objectives.

1.5 Objectives

1. To design a control strategy for Dynamic Voltage Restorer (DVR) to compensate the upstream faults.

2. To design a robust Fault Current Limiting Function for the DVR to compensate downstream faults.

3. To develop effective power flow management for series interfacing converter in hybrid microgrid.

4. Integrate fault limiting operation in the control strategy to ensure stable operation of hybrid microgrid.

1.6 Contribution of thesis

The present thesis work discuss about the development of control strategies for multifunction operation of series interfacing converter which has capability to operate in distribution and hybrid microgrid system. The multifunctional operation includes compensation of symmetric and asymmetric voltage sags and harmonics, compensation of voltage swells and compensation of faults at load side (downstream) when installed in distriution side. Further in this thesis work investigation on modes of operation of series converter(Interfacing Converter) in hybrid microgrid is presented. The main objective of series converter is to control the power flow from the utility (AC) source to the AC loads and also DC loads.The following points speaks about the contributions of the work:

- Comparative study of the performance of PLL prefilter algorithms under distorted grid conditions through simulation studies in PSCAD/EMTDC. Based on the studies Cascaded Delayed Signal Cancellation (CDSC) based prefilter is proposed which offers better disturbance rejection compared to other filters.

- To protect the sensitive loads from the harmonics produced in the source side an extractor is proposed based on the CDSC strategy to extract the desired harmonics in the load and thereby eliminating the addition of extra controller which are specifically designed to mitigate harmonics. Thus, a dual role operation of CDSC is proposed.

- Simulation and experimental analysis of dual role CDSC based Dual Vector Control (DVC) algorithm for DVR in PSCAD/EMTDC is carried out.

- Pseudo Derivative Feedback (PDF) controller-based voltage control scheme for DVR is proposed. A comparative analysis of performance parameters are carried out between PDF and existing controllers (P and PI) through simulation and experimental studies.

- A virtual impedance-based fault current limiting control for DVR during downstream faults is proposed thereby DVR acts like an additional line impedance in series with distribution feeder. This method eliminates the usage of conventional mechanical bypass switch and addition of extra superconducting devices which causes losses to the system.The efficacy of the proposed controller to limit downstream fault current is verified through simulation studies in PSCAD/EMTDC.

- In this thesis work control strategies for Transformerless DVR (TDVR) topology are also investigated. The proposed control strategy has good ability of reference tracking and robustness to parameter variations. The efficacy of the proposed controller is verified through simulation (in MATLAB) and experimental studies.

- Hybrid ac/dc microgrids are one of the most interesting approaches towards the development of the smart grid concept in the current distribution network. The term hybrid ac/dc microgrid refers to a microgrid that contains both ac/dc power sources and ac/dc loads. In view of power electronic converter utilization researchers in literature discussed as a custom power device to compensate voltage disturbances viz., sags and swells in the system. Further the proposed control strategies in this area are mainly focussed on power quality improvement on AC side of the system. In this view the role of series interlinking converter on power quality improvement in hybrid microgrid has not been discussed much yet. Thus, in this thesis an attempt is made to investigate different modes of operation for series interlinking converter in a hybrid microgrid which mainly focus on AC side and DC side voltage control and bidirectional power flow transfer control.

1.7 Thesis organization

The thesis is organized as follows

Chapter 1: This presents an introduction which consists of a brief overview of the thesis and the reasons for its motivation followed by the research objectives and a concise description of the flow in which the thesis is organized.

Chapter 2: In this chapter literature survey of control strategies employed for operation of series converter in distriution system for mitigating voltage disturbances is presented. Further the chapter also presents the different types of interlinking converters in the hybrid microgrid enviroment.

Chapter 3: In this chapter the concept of dual role CDSC is discussed. Prior to that a brief introduction to SRF-PLL is presented preceded by drawbacks of the conventional SRF-PLL. Further the process of reference generation is also discussed.

Chapter:4 In this chapter the proposed dual role CDSC based DVR system is evaluated extensively through simulation and experimental studies.

Chapter 5: This chapter mainly deals with the design aspects of proposed voltage controller PDF for compensation of upstream faults. The chapter starts with the evolution of proposed controller and precedes with comparative study of proposed controller with conventional P and PI controllers. The controller parameter tuning procedure is presented and finally results pertaining to simulation and experimental analysis of the proposed voltage controller based DVR system is presented.

Chapter 6: This chapter describes the design aspects of Fault current limiter and transformerless operation of DVR. Firstly, the virtual inductance based FCL operation of DVR is presented for compensating downstream faults. Later the chapter procedes with the design of virtual impedance parameter and discuss about the simulation results of performance of virtual impedance based DVR system under downstream faults. In addition to that this chapter presents a Uncertainity and disturbance estimator control scheme for transformerless operation of DVR to maintain load voltage at a constant value during voltage disturbance viz., sag and swells. The mathematical model of TDVR system is presented and the detailed description of proposed control scheme is also discussed. Further the

chapter concludes with the simulation and experimental results of TDVR system with proposed control.

Chapter 7: This chapter explores the different modes in which series converter can work when it is acting as an interface between the utility supply and the dc microgrid. Comprehensive analysis and design of control algorithms for the various modes are discussed. Finally, the simulation results of the series interfacing converter in hybrid microgrid environment are presented for various modes of operation.

Chapter 8: Summarizes the thesis major contributions and includes some discussions on possible future research.

Chapter 2

Literature Survey

Contents

2.1 Introduction

As mentioned in the previous chapter Power Quality (PQ) has become a serious concern with deregulation of energy markets and increased use of non-linear loads.Among the power quality events voltage sags, voltage swells and harmonics are some of the most commonly occurring momentary disturbances which affects the quality of power supplied to the industrial consumers. To prevent from the effects of voltage disturbances on the sensitive loads, different solutions are available. The most effective and flexible solution is to use power electronic devices as compensators. These compensators include series and parallel and series-parallel compensators which are called custom power devices (Gyugyi, 1992), (Gyugyi et al., 1995) as discussed in the previous chapter. The series compensators such as Static Series Compensator (SSC), Dynamic Voltage Restorers (DVR) are considered to be the most economical solutions to compensate voltage disturbances in distribution systems. Although, the control strategies and purposes of these compensators may differ from each other, but their operation principle and power circuit architecture are the same. However, the name DVR is mostly used for a series compensator, which compensates the voltage sags/swells.

The current thesis work discuss about investigating the control strategies for multi-mode operation of series interfacing converter. The multi-mode operation in the thesis refers to the different modes of operating the series converter in distribution system and in Hybrid Microgrid (HMG) environment. In the distriution system the installation of series converter act as custom power device as mentioned earlier to compensate the voltage disturbances and also mitigate the harmonics. On the other hand the series converter in the HMG act as interlinking converter (IC) between AC and DC microgrid. This application of series converter as IC facilitates to additional desired operating features for HMG viz., AC and DC bus voltage control, fault control on either side and power management between the AC and DC grids. In this regrad the literature survey is carried out mainly focussing on the control strategies to be employed for achieving effective multi-mode operation of series converter. The survey

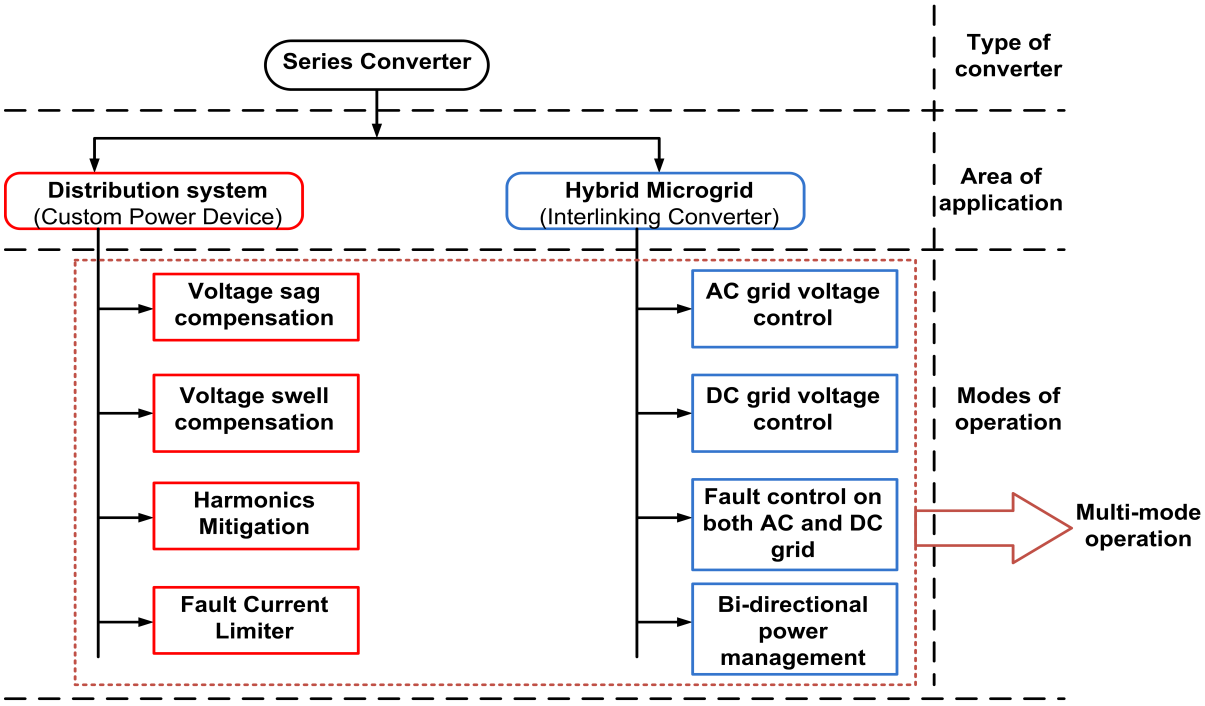


Figure 2.1: Multi-mode operation of series converter

comprises both application of series converter in distribution system and in HMG. Firstly the structure, control techniques for operating the series converter in distribution system is presented. Later the structure and control of series converter as IC in HMG is discussed.

2.2 Series converter operation as custom power device in distribution system

As mentioned earlier there are different types of series converter which are considered as custom power devices but Dynamic Voltage Restorer (DVR) is considered as economic solution. Thus in the current thesis work DVR is considered as series converter. The schematic of DVR is shown in Figure 2.2. It is connected in series between the source and load to maintain load voltage constant at its rated value even when voltage disturbances such as voltage sags, voltage swells occur at the source. It consists of a voltage source inverter (VSI), injection transformer, a control unit,

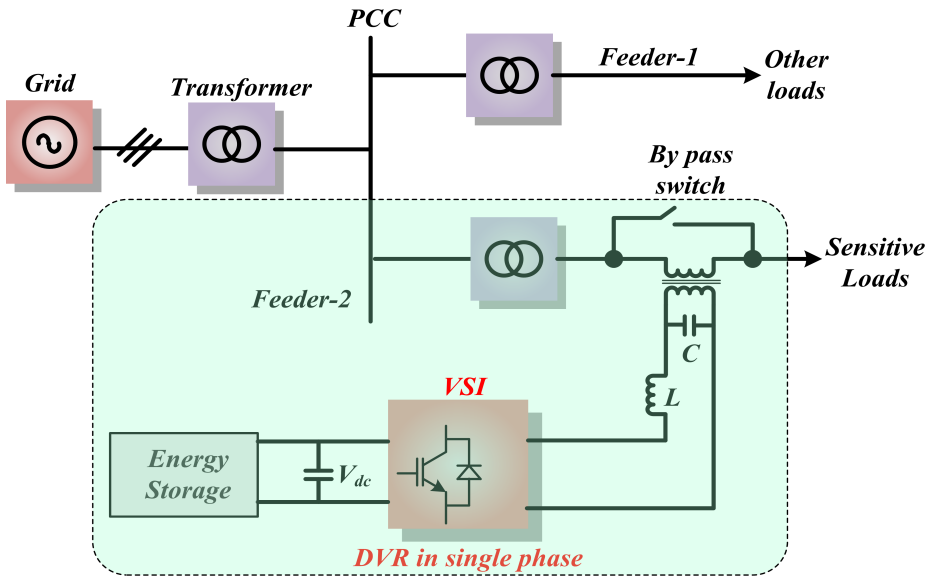


Figure 2.2: Schematic diagram of a typical DVR.

and LC filter. When voltage sag occurs the control unit senses the voltage, calculates the sag depth and voltage to be injected. It generates PWM switching pulses for the VSI to generate the voltage to be injected. An LC filter connected at the output of VSI removes high frequency switching harmonics. The output of LC filter is connected to an injection transformer which injects the voltage in series with the supply. Thus the voltage across the load is maintained constant even under abnormal voltage conditions.

2.2.1 Modes of Operation

There are three modes of operation for DVR, i.e., standby mode, injection mode (active mode), and the protection mode (Tmay et al., 2005).

1. **Standby mode:**This mode refers to no voltage disturbance on the grid voltage and hence DVR is not required to inject voltage to the grid. In this mode of operation, the DVR is usually bypassed using the bypass switch to avoid inverse effect on the line voltage during normal operation. Generally, the DVR is in standby mode and therefore, bypassing the DVR in this mode will prevent power losses in the DVR circuit.

2. **Injection mode:**If DVR control circuit detects the voltage disturbance then

the bypass switch is opened and the DVR enters to the injection mode in which the required compensation voltage is injected to the grid. This mode is also known as compensation mode. The DVR injection mode ends when the load voltage is recovered to its nominal value.

3. **Protection mode:** A short circuit fault on the downstream of the DVR (on the load side) causes high fault current. Without protection, this current flows through the injection transformer and hence reflected to the converter side. This fault current can destroy the DVR system including the injection transformer, the converter, the DC-link elements(capacitors) and the AC filters. Therefore, it is necessary to detect the downstream fault and protect the DVR against it.

2.2.2 Control strategies of series converter (DVR) for compensating voltage disturbances

The block diagram of a typical control system for DVR is shown in Figure 2.3. The input data to the control system is the measured voltage on the source/load side, measured line current and pre-settings such as nominal value of voltage and threshold for voltage sag/swell detection. Voltage and current on the grid or load side (or both sides) are measured and given to the operation mode selection and voltage disturbance detection unit. This unit decides the operation mode of the DVR, which can be the standby mode, compensation mode or protection mode. If the mode is standby, then all of the converter switches are turned off and the bypass switch is turned on. When a downstream fault current is detected, the DVR goes to the protection mode and the protection scheme is activated.Once a voltage disturbance is detected, the DVR goes to the compensation mode and the reference generation unit is activated. This unit generates the voltage that should be provided and injected by the DVR. In fact, the output of the reference generation unit is the DVR output reference voltage. In case that an open loop control is used, the output of the reference generation unit can be divided by the DC link voltage to provide the reference voltage for PWM. However, the closed loop control is preferred. In closed loop control, the output of the reference generation unit is fed to the voltage and current controllers. The output of these controllers is the reference voltage of the PWM. The reference voltage is applied to a PWM pulse generator and the generated pulses are applied to the converter. It should be noted that the input data is not only the measured voltages but also

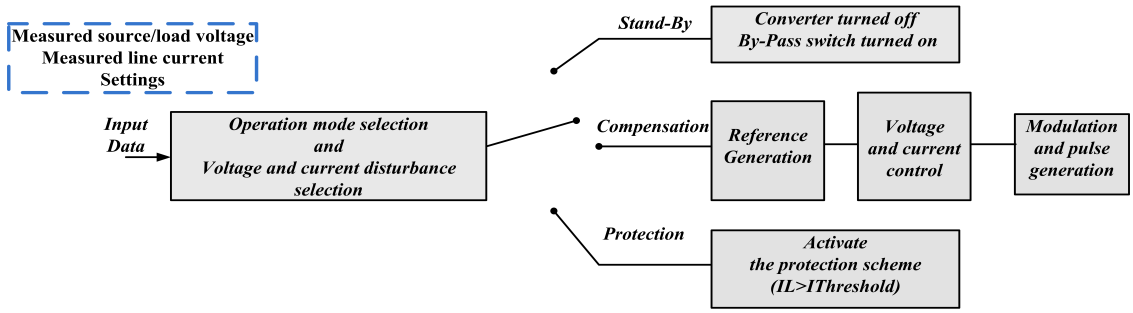


Figure 2.3: Schematic diagram of control system for DVR

additional information is necessary to control the DVR. This information includes but not limited to value of the filter capacitor current, adopted control strategy and DC-link voltage.

2.2.3 Control

A proper control and PWM scheme should be adopted to ensure a distortion free output voltage waveform at the output terminals of DVR. This control algorithm is expected to be robust to load and supply disturbances (Akagi et al., 1984) (Vilathgamuwa et al., 2002a).

Open loop ensures unconditional stability but absolute stability itself is not enough to determine the performance of a system, relative stability should also be considered while designing a control scheme for a system. Phase and gain margin must be good enough to ensure a good dynamic response of the system, which may not be the case when system is operating in open loop. Literature map of existing DVR control are presented in Figure 2.4.

Enough damping to the output voltage must be ensured by the controller as the system is connected to LC output filter. Poor damping of LC resonance leads to distortion of output voltage of the DVR (Vilathgamuwa et al., 2002a). Also voltage drop can occur in filter, transformer impedance and DVR may not be able to restore the load voltage to reference value when operated under open loop. Hence a closed loop control is necessary to ensure stability, good dynamic and steady state response of DVR.

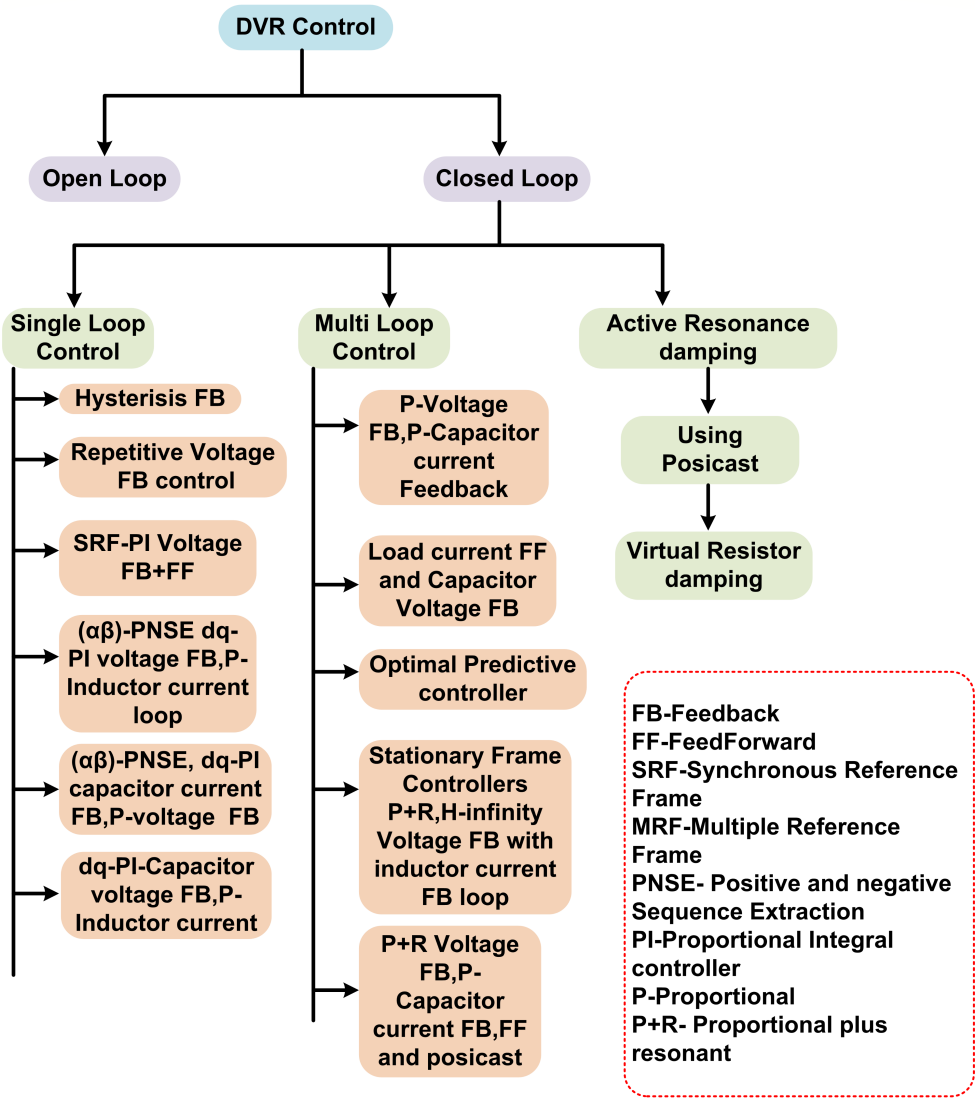


Figure 2.4: Literature review of DVR control structures

2.2.3.1 Closedloop loop control

Open Loop control has a low relative stability and offers less damping. Also it cannot accurately track the DVR reference voltage. Hence closed loop control is usually preferred. It can be classified based on number of feedback loops used as:

a) **Single loop control** Single loop control uses a single voltage feedback Loop. The feedback parameter i.e., measured DVR voltage(dq) is compared with reference DVR voltage. Well known controllers such as PI controllers can be used to track DVR voltages by using reference frame theory. PI controller implemented

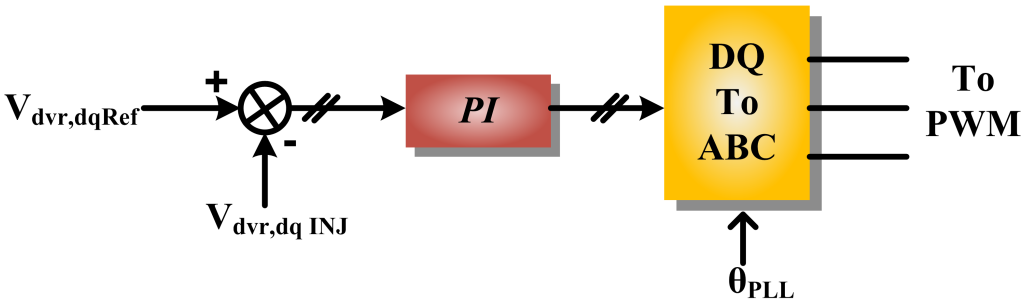


Figure 2.5: Voltage feedback with SRF-PI controller

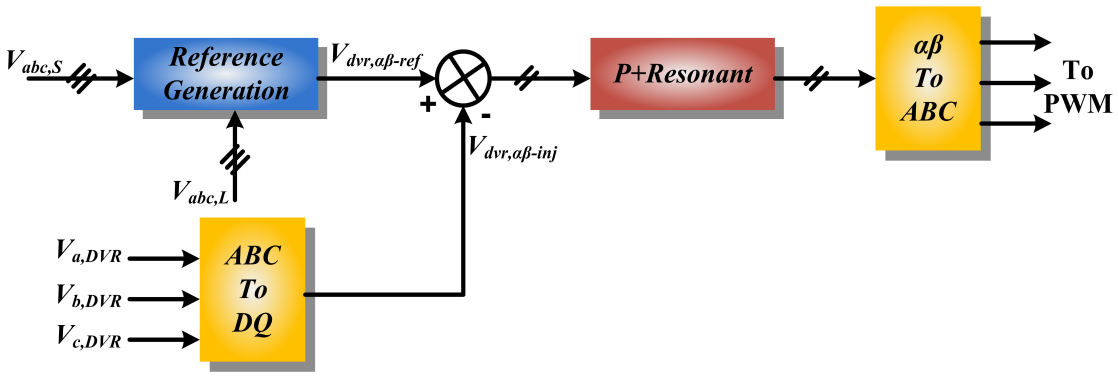


Figure 2.6: Voltage Feedback with Stationary frame controller

in synchronous reference frame, called SRF-PI controller, (Nielsen et al., 2004), (Meyer et al., 2008), (Babaei et al., 2014), (Newman et al., 2005) is shown in Figure 2.5

SRF-PI controllers can track reference voltages accurately resulting in zero steady state error. Large gains needed for good steady state and transient response of PI controller could cause instability. Hence a P+Resnonance control can be used as an alternative which is obtained by transforming PI- controller from synchronous frame to stationary $\alpha\beta$-frame.

$$G_{PR} = K_P + \frac{2K_I s}{s^2 + \omega_0^2} \tag{2.1}$$

where ω_0 is the fundamental frequency, K_P is the proportional constant and K_I is the integral constant. A stationary frame P+Resonant controller is shown in Figure 2.6. It offers inifinite gain at the fundamental frequency for both positive and negative sequence, but it has a very narrow bandwidth and thereby sensitive

to frequency variations. Thus a more practical model is obtained in (Li et al., 2007a), (Zmood et al., 2001a) which is given below.

$$G_{PR} = K_P + \frac{2K_I\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_0^2} \tag{2.2}$$

Where ω_{cut} is the cutoff frequency around resonance peak. This practical P+R controller is robust to fundamental frequency variations as the bandwidth around the resonant peak is increased. The overall bandwidth of this controller is very narrow resulting in a very slow response and hence a feedforward is added to speed up the response (Zmood et al., 2001b). However addition of feedforward leads to increase in resonant peak causing amplification of frequencies around resonance. Apart from the controllers discussed a repetitive controller is suggested in (Roncero-Sanchez et al., 2009), (Roncero-Sanchez and Acha, 2009) and a non-linear hysteresis control is proposed in (Kanjiya et al., 2013), (Jowder, 2009).

b) **Multi loop control:** Single loop control can lead to zero steady state error but it amplifies higher order frequencies around resonant frequency hence a multi loop controller is proposed in (Vilathgamuwa et al., 2002b),(Hyosung Kim and Seung-Ki Sul, 2005),(Li et al., 2007c),(Li et al., 2007d), (Li et al., 2007b),(Cheng et al., 2007).

Figure 2.7 shows Multi Loop controller implemented using capacitor current as second feedback loop (Vilathgamuwa et al., 2002b). Reference DVR voltages are compared with actual injected DVR voltages and the error is multiplied by a gain K_V to give reference capacitor current I_C^* . Capacitor current is taken as feedback and compared with virtual capacitor reference current I_C^* and the error is given to a current gain K_I. This output is given to PWM as reference voltage to generate switching pulses. The voltage feedback loop ensures that injected voltage tracks the reference voltage, where as current feedback loop ensures load current disturbance rejection and flattens the resonance peak. A voltage feed forward path is added to improve the speed of the system response and track the changes in reference DVR voltages quickly.

In (Hyosung Kim and Seung-Ki Sul, 2005) load current is taken as feedforward for inner current loop and the controller gains are designed to have better band-

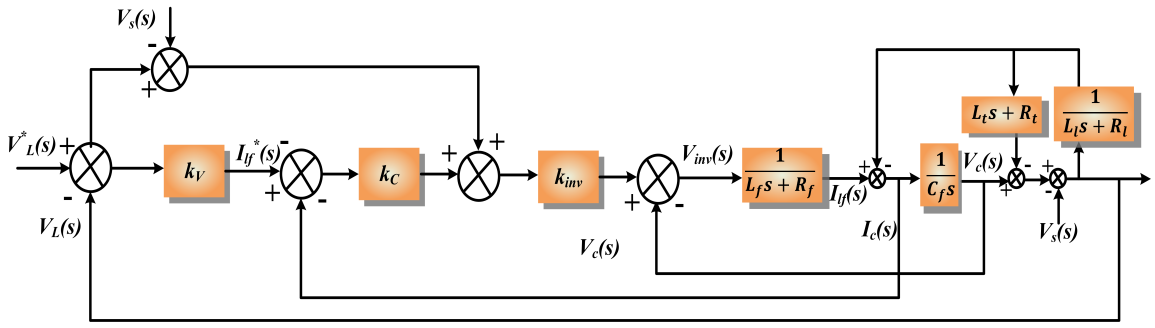


Figure 2.7: Multiloop controller

width. Voltage loop for DVR control should be designed with more bandwidth as it also involves injection of harmonics under distorted grid.

In (Li et al., 2007d) stationary frame H-infinity control (Robust) is proposed and its design also presented. In (Li et al., 2007b) H-infinity control is compared with P+Resonant controller and robustness of both controllers is tested at 2/3rd of system parameter variations (L and C). Parameter variations seem to have no major effect on H-infinity controlled system and its robustness is verified. P+R control is not robust to parameter variations and hence the injected voltage would be distorted.

In (Wang and Illindala, 2006a),(Babaei et al., 2014),(Cheng et al., 2007) positive and negative sequences are extracted and are controlled separately by using two different SRF-controllers. In (Wang and Illindala, 2006a) complex filters are used to extract positive and negative sequences from stationary $\alpha\beta$-frame and then they are converted to dq-frame. d-axis and q-axis networks are decoupled so that each axis can be individually controlled. In (Babaei et al., 2014) weighted recursive least squares is used to extract sequence components from stationary frame, and similar SRF-controller is used.

In (Chen et al., 2014) multiple references frames are used to extract the positive, negative sequence components of fundamental and harmonic voltages. Single PI controller is not enough to track all harmonic components in the DVR reference voltage. Hence a decoupled Multiple reference frame extracts sequence components of harmonics as well. Each harmonic sequence component is independently controlled by a set of PI controllers.

In (Newman et al., 2005) idea of operating DVR under steady state as ac-

tive series voltage filter is discussed, which eliminates selected harmonics under steady state operation and mitigates transient voltage disturbances like sags as well. P+Resonant filter is used to extract specific harmonic voltage as it offers large gains at the resonant frequency (fundamental frequency in this case) of the filter. In steady state operation DVR acts as active filter and eliminates these harmonics such that load voltage distortion is reduced. However it is also cautioned that the economic savings by operating it under steady state must be better as there are also losses in the equipment when operated in steady state.

Thus from the above it can be summarised as in open loop control the frequency response of the system has inadequate phase and gain margin. Further the damping of the system with open loop control of DVR is unsatisfactory .In single loop voltage control the trade-off between steady state response, transient response and stability is quite demanding because large control gains are generally required for good steady state and transient performance but it generally deteriorate the system stability. On the other hand if smaller gain is used to ensure adequate stability margin a significant steady state error may appear and system may react much slower. Thus a multiloop control scheme is adopted due to its flexibility to design and to avoid the issues related to single loop control scheme. In multiloop controller generally two loops have been considered, the outer loop as voltage feedback which aims for regulating the load voltage and the inner loop as current feedback which enhances the dynamic response and gives protection against overcurrent.

2.3 The Problem of Grid Phase Detection

To generate the synchronized reference signal V_{abc} required for PWM block, the DVR system should detect the grid phase angle $theta$ from the grid voltage signal $Vabc$ during compensation mode. Ideally, θ can be mathematically calculated from the sensed values of V_{abc}. However, in practice, V_{abc} is contaminated by persistent power quality disturbances and sensing noises. As a result, detecting $theta$ normally necessitates for signal processing techniques, thereby necessitating for more sophisticated detection systems.

Regardless of how the grid phase detection techniques are implemented, their fundamental goals remains same and as follows:

a) Accurately isolate the positive-sequence fundamental component of V_{abc}.

b) Promptly track θ during various short-term disturbances (phase jumps, frequency variations, voltage sags and swells, etc), and

c) Stably adapt to varied working conditions (grid voltage and frequency shifts, etc).

Apart from the basic objectives, other factors viz., computational complexity, the storage overhead, the robustness in varying working conditions, etc should be taken into account. Since these conditions are often convicted in nature, a number of grid phase detection schemes have been established by weighing various factors against their advantages and certain trade-offs. They are discussed in the following subsection.

2.3.1 State of art

As shown in Figure 2.9, the popular grid phase detection techniques can be generally categorized as frequency-domain and the time-domain methods. Discrete Fourier transform (DFT) and fast Fourier transform (FFT) are the most well-known frequency-domain detection methods (FFT) (McGrath et al., 2005),(Gonzalez et al., 2007). DFT transforms the discrete time-domain signal into the frequency domain, and determines the magnitude and the phase angle of all harmonic components up to the Nyquist frequency, including the fundamental one as well. FFT improves DFT by significantly reducing the number of calculations when certain criteria can be met. In real-time control systems, the input signal is repetitively sampled and updated through A/D conversion. Therefore, DFT is modified into the sliding DFT (SDFT), also known as the recursive DFT (RDFT), (Jacobsen and Lyons, 2003), (Jacobsen and Lyons, 2004). Besides DFT, FFT and SDFT, there are also other frequency-domain methods based on non-Fourier transforms, such as Kalman filtering and discrete cosine transform (Padua et al., 2007), (Moreno et al., 2007).

The assessment of these approaches with standardized experimental settings (Asiminoaei et al., 2005), (Asiminoaei et al., 2007) shows that frequency-domain methods exhibits at least one cycle settling period and require more data storage or computing resources. Therefore, these methods are more appropriate for harmonic metering

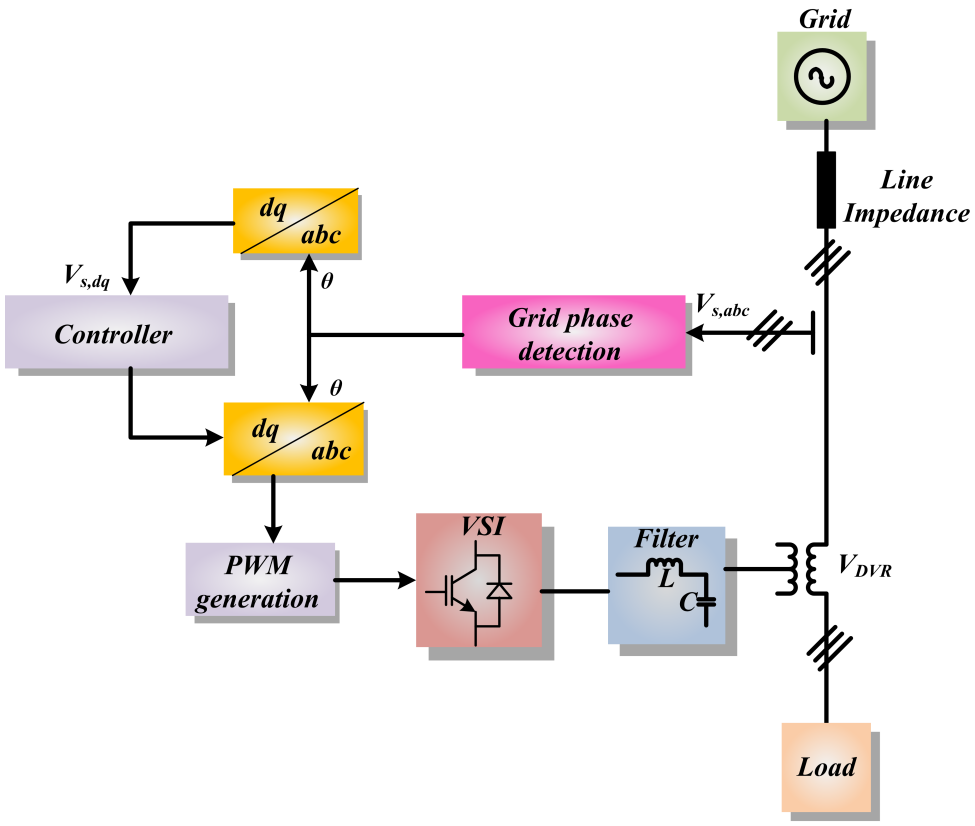


Figure 2.8: Location of grid phase detection block in DVR system

and monitoring. Time-domain techniques on the other hand work well for real-time control purpose.

Time domain appraoches are further subdivided into two methods: (1) open loop and (2) closed loop based. The classification is based on the type of detection method architecture. The open-loop methods include the improved arctangent method with component filtering, arctangent method, and the space vector Filtering (SVF) method (McGranaghan et al., 1993) (Svensson, 2001). The closed-loop methods include the weighted least square estimation (WLSE), the zero-crossings detection (ZCD), adaptive notch filtering (ANF), and the phase-locked loop (PLL) techniques (Xiaoqiang et al., 2008) (Choi et al., 2006).

The most basic open-loop method is based on four-quadrant arctangent calculation. This method transforms the abc-frame grid voltage signal v_{abc} into the $\alpha\beta$-frame by Clarke transformation, and the resulted $v_{\alpha\beta}$ can then be used to calculate the

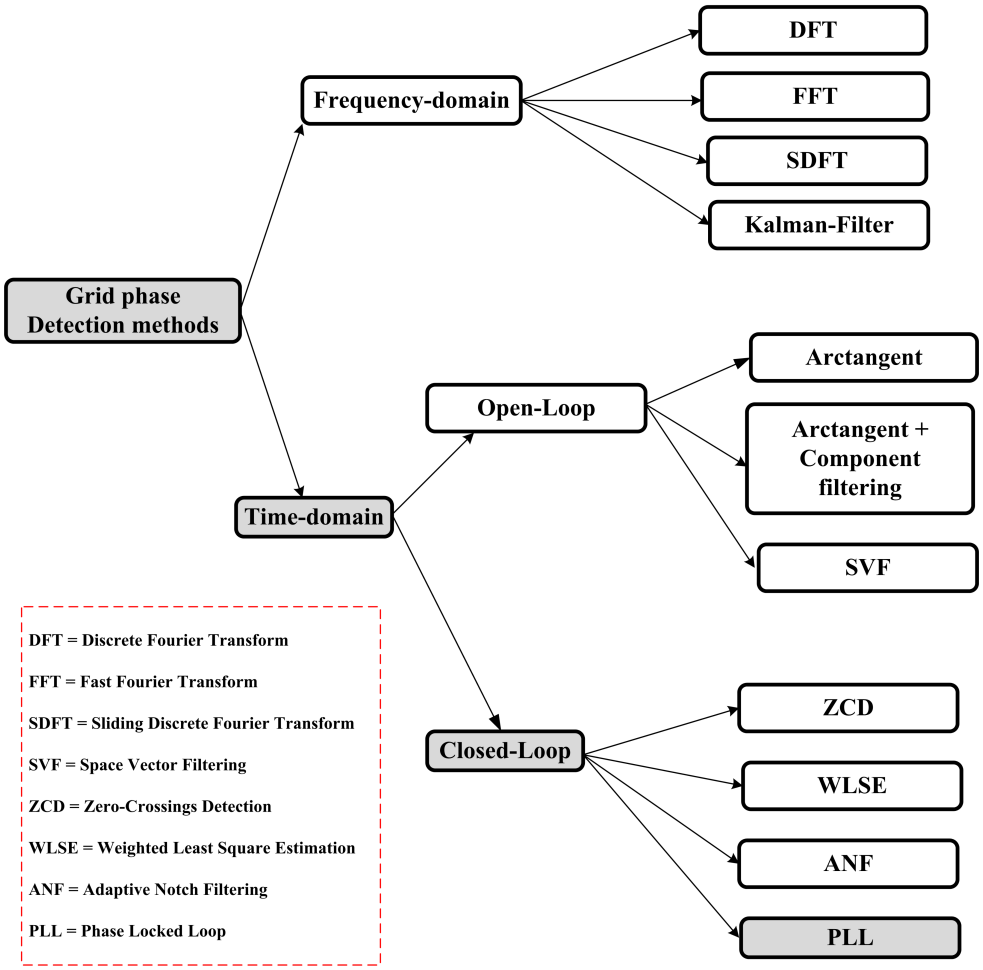


Figure 2.9: Classiffication of the common grid phase detection methods

phase angle θ. All harmonics and other disturbances in $v_{\alpha\beta}$ are reflected in θ also. Thus (McGranaghan et al., 1993) adopts a low-pass or band pass filters to filter out harmonic components in $\alpha\beta$ before doing the arctangent calculation. Such filters cannot however deal with the voltage imbalance, since the uneven signal can be divided into the positive and negative components of the series, which have the same fundamental frequency.

SVF method (Svensson, 2001) maintains an approximate local signal $\hat{v}_{\alpha\beta}$. The detected $v_{\alpha\beta}$ is transformed into $\hat{v}_{\alpha\beta}$ by combining with a weighting factor continuously, while θ is derived from the combined result. A technique like this can "cushion" sudden fluctuations in signal, but it is ineffective against steady-state disruptions like

harmonics.

Closed-loop techniques, on the other hand, involve one or more control loops and thereby gain greater precision and controllability. The easiest one is ZCD, which repeatedly resets when a zero-crossing point in the voltage signal is observed (Xiaoqiang et al., 2008), or uses a lead-lag relation and changes based on zero crossings (Choi et al., 2006). ZCD is normally very sluggish as the algorithm updates only for every half cycle; it is also susceptible to noise and fuss (Gardner, 1984).

The core principle of WLSE methods (Song and Nam, 2000), (Song et al., 2002) is to approximate and equate the cumulative product of all harmonic components present in the input signal with the real input. The error is then used to update the estimates by evaluating a covariance matrix. In (Vidal et al., 2010), a new version of WLSE is proposed where authors extracted real time grid frequency information by adding PLL to the scheme. The covariance matrix enlarges squarely in all these schemes with the increase of the number of harmonics to predict, and making it extremely difficult for the computing platform to handle when a wide range of harmonics are present.

As the name implies, ANF-based approaches separate the fundamental and harmonic components using a cluster of notch filters. This appraoch involves many blocks and one among them isolates the fundamental block (named as "Master ANF Block" to differentiate between the "Slave ANF Blocks" which isolate the other harmonic components). The output of this particular block is estimated fundamental frequency which inturn is used to adjust the filter parameters of other ANF blocks. Since such an adaptation mechanism is inherently sluggish, the response of ANF systems to a load change often exceeds a few cycles (Yazdani et al., 2008), (Yazdani et al., 2009).

The PLL has a long background in the field of ac signal monitoring (Hsieh and Hung, 1997),(Lai and Nakano, 1997). Because of its simple architecture and high tolerance for various problem backgrounds, it has been commonly used for grid phase detection (and other information) (Xiaoqiang et al., 2008). As a result, a large family of PLL systems has emerged, which can be divided into simple and advanced PLLs as shown in Figure 2.10.

The simple three-phase PLL can be built using either the synchronous reference frame tool (dq-frame) or the principle of instantaneous power (pq power); thus the dqPLL (also known as SRF-PLL) (Kaura and Blasko, 1997), (Chung, 2000) and

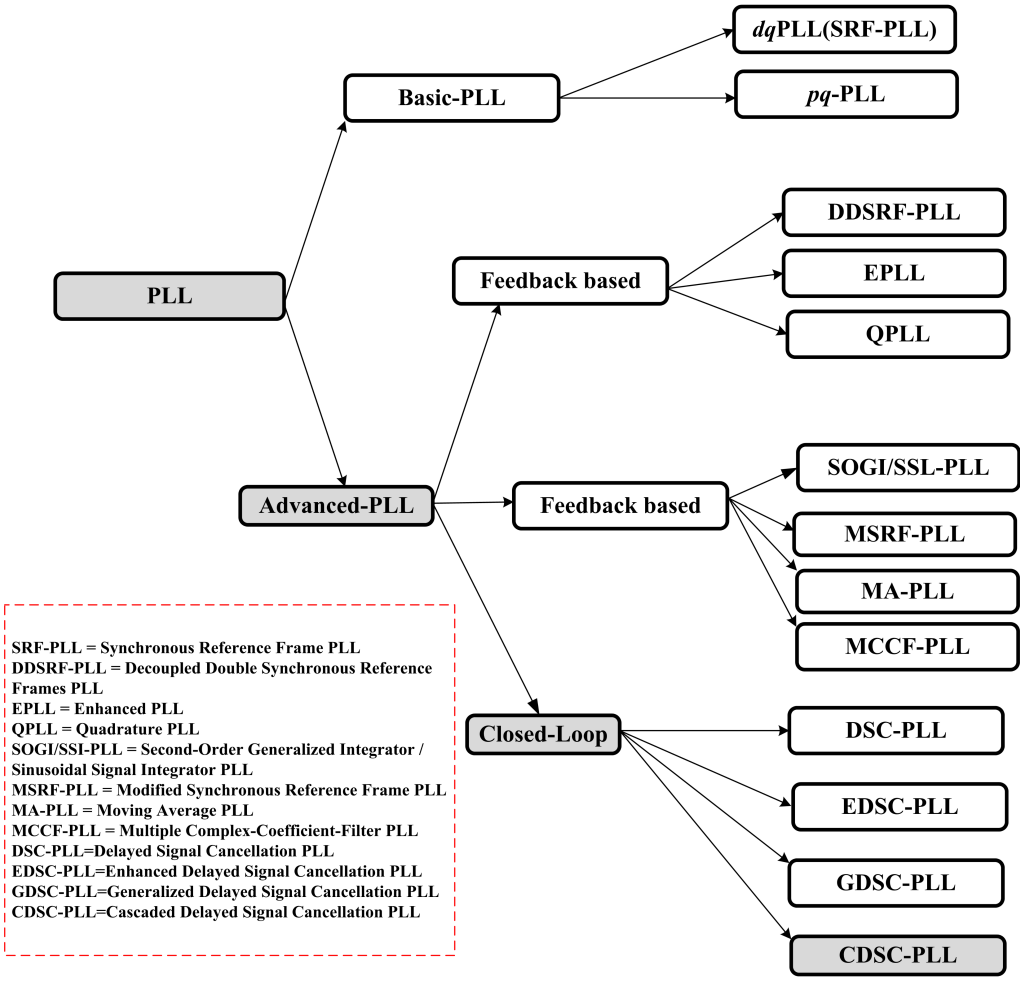


Figure 2.10: Classification of the common grid phase detection PLLs

*pq*PLL (Rolim et al., 2007), (Liccardo et al., 2011) schemes are mathematically equivalent to each other. Take, for example, the *dq* PLL, which accepts three-phase voltage/current signal as input and outputs estimates of the signal's amplitude, frequency, and phase angle. Higher bandwidth increases the transient response of the system but degrades harmonic immunity and on other hand The result of a lower bandwidth is quite opposite Chung (2000), (Bueno et al., 2005). Thus the trade-off between these two aspects would determine the actual PLL bandwidth. The PLL tuning becomes extremely difficult when the input signal is unbalanced as negative sequence components occurs in the *dq* frame. In order to eliminate the effect of negative sequence components a very low bandwidth is required thereby leads to slow system dynamics.

As a result, a natural idea is to incorporate a harmonic suppressing function into the PLL structure to prevent the compromise as described above. Inspired by this idea different advanced PLLs are developed and are categorized into three types feedback-based, the filtering-based and the signal delay-based ones.

The decoupled double synchronous reference frame PLL (DDSRF-PLL) (Rodriguez et al., 2007), (Rodriguez et al., 2008) which belongs to feedback separates the positive and negative-sequence elements by transforming the input into two sets of oppositely rotating dq-frames and using their respective outputs in various feedback loops. However, input harmonics are not taken into account in this design. Enhanced-PLL (EPLL) (Karimi and Iravani, 2004), (Karimi-Ghartemani and Reza Iravani, 2003) and quadrature PLL (QPLL) (Karimi et al., 2004) use the output estimates along with the input in a dynamic phase detector (PD) block to calculate the error and change accordingly. The two systems (EPLL for three-phase signals and QPLL for single-phase signals) have transient response times ranging from 30 to more than 60 ms, which is significantly longer than the filter and signal delay-based PLL schemes.

Filters which are carefully designed for filtering-based advanced PLLs can be applied to either the $\alpha\beta$ -or the dq-frame signal. Examples of dq-frame filtering include moving average PLL (MA-PLL) (Freijedo et al., 2009a), (Freijedo et al., 2009b) modified synchronous reference frame PLL (MSRF-PLL), and autoadjustable synchronous reference frame PLL (ASRF-PLL) (Minambres et al., 2009). The fact that the textitdq-frame filters are positioned within the PLL control loop, which impacts system stability when the loop gain is large, is their typical difficulty. Examples of $\alpha\beta$-frame filtering include multiple complex-coefficient-filter PLL (MCCF-PLL) (Guo et al., 2011) and second-order generalized integrator PLL (SOGI-PLL) (Rodriguez et al., 2006). SOGI is also known as sinusoidal signal integrator (SSI) (Yuan et al., 2002), (Bojoi et al., 2005). Both MCCF and SOGI essentially perform resonant filtering (at the fundamental and/or the harmonic frequencies). They are known to have a few drawbacks, such as the incomplete harmonic rejection, as well as the sensitivity in the magnitude and the phase responses around the resonant points.

Signal delay-based PLL schemes are among the most recently emerged advanced PLLs. Their common idea is to construct operators that associate the input signal and its delayed versions. In terms of signal processing, the signal delay-based operators can be regarded as finite impulse response (FIR) filters of higher-order, which are capable of more flexible harmonic suppressing.

Though, numerous advanced PLL schemes have been proposed. Among them, CDSC-PLL proves to be superior in terms of harmonic elimination ability, transient response, frequency adaptability. It also features small memory overhead and light computational burden. As suggested by the name, CDSC-PLL is formed as a PLL system augmented by the CDSC operator. The CDSC operator processes the input voltage signal and eliminates the harmonics it contains, leaving a pure signal to the PLL system. As a result, the PLL bandwidth can be set to a very high value to achieve excellent system dynamics, while no steady-state detection error arises due to the impact of the input harmonics. Thus CDSC-PLL is adopted for the DVR system to obtain the angle and frequency information of the system.

2.4 Control strategies for operation of series converter (DVR) as FCL to compensate downstream faults in distribution system

Over-currents are known to be the dominant cause of power system component failures or deterioration from full functionality. Some of these effects may remain unknown and could later result in catastrophic failures of the entire or large portions of the system. There are plenty of devices/methods available to limit the undesirable consequences of the over-current events. These devices/methods have great impact on system reliability by reducing stress on power system components and increasing their useful lifetime. Due to the importance of the subject, there is tremendous need to analyze and compare these devices/methods in terms of reliability.

Over-currents mainly occurs due to short circuit faults and also due to overloading of the system. Short circuit currents (also called fault currents) are known to be the dominant cause of power system component failures or deterioration from full functionality (Smeets et al., 2003). It is a common practice to use *Fault Current Limiters* (FCLs) and protection devices to eliminate undesirable impacts of short circuit currents. They do so by reducing the magnitude of the fault current and further reduces the time of exposure to fault current. On the other hand short circuit can cause catastrophes by posing huge amount of stress and mechanical forces in a very short amount of time, overloads can also raise serious issues due to much longer periods of exposure. Overcoming overloads problems usually requires control

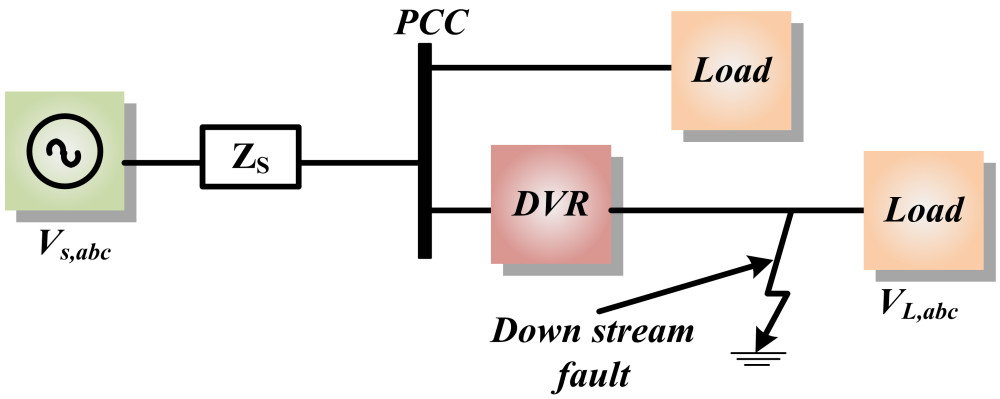


Figure 2.11: Downstream fault in DVR connected system

strategies such as generation rescheduling and/or load shedding, and optimized usage of existing assets.

Though circuit breakers and fuses emerged as the protection equipment of choice in the power system but have serious limitations and unwanted side effects. Circuit breakers interrupt the supply of power to the consumer. Thus in this situation i.e., increase in the issues related to large fault currents FCLs are becoming the preferred option to address the aforementioned problem.

Thus in this section the issue related to downstream faults in a distribution system with series converter (DVR) installed in the line is discussed. During the downstream fault large fault currents will flow through the DVR before the opening of a circuit breaker(Figure 2.11). This large fault current will cause PCC voltage drop, which would affect the MV or LV loads on the other feeders connected to PCC. Furthermore, if not controlled properly, DVR might also contribute to the PCC voltage drop in the process of compensating the required voltage, thus further worsening the fault situation. Thus in this section existing methods proposed in the literature for controlling fault current are discussed.

2.4.1 Fault current scenario in DVR system

Despite the advantages of implementing at medium voltage level, the DVR is subjected to increased downstream faults as it covers large number of loads. The downstream faults could cause large fault current flow, which might damage the series connected equipment (such as DVR) and system components. The large fault cur-

rent will also cause voltage at PCC to drop and affect most other loads on the parallel feeders connected to PCC.The DVR might further complicate the fault situation in the process of compensating the PCC voltage sag which could result in even large fault current, if not controlled properly.

An often used option for DVR operation during a downstream fault is to passively protect the DVR by enabling the bypass circuit (usually a slow mechanical bypass together with a fast solid-state switch) (Woodley et al., 1999), (Lee et al., 2002). However, large fault current flow would sustain and PCC voltage would drop. A more promising approach is thus to control the DVR actively to reduce the large fault current and restore the PCC voltage.

The DVR is connected in series with the electricity supply via transformer coupling to provide voltage support in the event of voltage sag/swell or disturbances from the supply side. This presents an imminent danger to the DVR when there is excess current flowing from the supply. Such a situation may arise due to several reasons but primarily as a result of short circuits at the load side. As the excessive current is also reflected in the secondary side of the injection transformer, the power semiconductor devices need to be protected.

For effective utilization of DVR it requires a special protection scheme (Lee et al., 2002). The compensating voltage is injected in series with the source by means of the primary of the injection transformer. As noted in (Vilathgamuwa et al., 2006), the transformer operates as a current transformer and hence the secondary cannot be opened during a fault in the distribution system. Otherwise, excessive voltages would appear on the secondary side. Therefore the series compensator cannot be protected with circuit breakers or fuses. A failure to balance the mmf from the primary winding will cause the transformer to be driven into excessive magnetic saturation. Rather, a path must be provided for the flow of the referred (secondary) current. If the current flows through the VSI, the DC bus voltage will rapidly increase, even when the VSI is disabled (Choi et al., 2005).

As a path for the secondary current must be provided, the performance of varistors and other protection devices in parallel with the secondary of the series transformer have been investigated (Lee et al., 2002), (Choi et al., 2005). In the event of a fault in a distribution network, the fault is cleared after a duration, which is determined by the time delay imposed by the protection system. This delay in turn is determined by the response time of the switching devices and the requirements of the protection

co-ordination. As noted in (Lee et al., 2002), total clearing time of a low-voltage circuit breaker depends on the amplitude of the fault current, but usually has a minimum value higher than 45 ms, whilst the minimum clearing time can exceed 100 ms for medium-voltage applications. Thus, the duration of the fault is a significant parameter in relation to the ability of the inverter to withstand the fault but also with regard to the ability of the varistors to accommodate the excessive current. In general, the power electronic devices of the series compensator will be the most vulnerable elements to system faults.

Additional protection hardware could be used, as proposed in (Lee et al., 2002), but this involves additional cost and energy dissipation. The scheme stated in this thesis involves an additional control function combined with the normal DVR operating scheme. To protect against the fault currents from exceeding the converter rating, DVR may make use of a bypass scheme to protect the power electronics switching devices. Protection can be provided by a solid-state SCR thyristor shorting switch that closes across the secondary terminals of the injection transformer when a downstream fault occurs (Woodley et al., 1999). While the Bypass switch is effective in protecting DVR, it cannot mitigate the impact of the fault on the parallel loads. Hence, the scheme does not completely solve the problem.

2.4.2 Existing methods

2.4.2.1 *Reverse Voltage Injection Method*

When the downstream fault occurs at load side, thus V_{Load}=0. To decrease the fault current, DVR can be controlled in a way that it reduces the fault current to its pre-fault status by injecting a reverse voltage to grid:

$$V_{DVR} = V_s - Z_s I_{Load(pre-fault)} \tag{2.3}$$

Figure 2.12 shows the phasor diagram of the voltages. V_{Line} indicates the voltage drop in the feeder line with source impedance Z_S, V_{SC} and V_S are the voltages injected by DVR and the voltage of main feeder respectively. If the fault current is reduced to a constant value, V_{Line} will fall in the dotted circle depend on the voltage injected by series compensator. Because Z_S is typically very small, the radius of the dotted circle is very short. So the maximum voltage output of the series compensator must

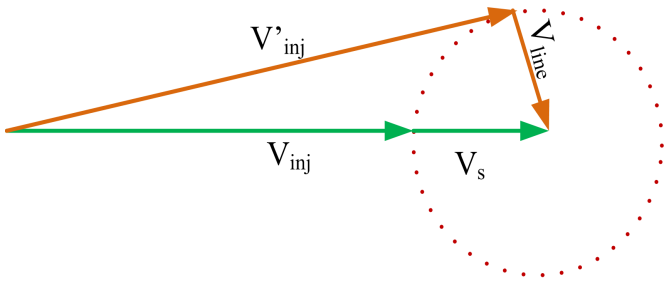


Figure 2.12: Phasor diagram of the voltages during fault occurrence

be close to the rated line voltage. For series-connected devices,the current rating is equal to the rated load current, so under this situation the power capacity of the series compensator must be equal to the load capacity, which will severely restrict the application of this method, because normally the power capacity of the series-connected devices is only about 50% of the load capacity (Marei et al., 2007). This is first limitation of the particular method.

Secondly, the reduced fault-current of fault current limiter (FCL) must satisfy the condition as shown in (2.3)

$$I_{relay} < I_{fcl} < I_{break} \tag{2.4}$$

where I_{fcl}, I_{relay} and I_{break} are the fault current when FCL works, current level at which protective (over-current and directional over-current) relays operate, and current level above which circuit breakers will be damaged, respectively. But for this control method, the fault current is restricted to below the rated current of the power converter, which is well below the current level of the protective relay. So under this situation the relay will not act. Though some remedial measures have been proposed, such as the utilization of existing feeder protection system to activate series compensator (Axente et al., 2006), this control method can't be widely used. The third shortcoming of this method is that very quick response of control system is required. The current rating of the DVR has to increase due to the current surge at the beginning of the downstream fault and before the FCL action can be affected completely. The advantage of this approach is that no any additional cost is added.

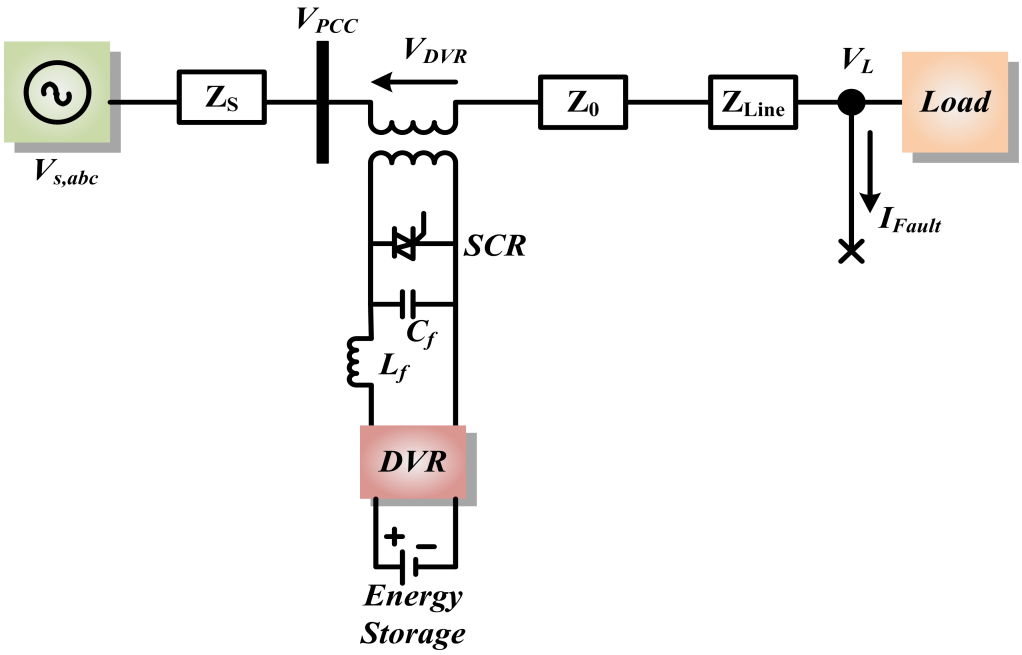


Figure 2.13: Adding additional reactor method (Method A)

2.4.2.2 *Shutting Down the Power Converter Method*

For this method, the power converter is shut down when downstream fault happens and bypassed through SCR as shown in Figure 2.13 Under this condition, the leakage reactance of injection transformer Z_{tr} is inserted to the power line to limit the fault current.

$$I_{limited} = \frac{V_s}{Z_s + Z_{tr}} \tag{2.5}$$

The advantage of this method is that it is actually equivalent to the passive protection method proposed in (Woodley et al., 1999). This is in fact an add-on feature of the commonly used passive protection method with no additional cost to be added. But typically the leakage reactance of the injection transformer is intentionally designed to be a very low value to decrease the voltage drop in normal condition, so fault current limiting ability will be very limited.

2.4.2.3 *Additional reactor Method*

Intentionally increase the leakage reactance of the injection transformer, or add an additional reactor Z_0 to the power line (Method B) as shown in Figure 2.14. Under

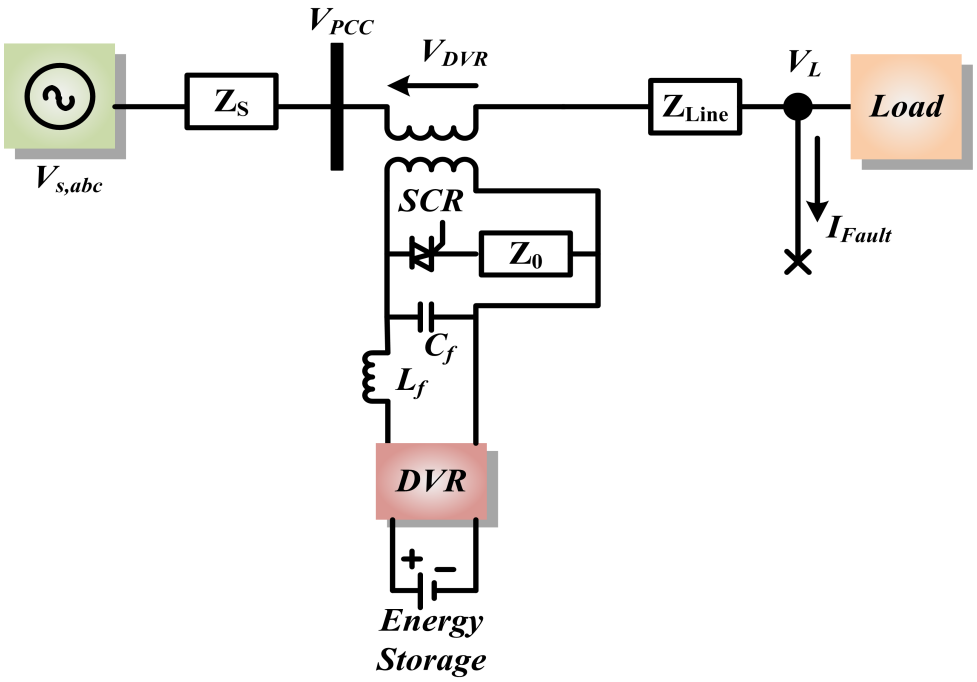


Figure 2.14: Adding additional reactor method (Method B)

this condition, (2.6) is attained when downstream fault occurs

$$I_{limited} = \frac{V_s}{Z_s + Z_{tr} + Z_0} \tag{2.6}$$

This measure may increase the voltage drop to a large extent when the DVR is in bypass mode. One way to solve this problem is that the additional voltage drop can be actively compensated by the DVR. Thereby additional power loss will be produced in the power converter of the DVR and the special injection transformer or the added reactor, and this additional power loss will dissipate all day long because in most cases DVR operate in bypass mode.

A possible method to decrease the power loss during normal condition (no-fault) is to shift the added reactor Z_0 to the solid switch bypass branch (Method B), as shown in Figure 2.14. At normal mode, DVR is bypassed by the power converter based system denoted as PCS, and when downstream fault occurs, the SCR is triggered and the PCS is shut down simultaneously to force the fault current shift from PCS to SCR branch instantaneously (Li et al., 2002). It is clear that Z_0 is not at work in most cases, so the additional power loss in normal mode is minimized. For this

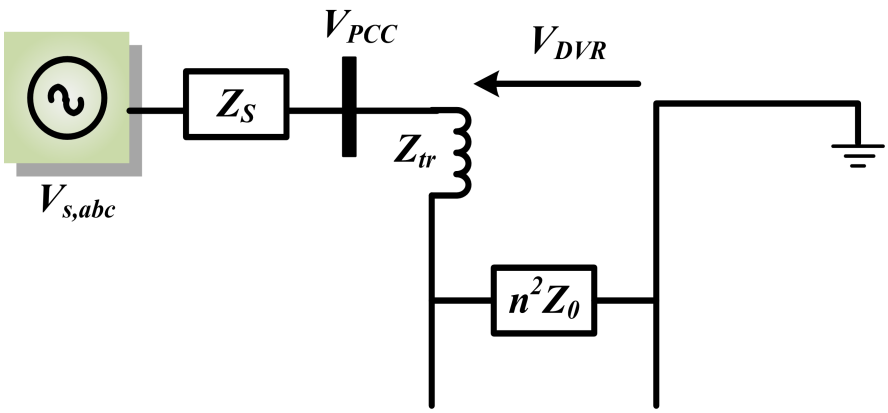


Figure 2.15: Equivalent circuit diagram during downstream fault occurs

method, the fault current can be expressed as equation (2.7), where n denotes the turns ratio of the injection transformer.

$$I_{limited} = \frac{V_s}{Z_s + Z_{tr} + n^2 Z_0} \tag{2.7}$$

When fault occurs, the equivalent circuit diagram is shown in Figure 2.15, where the filter elements L_f and C_f is omitted for the large impedance compared with Z_0 From Figure 2.15 the voltage rating of the power converter is given in (2.8).

$$V_{PCS} = \frac{n^2 Z_0}{Z_s + Z_{tr} + n^2 Z_0} V_s \tag{2.8}$$

Define the limiting rate α, the fault current limiting function as $(I_{fault} - I_{limited})/I_{fault}$ then 2.10 can be expressed as:

$$V_{PCS} = \alpha V_s \tag{2.9}$$

where the fact that Z_{tr} is normally very smaller than $n^2 Z_0$ is considered.

The (2.9) describes the relationship of the voltage rating of the DVR and the fault limiting ability. It shows that larger voltage rating of DVR is required with greater limiting rate.

$$\Delta V_{PCS} = \begin{cases} 0, & \alpha \leq \beta \\ (\alpha - \beta) V_s, & \alpha > \beta \end{cases} \tag{2.10}$$

Suppose the maximum compensation ability of DVR is β, it is to say that the voltage

rating of power converter system is βV_s, so the increased voltage rating of the DVR is derived as which determines the additional cost to achieve the fault current limiting function.

Thus to overcome the aforementioned issues and to protect DVR as well as PCC voltages a virtual impedance based FCL is adopted to control the fault current magnitude of series converter (DVR). In this method DVR acts as series impedance to limit the fault current and protects the PCC voltages during the downstream faults.

2.5 Series converter operation as Interlinking Converter in Hybrid Microgrid

In this chapter upto this point the control stategies of operating series converter (DVR) in distribution system is discussed where DVR mitigates the voltage disturbances viz., voltage sags, swell and protect DVR from downstream faults. In this section the operation of series converter as interlinking converter in hybrid microgrid is presented. Firstly the typical structure of hybrid microgrid is presented then the role of IC as well as different types of IC's are discussed in the later part of the section.

The conventional electric grid has been planned and structured for centralized generation of electricity predominantly from fossil fuels. The current trend is towards distributed generation of electricity especially from renewable energy sources such as solar and wind energy. Generating and consuming electricity locally is more economical, reliable and efficient, especially for electrification of off-grid or remote communities. This approach has led to a concept of interfacing autonomous and smart electrical networks with bidirectional power flow capability popularly referred to as microgrids (Lasseter, 2002), (Hatziargyriou et al., 2007). Integration of microgrids can improve grids performance and provide increased flexibility to its operation. A microgrid can be viewed as a small-scale power system comprising of generators, loads and storage. Typically, microgrid is considered as an partial entity from the utilitys point of view that can be operated in two modes : grid connected and islanded (Hatziargyriou et al., 2007).

Most of studies in the early stage of MG research had been done aimed at the development of control and operation methods in AC MG (Cheng et al., 2007). On the other hand, recent massive integration of renewable energy sources (RES) with rapid

emergence of consumer electronics and expansion of electric vehicle (EV) markets has led to development of DC microgrids. The DC distribution systems attracting significant interests from research community as DC grid performs better in terms of higher conversion efficiency, more reliable stability and scalability (Dragievi et al., 2016).

In the perspective of conventional power utility company, changing the existing AC grid into new DC grid does not seem to be a possible option owing to some physical and economic constraints even though there are clear advantages of DC grid over AC grid in modern power system environments. The DCMG can be viewed as an independent form of a small-size power system entity in the region of remote islands, independently operating factories and so on. The increasing installations of such DCMG's naturally leads to the integration of AC MG and DC MG for the sake of the maximization of benefits obtained from the utilization of both AC and DC grids.

In this context, the concept of hybrid AC/DC microgrid has been proposed (Liu et al., 2011). Simplified structure of hybrid AC/DC MG using an interlinking converter(ILC) is shown in Figure 2.16. It is the most promising type of MGs in the future power systems capable of most efficiently reducing the AC/DC conversion processes and facilitating the connection of various AC/DC sources and loads to power system.

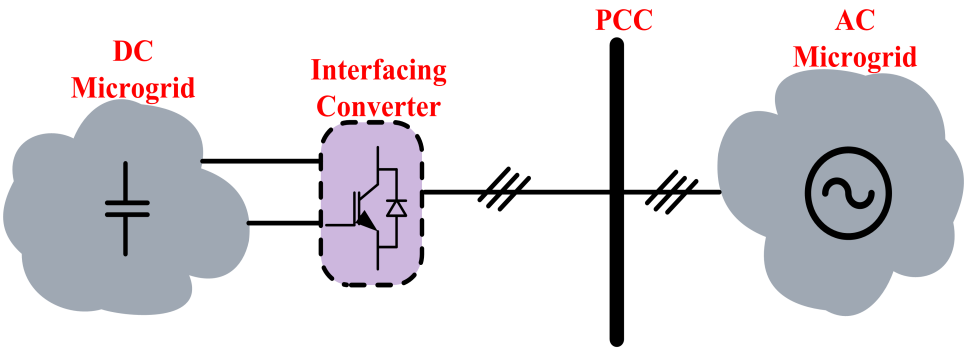


Figure 2.16: Simple Representation of Hybrid AC/DC System

2.6 Interlinking Converter

The IC can be used as a rectifier or an inverter, based on the direction of flow of power needed at each instant. The IC generally controls the DC bus voltage when the HMG is connected to the grid. In an islanded mode of operation, it may facilitate a slack bus either to the AC or DC subgrid (Hamad et al., 2016). Various converter topologies and configurations may be used as IC to allow power exchange among multiple dc/ac subgrids and the main grid.

The choice of IC topology relies basically on the control objectives required to be accomplished by it. There is a rising demand for incorporating added features other than the principal function of power management using a single IC instead of employing multiple ICs or additional active / passive components. Supplementary control objectives which contains, but not restricted to, storage coordination, stable improvement, managing power and voltage fluctuations among phases, grid current control, harmonics reduction, islanding diagnosis, synchronization, etc. This demand for multi-functional ICs has led to an exploration of different probable IC topologies. IC topologies can be categorized into three types depending on the number of converter stages and their locations viz., single stage, two stage and advanced ICs.

2.6.1 Single stage IC's

The most appropriate single stage IC for conventional HMG topology is a pulse width modulated (PWM) bidirectional VSC as shown in Figure 2.17 VSC can be controlled in voltage controlled mode (VCM) to regulate the ac or dc bus voltage or it can operate in current controlled mode (CCM) to regulate the power flow. VSC as an IC controlled in CCM is most common since it allows use of P-f and Q-V droop control in respective subgrids. Furthermore, multiple VSCs can be paralleled for exchanging higher amount of power (Chung, 2000), (Sun et al., 2017).

Single stage converters other than VSC have also been utilized as an IC owing to their distinct merits. For instance, a bidirectional quasi-Z-source inverter which has characteristics such as maximum constant boost and reduced switch stress is proposed and modeled as an IC in (Rodriguez et al., 2007). In the same way, a bidirectional switched boost converter which has merits viz., better stability and less number of reactive componentsis proposed as an IC in (Sahoo and Kumar, 2014). On a similar note, a modular multilevel converter with individual batteries integrated into each of

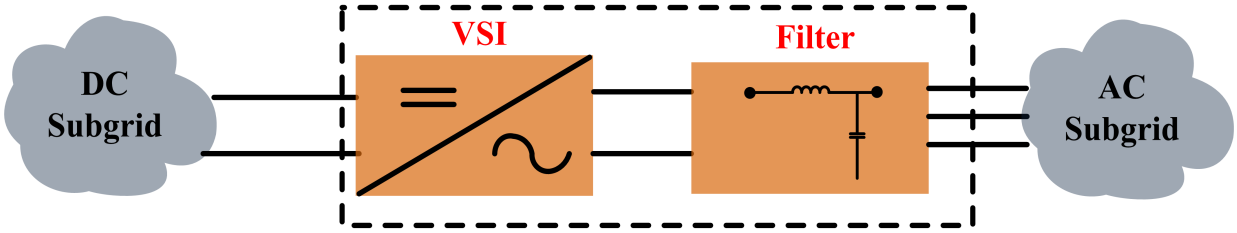


Figure 2.17: VSC as an IC

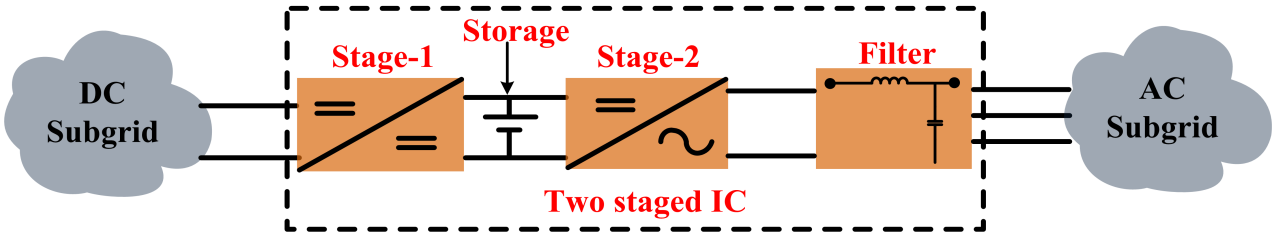


Figure 2.18: Two stage IC with battery at dc Link

its modules is employed as an IC thus reducing energy exchange between the subgrids and enhancing the overall efficiency (Zhang et al., 2015).

2.6.2 Two Stage IC's

Two stage ICs reported in literature either have cascade or parallel combination of different type of converters. These type of ICs provide additional power ports as well as allow more degree of freedom in control. A typical two-stage IC for storage integration (Loh et al., 2013a) is as shown in Figure 2.18. It consists of a storage connected at the common dc port of the boost converter and inverter. A similar configuration is implemented in (Yazdani et al., 2008) and (Yazdani et al., 2009) for integrating a bus of storages. On a similar note, a back to back (BtB) converter having two VSC stages can provide an additional port to interface the dc subgrid at its dc link (Majumder, 2014). BtB converter can also be used to interface ac microgrids having different frequencies (Che et al., 2015), (Loh et al., 2013b). Furthermore, a combination of diode rectifier in parallel with a three-level neutral point clamped (NPC) converter acting as an active front end has been proposed as an IC in (Hou and Huang, 2014).

2.6.3 Advanced IC's

Most of the ICs discussed so far have been employed mainly for power management. Advanced ICs refer to use of either advanced control strategies or atypical IC configurations for achieving multiple control objectives. For instance, power flow control and simultaneous improvement in power quality have been demonstrated using a multifunctional VSC in (Tummuru et al., 2014). The scheme presented in (Majumder, 2014) decides an appropriate response to faults occurring either on dc or ac side in addition to controlling power flow and the dc bus voltage. In similar way, the control strategy of (Mohamed et al., 2012) has integrated fault limiting feature in its IC control.

(Abdelsalam et al., 2014) and (Radwan and Mohamed, 2012) have proposed the use of individual ICs for interfacing the dc subgrid with the ac subgrid and with the main grid as shown in Figure 2.19. This type of IC configuration tends to permit ac subgrid to operate at a different frequency than that of main grid. (Karabiber et al., 2013) have proposed a complex IC configuration which interfaces "all distributed generator (DG)" connected dc bus and the main grid to the "load" ac bus. This configuration permits continuous exchange of power from the grid and local DGs, thus ensuring reliable and controllable power for the loads.

Thus IC plays an important role for the stability of whole hybrid microgrid.The desired operating features of the hybrid microgrid can be achieved through this interlinking converter. Due to this feature there is an increasing demand for executing additional functions other than the primary function of power management using a single IC rather than employing multiple ICs or additional active/passive components. In view of this the current thesis focuses on the investigation of different possible modes of operation of interlinking converter in hybrid microgrid to achieve objectives viz., AC, DC voltage control, fault current limiting operation and power management between ac and dc subsystems. In this approach DC subgrid is integrated with main utility grid via single interlinking converter. The control strategy adopted not only ensures the multi-mode operation of proposed single IC but also allows flexible bi-directional operation. Furthermore, the control strategy allows the IC to provide stable DC bus voltage for dc subgrid during transients and exchange power between the ac and dc buses.

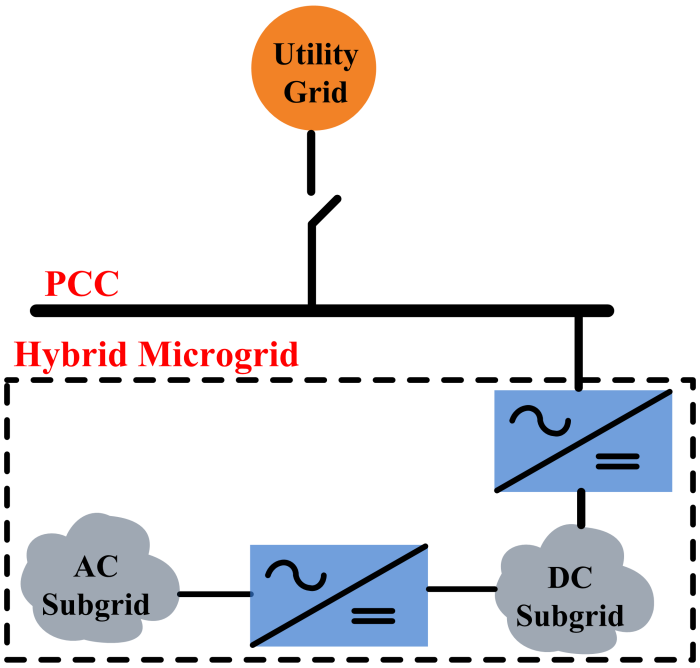


Figure 2.19: ICs interfacing dc subgrid with ac subgrid and with main grid

2.7 Conclusion

The multimode operation of series converter is discussed in this chapter. As mentioned earlier the multimode operation refers to operating the series converter in different modes when installed in distribution and hybrid microgrid environment. In view of this different control strategies developed in literature are discussed respectively. Some of the main conclusions are as follows

- Firstly in distribution system the different control stategies for operating series converter (DVR) to compensate voltage disturbances viz., sag, swell and harmonics is discussed. A multiloop control scheme is adopted due to its flexibility to design and to avoid the issues related to single loop control scheme.

- The problem of grid phase detection is discussed as this stage is crucial in DVR compensation mode which yeilds grid phase angle θ from the grid voltage signal V_{abc}. It is observed that a prefilter based PLL can solve the problems in obtaining the aforementioned parameters accurately during voltage disturbances. In this regard many prefilter based PLL are discussed and among them it is

identified that CDSC-PLL proves to be superior in terms of harmonic elimination ability, transient response, frequency adaptability. It also features small memory overhead and light computational burden.

- Further control strategies for operating series converter (DVR) as FCL are discussed to reduce the magnitude of fault current and to maintain the PCC voltage at prefault level. As per the literature study a virtual impedance based FCL control of DVR is proposed where the DVR acts as series impedance.

- Interlinking converter which links the AC and DC subgrids in the hybrid microgrid, plays an important role for the stability of whole hybrid microgrid. The desired operating features of the hybrid microgrid can be achieved through this interlinking converter. In view of this different types of IC's are discussed. In view of IC flexibility the present thesis work focuses on the investigation of different possible modes of operation of IC to achieve different objectives in hybrid microgrid environment.

Chapter 3

Concept of Dual Role CDSC - Prefilter and Extractor

Contents

3.1 Introduction

PLLs are commonly used to estimate the phase angle and magnitude of the grid voltage. During voltage unbalance and harmonics in the grid voltage the conventional PLL schemes has to comprimise between transient dynamics and steady-state accuracy. Among them CDSC based PLL-Prefilter proves to be superior in harmonic mitigation capability, frequency adaptability and do not involve any complexity for implementation. In this work the CDSC is utilised in two ways one as prefilter (source side) for PLL and secondly as an extractor for selective harmonic elimination (load side) thus accounts for dual role in compensation of upstream fault.

As a prefilter the CDSC operator process the input voltage signal and eliminates the harmonics present thereby delivering pure sinusoidal signal to the PLL system. Therefore the bandwidth of the PLL can be set to a high value to yield better system dynamics with low steady-state detection error, which arises due to harmonics in the input signal. On the other hand a fast and accurate selective harmonic detection scheme provides the vital information needed by many harmonic compensation systems. Thus a dual role CDSC strategy is used to achieve selective harmonic mitigation of load voltage. Therefore the CDSC operator plays key role in the preoposed system and should be designed well in proper manner. This chapter deals with concept of dual role CDSC in the proposed system.

Firstly in this chapter representation of harmonics in different schemes are presented. Then chapter preceds with basic operating principle of PLL, followed by conventional SRF-PLL. After introduction about SRF-PLL the discussion prolongs to the performance of SRF-PLL under distorted grid conditions followed by brief introduction to PLL-Prefilters. Section 4.6 and 4.7 elaborates about DSC operation in dq-frame followed by $\alpha\beta$-frame.

3.2 Representation of grid voltage quantities and harmonic voltage signals

The grid voltage in three phase power systems is represented either by rotating space vector (or)time domain signals. The Table 3.1 describes the mutual relation between aforementioned quantities. The alphabet 'a' mentioned in the table is unit length rotating factor defined as $a = e^{j120^0} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ thereby $a^2 = e^{j240^0} = e^{-j120^0} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$. The grid voltage space vector ($\overrightarrow{v}$) can be transformed either into synchronous

Table 3.1: Mathematical representation of grid voltage quantities.

Space Vectors	Stationary Reference Frames		Synchronous Reference Frame
	abc-frame	$\alpha\beta$-frame	dq-frame
	$\overrightarrow{v}_{abc} = \frac{2}{3}\left(v_a + av_b + a^2 v_c\right)$	$\overrightarrow{v}_{\alpha\beta} = v_\alpha + jv_\beta$	$\overrightarrow{v}_{dq} = v_d + jv_q$
Time domain signals	$v_{abc} = [v_a, v_b, v_c]^T = \begin{bmatrix} Vcos\theta \\ Vcos\left(\theta - 120^0\right) \\ Vcos\left(\theta + 120^0\right) \end{bmatrix}$	$v_{\alpha\beta} = \left[v_\alpha, v_\beta\right]^T = \begin{bmatrix} Vcos\theta \\ Vsin\theta \end{bmatrix}$	$v_{\alpha\beta} = \left[v_\alpha, v_\beta\right]^T = \begin{bmatrix} Vcos\theta \\ Vsin\theta \end{bmatrix}$

reference frame (dq-frame, $\overrightarrow{v}_{dq}$) or *stationary reference frame* ($\alpha\beta$-frame, $\overrightarrow{v}_{\alpha\beta}$). It is to be noted that the magnitude of the grid voltage, V remains the same in all the frames and is equal to peak value of grid phase voltage. Let θ be the phase angle of $\overrightarrow{v}$ in $\alpha\beta$ and abc frames thereby the pahse angle in the dq-frame becomes $\delta = \theta - \upsilon$ where υ is the angle difference between d-axis and α axis. Generally the angle υ is chosen to be same as θ, which represents that d-axis is alligned along $\overrightarrow{v}_a$) (same as a-axis), therefore δ=0, v_q=0, v_d=V. This method is known as Voltage-Oriented Control (VOC) method for power electronic converter.

During the ideal grid voltage conditions, the vector $\overrightarrow{v}_{\alpha\beta}$ is rotating with constant frequency of $\omega = {}^{d\theta}/_{dt}$ and hence the signals v_α, v_β are sinusoidal signals. However, in the reality grid voltage is usually distorted and unbalanced therefore the signals v_α & v_β are comprised of a series of harmonics signals represented as

$$\begin{aligned} \overrightarrow{v}_{\alpha\beta} &= v_\alpha + jv_\beta \\ &= \sum_{h=-H}^{h=+H} v_\alpha^h + j \cdot \sum_{h=-H}^{h=+H} v_\beta^h \\ &= \sum_{h=-H}^{h=+H} V^h cos\theta^h + j \cdot \sum_{h=-H}^{h=+H} V^h sin\theta^h \\ &= \sum_{h=-H}^{h=+H} V^h \left[cos\theta^h + jsin\theta^h\right] \\ &= \sum_{h=-H}^{h=+H} V^h e^{j\theta^h} = \sum_{h=-H}^{h=+H} \overrightarrow{v}_{\alpha\beta}^h \end{aligned} \tag{3.1}$$

In the above (3.1) ω is the fundamental angular frequency which is equal to $2\pi f$ and the instantaneous angle of each harmonic space vector $\theta^h = h\omega t + \varphi^h$ where φ^h is the initial phse angle. The h represents the harmonics order (h=0, $\pm$1, $\pm$2...H). Any positive value of h represents a positive sequence harmonic component, negative value

of h represents negative sequence harmonic component. Thus the harmonic distortion of the time domain signals are transformed to space vector $\overrightarrow{v}_{\alpha\beta}$ which is no longer a single vector, but equals to vectorial sum of a series of harmonic vectors which are rotating at harmonic frequencies $h\omega$ respectively.

Similarly, in dq-frame,

$$\begin{aligned}
\overrightarrow{v}_{dq} &= v_d + jv_q \\
&= \sum_{h=-H}^{h=+H} v_d^h + j \cdot \sum_{h=-H}^{h=+H} v_q^h \\
&= \sum_{h=-H}^{h=+H} V^h cos\delta^h + j \cdot \sum_{h=-H}^{h=+H} V^h sin\delta^h \\
&= \sum_{h=-H}^{h=+H} V^h \left[cos\delta^h + jsin\delta^h\right] \\
&= \sum_{h=-H}^{h=+H} V^h e^{j\delta^h} = \sum_{h=-H}^{h=+H} \overrightarrow{v}_{dq}^h
\end{aligned} \tag{3.2}$$

where the instantaneous phase angle δ^h=hωt+φ^h and h is the harmonic order in dq-frame. It is to be noted that the dq-frame vector $\overrightarrow{v}_{dq}^h$ arises from the $\alpha\beta$-frame vector $\overrightarrow{v}_{\alpha\beta}^{h+1}$ as the dq-frame itself is rotating counter-clockwise at ω.

3.3 Phase Locked Loop

PLL is commonly used to estimate the phase angle and magnitude of the grid voltage. A PLL consists of a Phase Detector (PD), Loop Filter (LF) and a voltage controlled oscillator (VCO). For estimating the phase angle and magnitude of a single-phase grid voltage, a multiplier is used as a PD (multiplier PD), a PI controller acts as a LF to eliminate harmonics and to track changes in the grid voltage frequency and phase angle. An integrator acts as a VCO to generate the estimated phase angle of the grid voltage as shown in Figure 3.1. If the input signal applied to this system is given by

$$v = V_m sin(\omega t + \varphi) \tag{3.3}$$

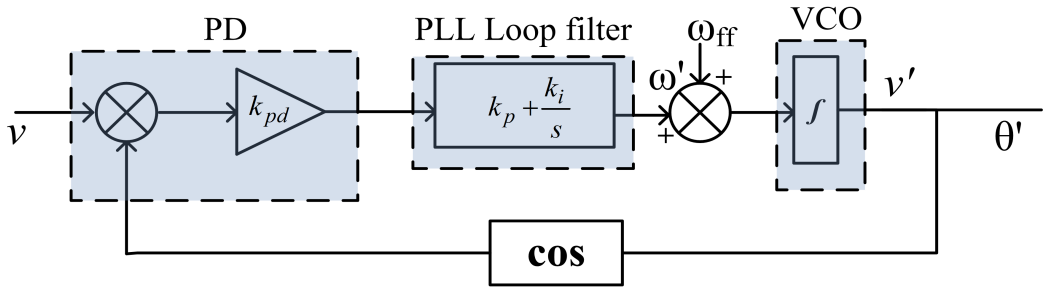


Figure 3.1: Phase Locked Loop

and the signal generated by the VCO is given by

$$v^{'} = cos(\omega^{'}t + \varphi^{'}) \tag{3.4}$$

the phase error signal from the multiplier PD output can be written as

$$\epsilon = v_m k_{pd} cos(\omega^{'}t + \varphi^{'}) sin(\omega t + \varphi) \tag{3.5}$$

$$\epsilon = \frac{v_m k_{pd}}{2}\left[sin\left((\omega - \omega^{'}\right)t + (\varphi - \varphi^{'})) + sin\left((\omega + \omega^{'}\right)t + (\varphi + \varphi^{'}))\right] \tag{3.6}$$

where k_{pd} is the gain offered by the PD. (3.6) consists of one lower frequency term $(\omega - \omega^{'})$ and a higher frequency term $(\omega + \omega^{'})$. A PI controller with gains k_p, k_i acts as a loop filter to eliminate higher frequency terms and thus error can be approximated as

$$\epsilon = \frac{v_m k_{pd}}{2} sin(\theta - \theta^{'}) \tag{3.7}$$

where $(\theta - \theta^{'})$ is the essential phase angle and $\theta = \omega t + \varphi$ is the grid phase angle. By tuning k_p and k_i the transient and steady state response of the PLL can be controlled, where large k_p leads to a quick response and large value of k_i improves tracking accuracy. Using optimizing techniques, these parameters can be tuned to yield optimum performance.

For smaller values of $(\theta - \theta^{'})$ i.e., when the phase angle and frequency of the input voltage signal and estimated signal are nearly equal the equation can be linearized to get small signal model

$$\epsilon = v_m k_{vco} \tag{3.8}$$

where $k_{vco} = \frac{k_{pd}}{2}(\theta - \theta^{'})$

This gives estimated frequency of the grid voltage signal, which is in turn used by

VCO to fetch the phase angle information.

$$\omega^{'} = \omega_{ff} + v_m k_{c0} \tag{3.9}$$

$$\omega^{'} = \omega_{ff} + \Delta\omega \tag{3.10}$$

where ω_{ff} is the center frequency of VCO and $\theta^{'} = \int \omega^{'} dt$

Any change in the phase angle and frequency of the voltage, generates an error which is tracked by the PI controller (Loop Filter) so that the estimated phase angle $\theta^{'}$ maintains the phase lock with the grid voltage, hence it is called a phase locked loop. In multiplier based phase detector PLLs, the loop filter has to be tuned to eliminate the higher frequency component which has a frequency of 100 Hz, which leads to a slow dynamic response of the PLL. Even though this type of PLL can track changes in frequency and phase angle, the loop filter has to be tuned to a lower frequency cut off to eliminate the double frequency component and this leads to a slow dynamic response of the PLL. This concept of phase locked loop is extended for three phase systems by replacing multiplier PD with a synchronous reference frame based PD and the resulting PLL is called a Synchronous Reference Frame-PLL (SRF-PLL).

3.4 Synchronous Reference Frame

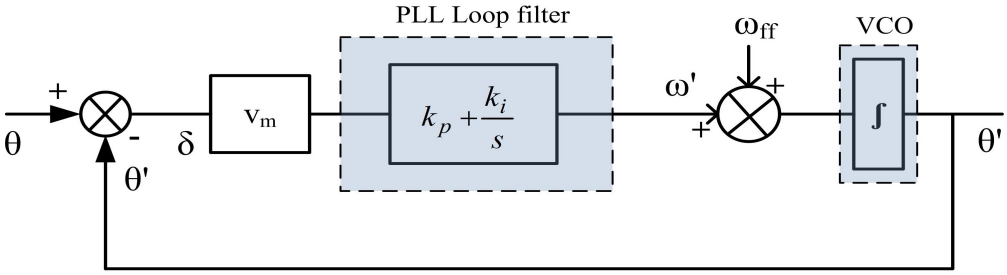


Figure 3.2: Conventional SRF-PLL

For three phase systems SRF-PLL, shown in Figure 3.2, is usually employed for extracting the phase angle information and magnitude of the grid voltage. The issues with a multiplier PD of a PLL are overcome by replacing it with a SRF-PD. SRF-PD is better than multiplier PD as the second harmonic component is eliminated from the error estimated in this type of PD for balanced input voltages.

The principle behind SRF-PLL is it transform the three phase grid voltages into synchronous frame of reference which results in quadrature voltages v_d, v_q as shown in Figure 3.3 rotating with angular speed ω. The frequency and phase angle of the synchronous frame are locked to that of grid voltages by taking it as a feedback and continuously compare it with grid phase angle to derive the error signal. This error signal is tracked by the PI controller to maintain phase lock with the grid voltages. The phase comparison to generate error is achieved by using krauses generalized frame transformation (kra, 2013) given in (3.11) (Clarke, 1943) and (3.12).

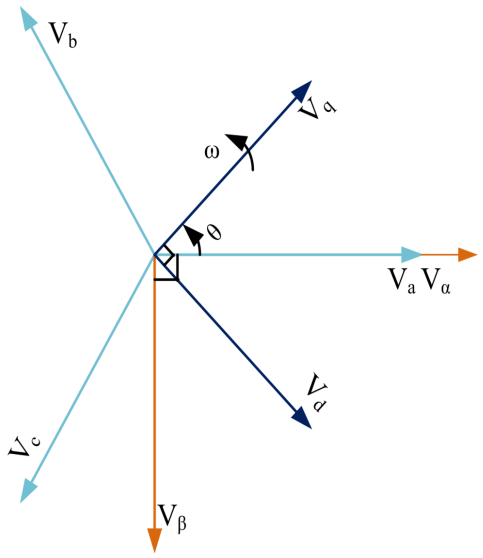


Figure 3.3: Graphical representation of frame transformation

The grid voltage can be transformed to stationary and synchronous reference frame of reference by using (3.11) and (3.12) respectively.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.11}$$

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta' & cos\left(\theta' - 2\pi/3\right) & cos\left(\theta' + 2\pi/3\right) \\ sin\theta' & sin\left(\theta' - 2\pi/3\right) & sin\left(\theta' + 2\pi/3\right) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.12}$$

$v_{\alpha\beta}$, v_{dq} represent grid voltages in stationary and synchronous reference frames respectively. $\omega^{'} = d\theta^{'}/dt$ is the frequency of synchronous reference frame in rad/s. When

balanced grid voltages are transformed to SRF, quadrature dq-voltages obtained are given in (3.16)

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \begin{bmatrix} v_m sin\theta \\ v_m sin\left(\theta - {}^{2\pi}/_{3}\right) \\ v_m sin\left(\theta + {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{3.13}$$

$$[v_{\alpha\beta}] = [T_{\alpha\beta}] \quad [v_{abc}] \tag{3.14}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \begin{bmatrix} v_a \\ {}^{-1}/_{\sqrt{3}}\left(v_b - v_c\right) \\ 0 \end{bmatrix} = \begin{bmatrix} v_m sin\theta \\ v_m cos\theta \\ 0 \end{bmatrix} \tag{3.15}$$

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} cos\theta' & -sin\theta' \\ sin\theta' & cos\theta' \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v_m sin(\theta - \theta') \\ v_m cos(\theta - \theta') \end{bmatrix} \tag{3.16}$$

From (3.15) it can be observed that the three phase voltages are now converted to balanced two phase voltages in stationary frame which are in quadrature as shown in Figure 3.3.

From (3.16) it can be observed that when the PLL maintains a phase lock or when the phase error $\delta = \theta - \theta'$ is small, the equations can be approximated to a linearized small signal model.

$$\begin{bmatrix} v_q \\ v_d \end{bmatrix} = \begin{bmatrix} cos\theta' & -sin\theta' \\ sin\theta' & cos\theta' \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v_m \delta \\ v_m \end{bmatrix} \tag{3.17}$$

From (3.17) conclusions can be drawn that the synchronous reference frame acts as a PD and computes the error between the estimated and actual grid phase angles. v_q is normalized and it is considered as error which it is utilized to estimate the grid phase angle by SRF-PLL as shown in Figure 3.2.

3.5 SRF PLL under distorted grid conditions

The three phase voltages of the grid can experience voltage sags, swells and can be distorted due to the presence of harmonics.Under these distorted grid voltage conditions the output dq-voltages of SRF-PLL contains oscillations (Chung, 2000).

To overcome these issues, grid voltages are passed through filters to eliminate these disturbances from the measured grid voltages before locking it to a SRF-PLL. Before discussing pre-filters or issues with SRF-PLL, mathematical model of harmonics in dq-frame is obtained. Then the performance of a conventional SRF-PLL under distorted grid voltages is analyzed.

Each harmonic including the fundamental can be resolved into positive, negative and zero sequence components. When the voltages are balanced only positive sequence components are present in the grid voltage, but if unbalance exist in these harmonic voltages negative and zero sequence components also appear. Hence, these grid voltages can be represented as sum of fundamental and harmonic components.

$$v_{abc} = v_{abc}^{+1} + v_{abc}^{h} \tag{3.18}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = v^{+1} \begin{bmatrix} v_m sin\theta \\ v_m sin\left(\theta - {}^{2\pi}/_{3}\right) \\ v_m sin\left(\theta + {}^{2\pi}/_{3}\right) \end{bmatrix} + v^{h} \begin{bmatrix} v_m sinh\theta \\ v_m sin\left(h\theta - {}^{2\pi}/_{3}\right) \\ v_m sin\left(h\theta + {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{3.19}$$

where v^{+1} is magnitude of fundamental component of source voltage, h is the order of the harmonic, v^h is magnitude of h^{th} harmonic component of source voltage . h>0 (h=+1, +2.) represents positive sequence components, h<0 (h=-1, -2, -3.) represents negative sequence components. For example h= +1, h= -1,h=0 represents positive, negative and zero sequence components of fundamental grid voltages. When these voltages are converted to positively rotating synchronous frame using (3.12) dq-voltages obtained are given in (3.20)

$$v_{dq} = v^{+1} \begin{pmatrix} 1 \\ 0 \end{pmatrix} + v^{h} \begin{pmatrix} cos\left((h-1)\omega t\right) \\ sin\left((h-1)\omega t\right) \end{pmatrix} \tag{3.20}$$

Generally, in distribution systems triplen harmonics, being zero sequence harmonics, are not present in line voltages as the distribution systems are usually 3 phase and 3 wire systems. Loads such as electric arc furnace, half bridge rectifiers would give rise to even order harmonics as they draw half wave asymmetric non-linear currents from the grid. However, the percentage of even order harmonics in grid are small. Hence, only odd harmonics of order h= -5, +7, -11, +13 are commonly found in the

grid voltages. These harmonics are called asymmetric odd order harmonics (Wang and Wei Li, 2011).

With increased use of single phase non-linear loads such as full bridge converters which are used for power supplies, harmonics in grid voltage are no longer balanced. As a result, the grid voltage triplen harmonics contain positive and negative sequence components along with zero sequence components. The other reason for third harmonic currents are usage of uncontrolled rectifiers which draws a trapezoidal current from the grid when connected to an RL load. Hence, harmonics h= +5, -7 and so on can also be expected in the grid voltage along with h= -5, +7... and triplen harmonics.These harmonics are termed as asymmetric harmonics.Thus, all odd order harmonics n = +3, +5, +7, +9 would appear in the grid voltage. When grid voltages are balanced and doesnt contain harmonics i.e, $v^h = 0$, only positive sequence voltages are present and hence the dq-voltages obtained in (3.20) are constants.

$$v_{dq} = v^{+1} \begin{pmatrix} 1 \\ 0 \end{pmatrix} \tag{3.21}$$

when the grid voltage is unbalanced, negative sequence voltages are present. These negative sequence components when converted to synchronous frame the dq-voltages appear as double frequency components along with the fundamental positive sequence voltage. This can be obtained mathematically by substituting h= -1 in (3.20).

$$v_{dq} = v^{+1} \begin{pmatrix} 1 \\ 0 \end{pmatrix} + v^{-1} \begin{pmatrix} cos\,(-2\omega t) \\ sin\,(-2\omega t) \end{pmatrix} \tag{3.22}$$

Similarly it can be observed any harmonics h= +k present in the grid voltage would appear as p=+k-1 harmonics in dq-frame with time periods T/p where (k=+1, +2..) The PI loop filter of SRF-PLL would no longer be able to track the phase error properly and hence the detection of output grid phase angle would be inaccurate. (Lee et al., 1999)

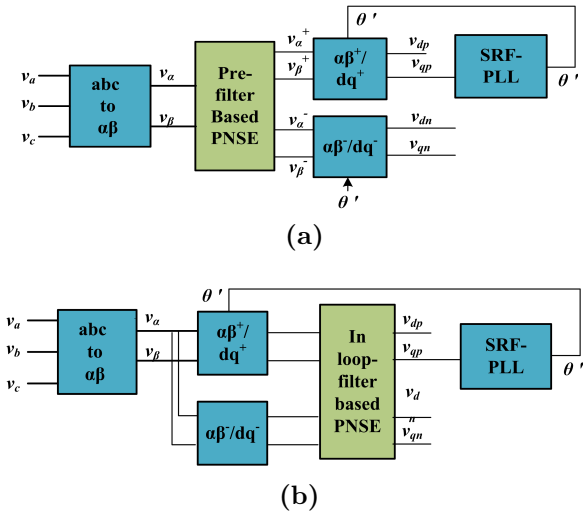


Figure 3.4: (a) $\alpha\beta$-frame PNSE (prefilter) (b) dq-frame (in-loop filter) PNSE

3.6 PLL-Prefilter

To overcome these problems of SRF-PLL filters can be placed either in loop (dq-frame) or in stationary reference frame($\alpha\beta$-frame). Figure (3.4a),(3.4b) shows Positive and Negative Sequence Extractors (PNSE) in dq-frame and $\alpha\beta$-frame respectively. Moving Average Filter (MAF), Delayed Signal Cancellation (DSC) are examples of in-loop filters presented in the literature.

Pre-filters are usually preferred as they dont create delay in the control loop of PLL (Wang and Wei Li, 2011). The symmetrical components of the grid voltage can be extracted by using Lyons Instantaneous Symmetrical Component (ISC) transformation.

Three phase sinusoidal voltages can be separated into positive (v^+_{abc}), negative sequence (v^-_{abc}), and zero sequence voltages(v^0_{abc}).

$$\left[v^+_{abc}\right] = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = [T_+]\, v_{abc} \tag{3.23}$$

$$\left[v^-_{abc}\right] = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = [T_-]\, v_{abc} \tag{3.24}$$

$$\left[v^0_{abc}\right] = \frac{1}{3}\begin{bmatrix}1 & 1 & 1\\ 1 & 1 & 1\\ 1 & 1 & 1\end{bmatrix}\begin{bmatrix}v_a\\ v_b\\ v_c\end{bmatrix} = [T_0]\, v_{abc} \tag{3.25}$$

These equations are obtained in stationary frame by transforming the positive and negative sequence matrix from abc frame to stationary frame.

$$\left[v^+_{\alpha\beta}\right] = [T_{\alpha\beta}]\left[v^+_{abc}\right] = [T_{\alpha\beta}]\,[T_+]\,[v_{abc}] \tag{3.26}$$

$$\left[v^-_{\alpha\beta}\right] = [T_{\alpha\beta}]\left[v^-_{abc}\right] = [T_{\alpha\beta}]\,[T_-]\,[v_{abc}] \tag{3.27}$$

$$\left[v^+_{\alpha\beta}\right] = [T_{\alpha\beta}]\,[T_+]\,[T_{\alpha\beta}]^{-1}\,[v_{abc}] \tag{3.28}$$

$$\left[v^-_{\alpha\beta}\right] = [T_{\alpha\beta}]\,[T_-]\,[T_{\alpha\beta}]^{-1}\,[v_{abc}] \tag{3.29}$$

$$\begin{bmatrix}v^+_\alpha\\ v^+_\beta\end{bmatrix} = \frac{1}{2}\begin{bmatrix}1 & -q\\ q & 1\end{bmatrix}\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix} \tag{3.30}$$

$$\begin{bmatrix}v^-_\alpha\\ v^-_\beta\end{bmatrix} = \frac{1}{2}\begin{bmatrix}1 & q\\ -q & 1\end{bmatrix}\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix} \tag{3.31}$$

From (3.30) and (3.31) ISC can be obtained in stationary frame where q is a 90^0 phase lag factor.

This q operator can be implemented in two ways. One way is by using Quadratic Signal Generators(QSG) like Second Order General Integrators (SOGI), Hilberts transformation etc., or by using techniques such as Delayed Signal Cancellation (DSC).

3.6.1 Delayed Signal Cancellation(DSC)

The harmonics present in the grid voltage retain their periodic nature even when they are transformed to synchronous reference frame. DSC technique exploits this property so that it is possible to eliminate harmonic signal by summing it with half cycle delayed version. This technique is primarily implemented in dq-frame and it can suppress negative sequence harmonics and symmetric odd order harmonics.

The mathematical model of DSC filter in dq-frame is (Neves et al., 2010)

$$dqDSC_n = \frac{1}{2}\left[v_{dq}(t) + v_{dq}(t - {}^T/_n)\right] \tag{3.32}$$

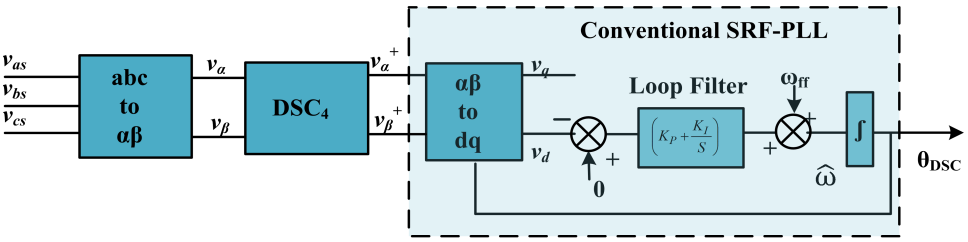


Figure 3.5: DSC-PLL

Where T is grid fundamental period, n is the "delay factor" and T/n is the delay time". If T is known the parameter n can be calculated such that the value of T/n equals to one-half cycle of harmonic which is to be eliminated. The subsequent formula is derived as follows: After applying the DSC operator to the d-axis harmonic component $v_d^h(t)$ yields the following equation

$$\begin{aligned} dqDSC_n\left[v_d^h(t)\right] &= \frac{1}{2}\left[v_d^h(t) + v_d^h(t - {}^T/_n)\right] \\ &= \frac{1}{2}\left[V^h cos\left(h\omega t + \varphi^h\right) + V^h cos\left(h\omega\left(t - {}^T/_n\right) + \varphi^h\right)\right] \\ &= \frac{V^h}{2}\left[cos\left(h\omega t + \varphi^h\right) + cos\left(h\omega t - h\cdot {}^{2\pi}/_n + \varphi^h\right)\right] \\ &= V^h cos\left(h\omega t + \varphi^h - {}^{h\pi}/_n\right)\cdot cos\left({}^{h\pi}/_n\right) \end{aligned} \tag{3.33}$$

Similarly, application to q-axis harmonic component $v_q^h(t)$ yields the following equation

$$\begin{aligned} dqDSC_n\left[v_q^h(t)\right] &= \frac{1}{2}\left[v_q^h(t) + v_q^h(t - {}^T/_n)\right] \\ &= \frac{1}{2}\left[V^h sin\left(h\omega t + \varphi^h\right) + V^h sin\left(h\omega\left(t - {}^T/_n\right) + \varphi^h\right)\right] \\ &= \frac{V^h}{2}\left[sin\left(h\omega t + \varphi^h\right) + sin\left(h\omega t - h\cdot {}^{2\pi}/_n + \varphi^h\right)\right] \\ &= V^h sin\left(h\omega t + \varphi^h - {}^{h\pi}/_n\right)\cdot cos\left({}^{h\pi}/_n\right) \end{aligned} \tag{3.34}$$

$$
\begin{aligned}
dqDSC_n\left[\overrightarrow{v}^h_{dq}(t)\right] &= dqDSC_n\left[v^h_d(t)+jv^h_q(t)\right] \\
&= dqDSC_n\left[v^h_d(t)\right]+jdqDSC_n\left[v^h_q(t)\right] \\
&= V^h\left[cos\left(h\omega t+\varphi^h-{}^{h\pi}/_n\right)+jsin\left(h\omega t+\varphi^h-{}^{h\pi}/_n\right)\right]\cdot cos\left({}^{h\pi}/_n\right) \\
&= V^h e^{j\left(h\omega t+\varphi^h-{}^{h\pi}/_n\right)}\cdot cos\left({}^{h\pi}/_n\right) \\
&= V^h e^{j\left(h\omega t+\varphi^h\right)}\cdot cos\left({}^{h\pi}/_n\right)e^{-j{}^{h\pi}/_n} \\
&= \overrightarrow{v}^h_{dq}(t).\overrightarrow{G}^h_n
\end{aligned}
\tag{3.35}
$$

Now by combining both d & q axis component DSC space vectors yields a combine space vector $\overrightarrow{v}^h_{dq}(t)$ and given in (3.35). where $\overrightarrow{G}^h_n$ is termed as "Harmonic gain" of $dqDSC_n$ operator which is complex number whoose magnitude is given as

$$
G^h_n=\left|\overrightarrow{G}^h_n\right|=cos\left({}^{h\pi}/_n\right) \tag{3.36}
$$

with a phase angle of

$$
\phi^h_n=\angle\overrightarrow{G}^h_n=-{}^{h\pi}/_n \tag{3.37}
$$

From the (3.36) & (3.37) it can be inferred that the time domain DSC operation scales the magnitude of the signal $\overrightarrow{v}^h_{dq}(t)$ to G^h_n and shifts the signal by an angle of ϕ^h_n along the ωt axis. In other words it delays the signal ϕ^h_n/ω along ωt axis.

From (3.36) it can be seen that the value of G^h_n ranges from 0 to 1. While zero gain corresponds to the situation that the DSC completely eliminates the harmonic, unity gain corresponds to that sitution where harmonic signals are not attenuated. For all the other values between 0 and 1, the harmonic is attenuated yet not eliminated. Therefore, in order to determine DSC parameters for the elimination of a certain harmonic, let G^h_n=0, and it can be solved from (3.36) that

$$
n=\left|\frac{h}{2k\pm{}^1/_2}\right|,\quad k=1,2,3.....\quad h=0,\pm1,\pm2,.....\pm H \tag{3.38}
$$

where k is an integer, h is the dq-frame harmonic order. It means that a DSC operator with the obtained delay factor n can eliminate the corresponding harmonic signal v^h_{dq}

With a single DSC operator all harmonics (h) satisfying the (3.38) are eliminated while the other components are either attenuated or remains unchanged. Therefore single DSC operator is not enough to eliminate all harmonics in the signal v^h_{dq}(t).

Moreover, this technique is not capable of blocking asymmetric odd harmonics. To overcome this issue the concept of DSC can be extended to filter out other harmonics by cascading multiple DSC operators (in an arbitrary sequence) to form a cascaded delayed signal cancellation (CDSC) operator (Wang and Li, 2011), which can then be applied to the input signal and eliminate all undesired harmonics step by step.

Similar to the DSC operator the harmonic elimination capability of CDSCoperator depends on its gain. In this regard the generalized gain of CDSC operator can be analysed. Consider two DSC operators $dqDSC_n[\cdot]$ and $dqDSC_m[\cdot]$ which are used to construct a CDSC operator $dqDSC_{n,m}[\cdot] = dqDSC_m[dqDSC_n[\cdot]]$

$$\begin{aligned} dqDSC_{n,m}\left[\overrightarrow{v}^h_{dq}\right] &= dqDSC_m\left[dqDSC_n\left[\overrightarrow{v}^h_{dq}\right]\right] \\ &= dqDSC_m\left[\overrightarrow{v}^h_{dq}\cdot\overrightarrow{G}^h_n\right] \\ dqDSC_m\left[\overrightarrow{v}^h_{dq}\right]\cdot\overrightarrow{G}^h_n &= \overrightarrow{v}^h_{dq}\cdot\overrightarrow{G}^h_m\cdot\overrightarrow{G}^h_n = \overrightarrow{v}^h_{dq}\cdot\overrightarrow{G}^h_{n,m} \end{aligned} \tag{3.39}$$

From the (3.39) it can be concluded that the cascaded gain ($\overrightarrow{G}^h_{n,m} = \overrightarrow{G}^h_m\cdot\overrightarrow{G}^h_n$) is the product of individual gains of DSC operators (in the above equation it is product of indivudual gains of two DSC operators) which are involved in forming CDSC operator.

The selection of CDSC operator i.e., combination of DSC operators depends upon the predicted harmonic input. If the grid voltage is unbalanced and not distorted then the only target is to eliminate negative sequence harmonics which is served by using $dqDSC_4$. On the other hand if grid voltage is distorted in symmetrical and asymmetrical pattern then $dqDSC_{4,8,16,32}$ should be used.

3.6.2 $\alpha\beta$ frame DSC operation

Consider a ideal condition where the input signal to the PLL is pure sinusoidal, the bandwidth of PLL loop can be tuned to a very high value for good system dynamics. It is to be noted that DSC/CDSC operators in the dq-frame introduce time delay into the control loop, and will complicate PLL tuning (Wang and Li, 2011). Especially, in the case of $dqDSC_4$ introduces ${}^T/_4 = 0.25T$ delay. Whereas $dqDSC_{2,4,8,16,32}$ introduces ${}^T/_2 + {}^T/_4 + {}^T/_8 + {}^T/_{16} + {}^T/_{32} = {}^{31T}/_{32} \approx 0.97T$ delay. As these dealys are present within the PLL loop have adverse affects on the PLL performance. Similar problems also exist in other PLL systems that involve dq-frame time delay, such as the one in

(Bradaschia et al., 2008), (Souza et al., 2009), (Neves et al., 2010). Thus to overcome this issue the DSC/CDSC operators should be moved outside the PLL loop to ensure the PLL stability with haigh gains. This section presents the mapping of dq-frame DSC/CDSC operators to $\alpha\beta$ frame mathematically.

As shown in the figure the dq-frame harmonic space vector $\overrightarrow{v}^{h}_{dq}(t)$ can be associated with the corresponding $\alpha\beta$-frame vector $\overrightarrow{v}^{h+1}_{\alpha\beta}(t)$ with angle ϑ (the difference between d axis and α axis). Therefore

$$\begin{aligned}\overrightarrow{v}^{h}_{dq}(t) &= Ve^{j\delta^h} = Ve^{j\left(\theta^{h+1}-\vartheta\right)} \\ &= e^{-j\vartheta}.Ve^{j\theta^{h+1}} = e^{-j\vartheta}.\overrightarrow{v}^{h+1}_{\alpha\beta}(t)\end{aligned} \tag{3.40}$$

Similarly the delayed vector $\overrightarrow{v}^{h}_{dq}(t - {}^{T}/_{n})$ can be witten as

$$\overrightarrow{v}^{h}_{dq}(t - {}^{T}/_{n}) = e^{-j(\vartheta - 2\pi/n)}.\overrightarrow{v}^{h+1}_{\alpha\beta}(t - {}^{T}/_{n}) \tag{3.41}$$

substituting the equations (3.40) & (3.41) in (3.32) we obtain

$$\alpha\beta DSC_n\left[\overrightarrow{v}^{h}_{\alpha\beta}(t)\right] = \frac{1}{2}\left[\overrightarrow{v}^{h}_{\alpha\beta}(t) + e^{j2\pi/n}.\overrightarrow{v}^{h}_{\alpha\beta}(t - {}^{T}/_{n})\right] \tag{3.42}$$

after expansion of the above equation the time domain representation is given as

$$\alpha\beta DSC_n\left[v^{h}_{\alpha\beta}(t)\right] = \frac{1}{2}\begin{bmatrix} v^{h}_{\alpha}(t) + cos\left(\frac{2\pi}{n}\right)v^{h}_{\alpha}(t - {}^{T}/_{n}) - sin\left(\frac{2\pi}{n}\right)v^{h}_{\beta}(t - {}^{T}/_{n}) \\ v^{h}_{\beta}(t) + cos\left(\frac{2\pi}{n}\right)v^{h}_{\beta}(t - {}^{T}/_{n}) + sin\left(\frac{2\pi}{n}\right)v^{h}_{\alpha}(t - {}^{T}/_{n}) \end{bmatrix} \tag{3.43}$$

Even though this technique can suppress symmetric odd harmonics and negative sequence components, it is not capable of blocking asymmetric odd harmonics. This concept can be extended to filter out other harmonics. This requires a generalized model of delay operator DSC_n which can be obtained in stationary frame or in SRF. These delay operators are cascaded to obtain Cascaded Delayed Signal Cancellation (CDSC) filter (Golestan et al., 2015), (Wang and Wei Li, 2011). The delay operator can be expressed in stationary frame by converting it from SRF.

$$dqDSC_n\left[v_{dq}(t)\right] = \frac{1}{2}\left[v_{dq}(t) + v_{dq}(t - {}^{T}/_{n})\right] \tag{3.44}$$

$$v_{dq}(t) = e^{-j\theta'}\left(v_{\alpha\beta}\right) \tag{3.45}$$

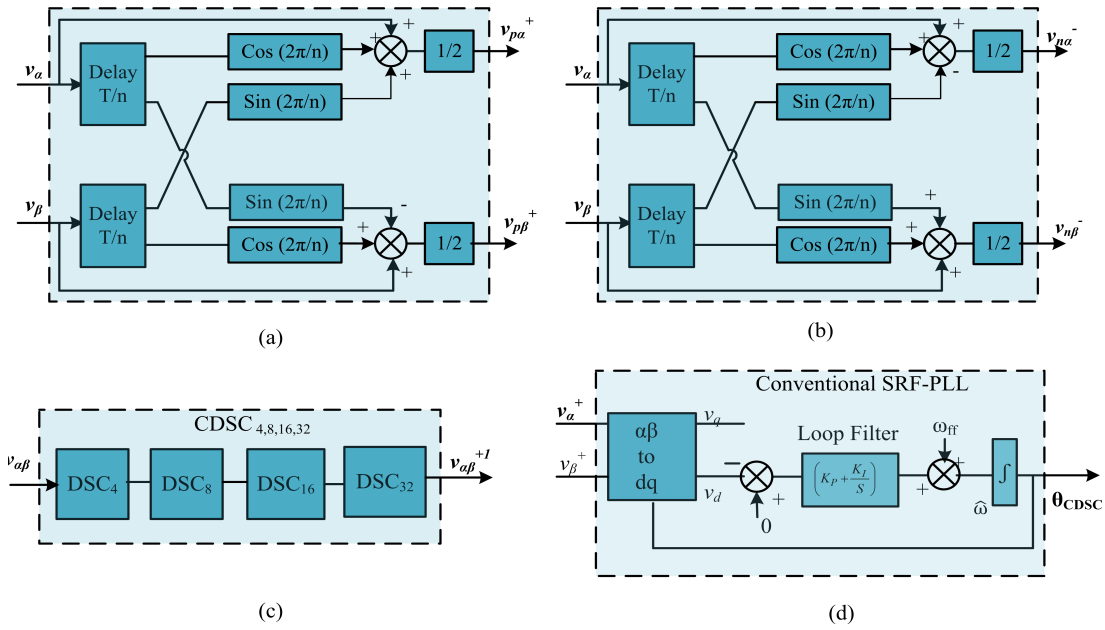


Figure 3.6: (a) Positive sequence extractor. (b) Negative sequence extractor. (c) CDSC filter. (d) CDSC-PLL

$$v_{dq}(t - {}^{T}/_{n}) = e^{-j(\theta' - 2\pi/n)}\,(v_{\alpha\beta}) \tag{3.46}$$

DSC_n represents generalized delay operator which delays the input signal by ${}^{T}/_{n}$. Positive sequence voltages after application of a DSC_n operator are given in (3.47) as shown in Figure 3.6(a) similarly negative sequence voltages can also be obtained as shown in Figure 3.6(b) and (3.48) depicts the respective mathematical equation

$$\begin{bmatrix} v^{+}_{\alpha n} \\ v^{+}_{\beta n} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_\alpha + v_\alpha(t - {}^{T}/_{n})cos\left(\frac{2\pi}{n}\right) + v_\beta(t - {}^{T}/_{n})sin\left(\frac{2\pi}{n}\right) \\ v_\beta + v_\beta(t - {}^{T}/_{n})cos\left(\frac{2\pi}{n}\right) - v_\alpha(t - {}^{T}/_{n})sin\left(\frac{2\pi}{n}\right) \end{bmatrix} \tag{3.47}$$

$$\begin{bmatrix} v^{-}_{\alpha n} \\ v^{-}_{\beta n} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_\alpha + v_\alpha(t - {}^{T}/_{n})cos\left(\frac{2\pi}{n}\right) - v_\beta(t - {}^{T}/_{n})sin\left(\frac{2\pi}{n}\right) \\ v_\beta + v_\beta(t - {}^{T}/_{n})cos\left(\frac{2\pi}{n}\right) + v_\alpha(t - {}^{T}/_{n})sin\left(\frac{2\pi}{n}\right) \end{bmatrix} \tag{3.48}$$

The transfer function of the DSC_n operator can be represented as shown in (3.49).

$$DSC_n(j\omega) = \left|cos\left(\left(\frac{\omega T}{2n}\right) - \frac{\pi}{n}\right)\right| \angle - \left(\left(\frac{\omega T}{2n}\right) - \frac{\pi}{n}\right) \tag{3.49}$$

DSC_4 filter uses a single delay operator which is obtained by substituting n=4 in the

(3.47) and (3.48) . DSC filter can eliminate all odd order harmonics of order h=4k-1 (k=+1,+2..) as the gain offered by DSC_4 is zero for these harmonics but it allows h=4k+1 order harmonics to pass through which is evident from the gain offered by the DSC_n transfer function (3.49).

CDSC filter can overcome these problems as it uses multiple delay operators which are chosen to eliminate specific harmonics of interest. As discussed earlier the grid voltage consists of both asymmetric and symmetric harmonics, hence CDSC operators should possess the ability to filter these harmonics. Delay operators n=4,8,16,32 can block all the odd order harmonics upto 30^{th} order. Even order harmonics can be filtered out by adding an additional delay operator with n=2. As even order harmonics are very small, CDSC filter is formed by cascaded operators n=4,8,16 and 32. CDSC positive and negative sequence extractors are shown in Figure 3.6(a), (3.6(b)) respectively. $CDSC_{4,8,16,32}$ filter is shown in Figure 3.6(c) and Figure 3.6(d) shows the CDSC-PLL.

The performance of SRF-PLL is poor when the grid voltage is polluted with harmonics and negative sequence voltages. This issue can be resolved by using pre-filters such as DSC, CDSC and Double Second Order Generalized Integrator (DSOGI). The performance of CDSC pre-filter is better when the grid voltage contains asymmetric odd order harmonics whereas DSC and DSOGI filters cannot filter out these harmonics. Hence, a CDSC pre-filter is chosen for effective reference generation.

3.7 CDSC Extractor

The concept of harmonic extraction is based on harmonic gain i.e., a zero gain of a DSC on a harmonic signal means the DSC can eliminate the harmonic signal and on the other side unity gain means the harmonic can pass through without attenuation. In the above section the original CDSC operator which are first derived in dq frame and mapped to $\alpha\beta$-frame guarantees the elimination of undesired harmonics and always have the unity gain to positive sequence fundamental signal. The modified CDSC extractor can eliminate the fundamental positive sequence signal as well to achieve the target harmonic extraction.

Consider a set of three phase voltage signal v_{abc} as input to the selective harmonic detection block. As mentioned earlier the input signal is transformed to $\alpha\beta$-frame. If the original signal v_{abc} is distorted and/or unbalanced the resultant time domain signal

$v_{\alpha\beta}$ is summation of harmonic components i.e., $v_{\alpha\beta} = \sum v^h_{\alpha\beta}$, where h is harmonic order. Each harmonic component of $v^h_{\alpha\beta}$ can be represented in each $\alpha\beta$-frame through a space vector $\overrightarrow{v}^h_{\alpha\beta} = Ve^{h\omega t+\varphi}$, where V is the magnitude, ω is fundamental angular frequency, and φ is the initial phase angle. The positive-sequence harmonics ($h > 0$) of $v^h_{\alpha\beta}$ are rotating counterclockwise at hω frequency in the $\alpha\beta$-frame while $\alpha\beta$-frame while negative-sequence harmonic components ($h < 0$) are rotating clockwise.

3.7.1 Derivation of CDSC-extractor

As mentioned earlier that different harmonic components(space vector) of $v^h_{\alpha\beta}$ rotate at different frequencies ($h\omega$) which implies that these space vectors rotate with different angles in the same portion of time. This feature is used to distinguish them by delay operation. For example if $^T/_n$ is the delay time where T is the fundamental period and n is the delay factor then $\overrightarrow{v}^h_{\alpha\beta}(t - {}^T/_n)$ is the delayed version of h^{th} harmonic vector by $^T/_n$ is lagging the original vector by $\overrightarrow{v}^h_{\alpha\beta}(t)$ by an angle of

$$\theta_n = h\omega \cdot \frac{T}{n} = \frac{2\pi h}{n} \tag{3.50}$$

Now the delayed vector is rotated with a chosen angle θ_r and the resultant vector is called rotated vector. The delayed and rotated vector are together used with original vector to construct the CDSC extractor as follows

$$\begin{aligned} DSC_n\left[\overrightarrow{v}^h_{\alpha\beta}(t)\right] &= \frac{1}{2}\left[\overrightarrow{v}^h_{\alpha\beta}(t) + e^{-j\theta_r} \cdot \overrightarrow{v}^h_{\alpha\beta}(t - {}^T/_n)\right] \\ &= \frac{1}{2}\left[\overrightarrow{v}^h_{\alpha\beta}(t) + e^{-j\theta_r} \cdot e^{-j\theta_n} \cdot \overrightarrow{v}_{\alpha\beta}(t)\right] \\ &= \overrightarrow{v}^h_{\alpha\beta}(t) \cdot \frac{1 + e^{-j(\theta_r+\theta_n)}}{2} \\ &= \overrightarrow{v}^h_{\alpha\beta}(t) \cdot \overrightarrow{G} \end{aligned} \tag{3.51}$$

Where the harmonic gain $\overrightarrow{G} = \left[1 + e^{-j(\theta_r+\theta_n)}\right]/2$ is a complex number with magnitude G and phase angle ϕ and given as

$$\begin{aligned} \overrightarrow{G} &= \left|cos\left[{}^{(\theta_r+\theta_n)}/_2\right]\right| \\ \phi &= -\frac{(\theta_r + \theta_n)}{2} \end{aligned} \tag{3.52}$$

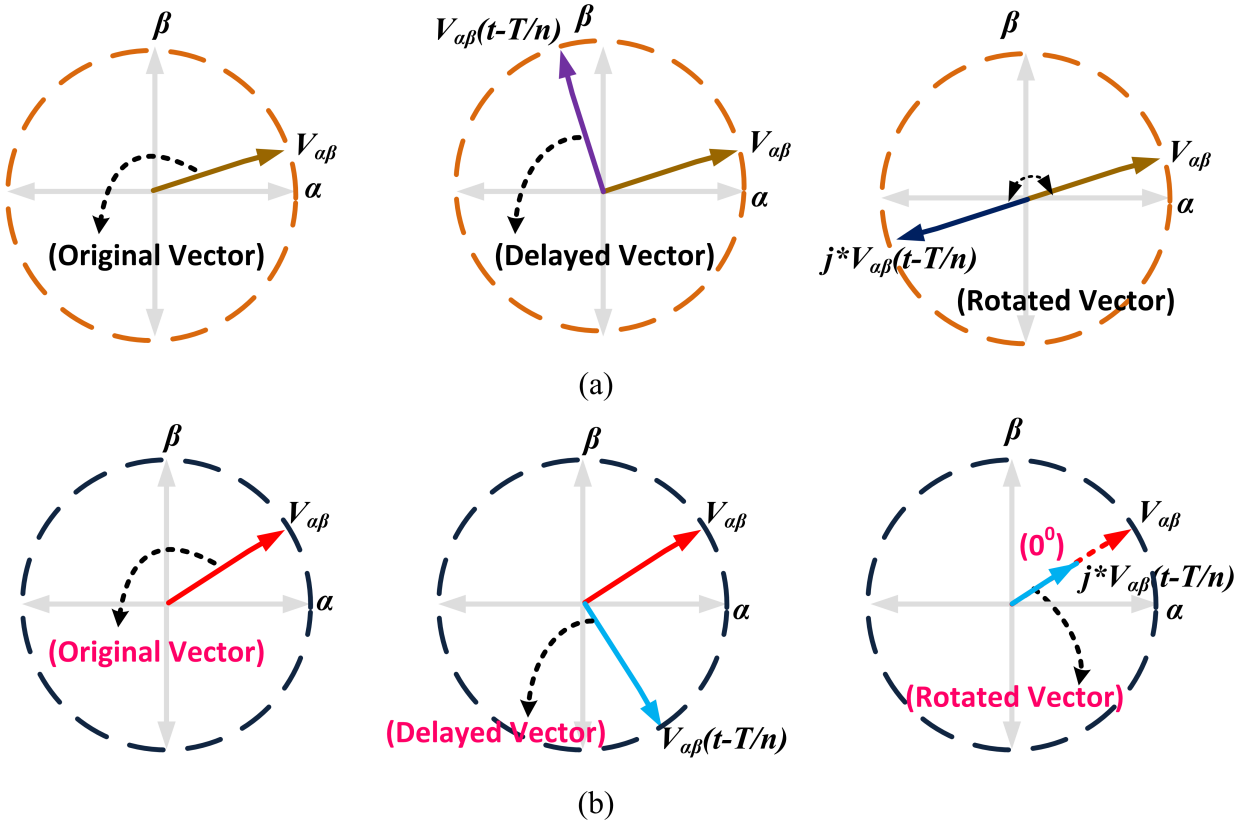


Figure 3.7: CDSC extractor Gain: (a)G=0,(b)G=1

From the above equation if θ_r=-θ_n the value of G=1 and on the other hand if θ_r= $\pi-\theta_n$ then the value of G=0.It can be concluded that the former case implies rotating vector is in phasse with original vector while the later case implies the rotating vector is in opposite phase to original vector as shown in Figure 3.7

The CDSC extractor is constructed as follows (Wang and Li, 2013)

$$DSC_n\left(\vec{v}^{h}_{\alpha\beta}\right) = \frac{1}{2}\left[\vec{v}^{h}_{\alpha\beta} + e^{-j\theta_r}.\vec{v}^{h}_{\alpha\beta}(t - {}^{T}/_{n})\right] \tag{3.53}$$

The space vector form of (3.53) can be rewritten into corresponding time domain signal form:

$$DSC_n\left(v_{\alpha\beta}(t)\right) = \frac{1}{2}\left[v_{\alpha\beta}(t) + R(\theta_r).v_{\alpha\beta}(t - {}^{T}/_{n})\right] \tag{3.54}$$

where $R(\theta_r)$ is given as $\begin{pmatrix} cos\theta_r & \sin\theta_r \\ -\sin\theta_r & cos\theta_r \end{pmatrix}$ and rotation angle $\theta_r = -2\pi h^*/n$.

For illustration purpose, let us consider a typical harmonic scenario where the

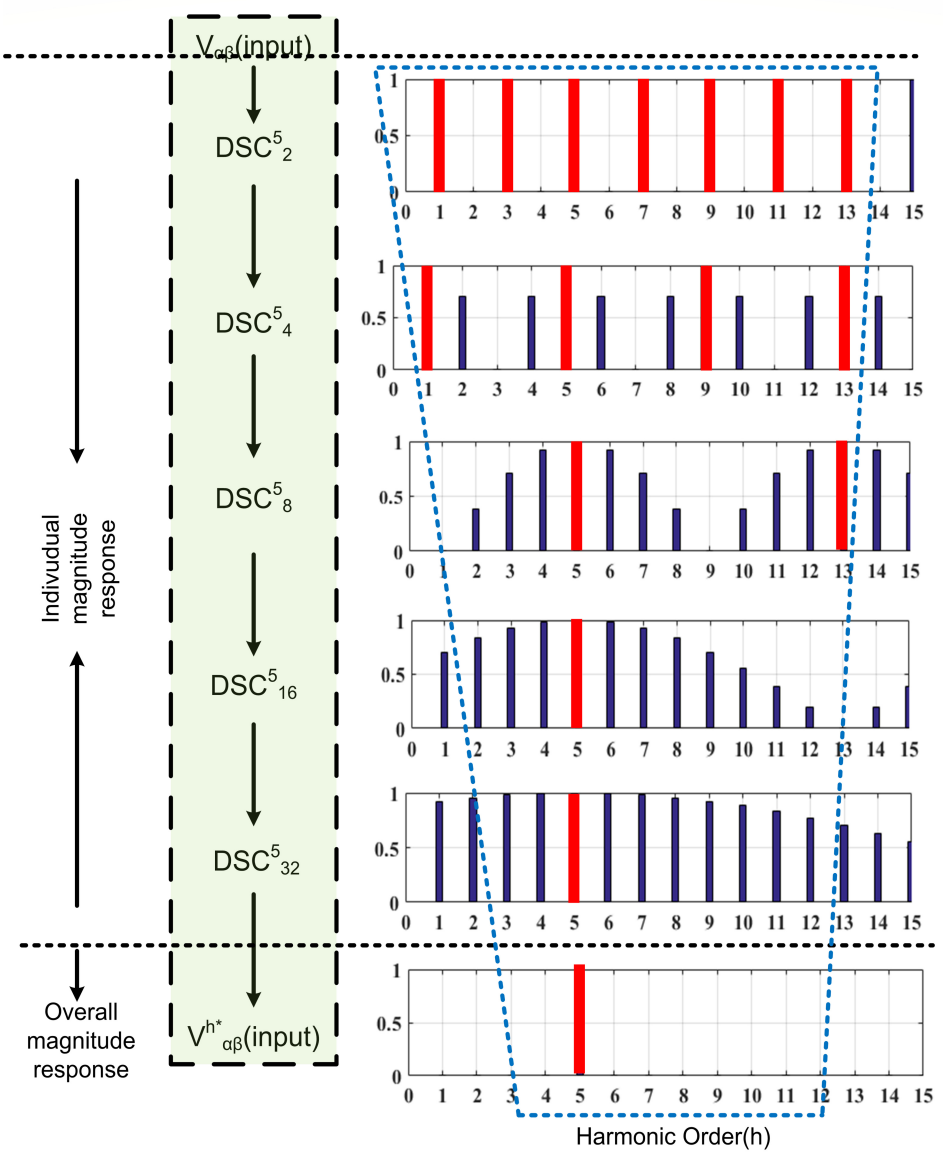


Figure 3.8: CDSC extractor:individual and overall magnitude response of $CDSC^5$ operator

voltage source consists of h=-1, 3,5, 7, 9, 11, 17, 19.....30. Let the target harmonic to be extracted is h^*=5 then CDSC should eliminate h=3, 7, 9, 11, 17, $\pm$19.....$\pm$30. To achieve this 5 DSC blocks of n=2(even order harmonics and DC components), n=4(-29, -25, -21, -17, -13, -9, -5, -1, 3, 7, 11, 15, 19, 23, 27, 31), n=8(-39, -31, -23, -15, -7, 1, 9, 17, 25, 33, 41) n=16(-19, -3, 13, 29) and n=32(-11, 21) are used. Figure 3.8 depicts that the constructed $CDSC^5$ operator eliminates all undesired harmonics by providing zero gain and extracts the 5^{th} harmonic component by providing unity

gain.

3.8 Frequency Adaptability feature of CDSC-PLL

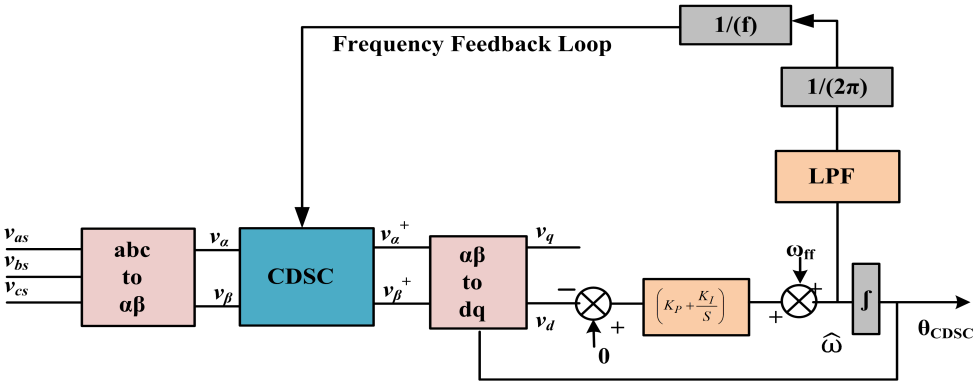


Figure 3.9: Block diagram of the $\alpha\beta$-frame CDSC-PLL system equipped with FFL for frequency adaptive grid phase detection

Besides harmonic distortion, grid voltage may also experience various frequency variations. In this case, it is no longer accurate to use a constant T=1/f s in the CDSC block to calculate the delay times. In order to equip the PLL system with frequency adaptability, T must be obtained in real time from the output frequency ω. A new control loop—the frequency feedback loop (FFL) (Wang and Li, 2013), is added to the CDSC-PLL system to fulfill such requirement. The modified system is shown in Figure 3.9.

$$F(s) = \frac{\omega_f}{s + \omega_f} \tag{3.55}$$

In the diagram, the estimated angular frequency ω is passed through a first order low-pass filter (LPF) and divided by 2π to generate estimated frequency $\hat{f}$. The reciprocal of $\hat{f}$ is the estimated period $\hat{T}$, which is then fedback to the CDSC block to calculate their delay intervals. Now with the FFL, the PLL comprises two loops with feedback variables as θ_{CDSC} and $\hat{T}$. The outer loop of $\hat{T}$ must work slower than the inner loop of θ_{CDSC} to maintain stability. This is realized by the LPF placed in the FFL. However, by properly tuning the LPF cut-off frequency ω_f, the dynamics of the inner and the outer loops can be optimally matched.

3.9 Reference Generation

The compensation voltage injected by DVR includes both fundamental and non-fundamental component. The proposed dual role CDSC has a feature of generating both components simultaneously. Firstly, the prefilter extracts ISC of grid voltage and is fed to DVR control algorithm to generate fundamental component. Apart from that to achieve the harmonic mitigation of load voltages an extractor based on modified CDSC strategy is designed which generates non-fundamental component of compensation voltage and added in 180^0 phase opposition with the fundamental component. Thereby the use of additional controllers for harmonic compensation such as resonant controllers proposed in the literature can be eliminated because, the single CDSC operator is performing the dual role as pre-filter and extractor. In this application, many authors have addressed the harmonic compensation during unbalanced grid conditions but here an attempt is made to classify harmonics into symmetric, asymmetric and its compensation is achieved during distorted grid conditions.

3.10 Conclusion

This chaptetr systematically introduces the concept of dual role CDSC as PLL-prefilter for grid phase detection and as extractor (selective harmonic elimination) for load voltage compensation. It begins from the representation of grid voltage harmonic signal and the structure and the operating principles of basic SRF-PLL system.

The performance of SRF-PLL is poor when the grid voltage is polluted with harmonics and negative sequence voltages. This issue can be resolved by using the prefilters such as, DSC, DSOGI and CDSC. The performance of CDSC prefilter is better when grid voltage contains symmetric and asymmetric voltage sags and harmonics whereas DSC and DSOGI cannot filter out these asymmetric harmonics. Hence, CDSC prefilter is chosen for effective reference generation and control of DVR. On the other hand, to achieve harmonic mitigation of load voltages due to distorted source an extractor based on modified CDSC strategy is designed. As DSC is a single operator and cannot eliminate all the undesired harmonics so multiple DSC operators are cascaded together (CDSC) to eliminate all undesired harmonics. Thus, dual role CDSC contributes to the generation of fundamental component (from CDSC prefilter) plus non-fundamental component (extractor) of the compensation voltage.

Chapter 4

Performance analysis of proposed dual role CDSC based DVC control of DVR

Contents

4.1 Introduction

In this chapter the DVR control strategy is analyzed. Open loop or feedforward control of DVR offers stability but has poor transient response. Also open loop control might result in a steady state error while tracking the DVR reference voltages as it doesnt consider the voltage drop in the transformer or inductor. Hence, closed loop control is preferred. A single loop controller with a capacitor voltage or load voltage feedback offers trade off between steady state response and transient response (Xiaoqiang et al., 2008), (Hatziargyriou et al., 2007). Hence, multiloop controllers with an additional current feedback are preferred for DVR control. LC filter plays a major role in determining the transient response of DVR. Hence, a mathematical model is derived for DVR with LC filter.

In this chapter a modified Dual Vector Control (DVC) algorithm is presented for DVR control. Firstly, the general control scheme for DVR is presented. Furhter the mathematical model of DVR is derived in dq-frame and followed by discussion on dual role CDSC based DVC algorithm for compensation of upstram faults. Then the other part of chapter focuses on the perfromance analysis of proposed dual role CDSC based DVC control of DVR under distorted grid conditions viz., symmetrical and asymmetrical voltage sags, voltage harmonics through simulation and experimental studies.

4.1.1 Basic multiloop structure

The structure of multiloop is still favoured because of its simplicity in control and natural hierarchy of bandwidth requirement. In multiloop controller generally two loops have been considered, the outer loop as voltage feedback which aims for regulating the load voltage and the inner loop as current feedback which enhances the dynamic response and gives protection against overcurrent. The voltage feedback loop can have either load voltage or capacitor voltage as feedback. From simulation studies, it has been found that when capacitor voltage is considered as a feedback the steady state value of the load voltage is slightly less than the reference value (the difference is same as the transformer loss). Therefore, load voltage feedback is considered in outer loop. Similarly, current feedback loop can have either inductor current or capacitor current as feedback. In this section for analysis purpose, the inductor current is considered as current loop feedback. The general control scheme for DVR with feedforward structure is shown in Figure 4.1. When sag occurs, the measured load voltage is compared with reference voltage and the resultant error is fed to voltage controller. The output of the voltage controller is compared with the inductor current and the resultant is fed to the current controller (proportional) as shown in Figure 4.1

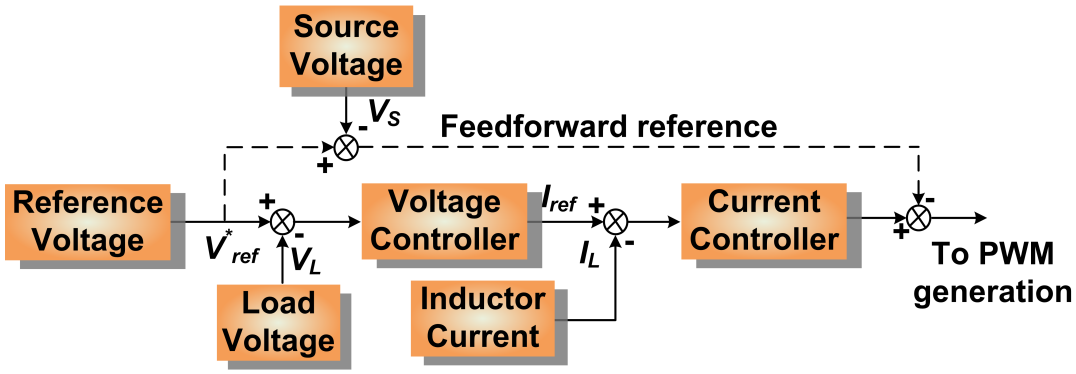


Figure 4.1: General control scheme for DVR

4.2 Mathematical model of DVR

Single line diagram of DVR is shown in Figure 4.2. For deriving the mathematical model, L filter is modeled as an inductor with small resistance (R+jωL),transformer

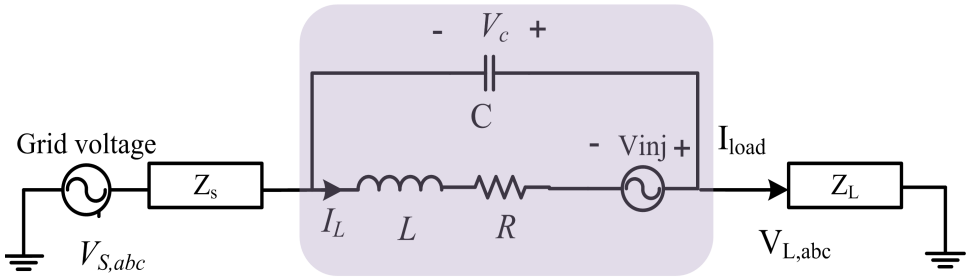


Figure 4.2: Single line diagram of DVR

is considered to be ideal with a ratio of 1:1 and is modeled as a voltage source with voltage v_i (Wang and Illindala, 2006b) to represent DVR injected voltages.

The dynamic equations of LC filter in abc frame are

$$\frac{di_{L,abc}}{dt} = \frac{1}{L}\left(v_{i,abc} - v_{c,abc} - i_{L,abc}R\right); \frac{dv_{c,abc}}{dt} = \frac{1}{C}\left(i_{L,abc} - i_{load,abc}\right); \tag{4.1}$$

where v_C, i_L, v_i, i_{load} represent capacitor voltage, inductor current, inverter voltage and load current respectively. These equations are converted to stationary frame as given below

$$\frac{di_{L,\alpha\beta}}{dt} = \frac{1}{L}\left(v_{i,\alpha\beta} - v_{C,\alpha\beta} - i_{L,\alpha\beta}R\right); \frac{dv_{C,\alpha\beta}}{dt} = \frac{1}{C}\left(i_{L,\alpha\beta} - i_{load,\alpha\beta}\right); \tag{4.2}$$

These equations in (4.2) are converted to positive synchronous reference frame ($\left(dq^{+}\right)$-frame) and negative synchronous reference frame ($\left(dq^{-}\right)$-frame) respectively to get (4.3) - (4.6) respectively.

$$\left(\frac{di_{L,dq}}{dt}\right)^{+} = \frac{1}{L}\left[v^{+}_{i,dq} - v^{+}_{C,dq} - i^{+}_{L,dq}R\right] - j\omega i_{L,dq} \tag{4.3}$$

$$\left(\frac{dv_{C,dq}}{dt}\right)^{+} = \frac{1}{C}\left[i^{+}_{L,dq} - i^{+}_{load,dq}\right] - j\omega v_{C,dq} \tag{4.4}$$

$$\left(\frac{dv_{L,dq}}{dt}\right)^{-} = \frac{1}{L}\left[v^{-}_{i,dq} - v^{-}_{C,dq} - i^{-}_{L,dq}R\right] + j\omega i^{-}_{L,dq} \tag{4.5}$$

$$\left(\frac{dv_{C,dq}}{dt}\right)^{-} = \frac{1}{C}\left[i^{-}_{L,dq} - i^{-}_{load,dq}\right] + j\omega v_{C,dq} \tag{4.6}$$

where '+' represents positive sequence and - represents negative sequence.

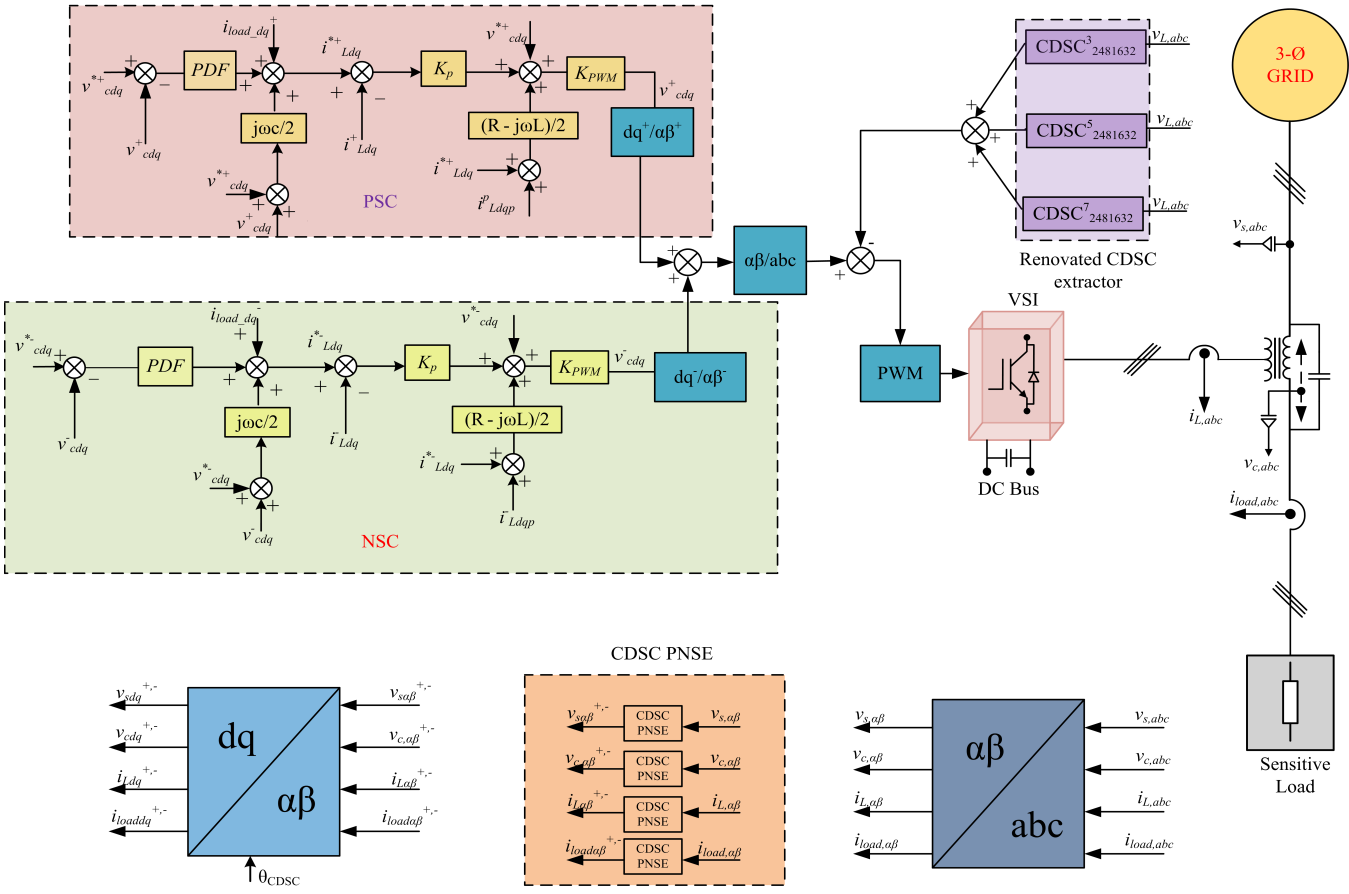


Figure 4.3: Control block diagram of DVR

4.3 Dual role CDSC-based DVC algorithm

DVC algorithm proposed in (Awad and Svensson, 2002) is a multiloop controller with capacitor voltage and inductor current feedback. This controller is obtained by discretizing the system equations in *dq*-frame using forward euler method. However, this algorithm doesnt have sequence decomposition and hence performs poorly under unbalanced grid voltages. Modified DVC with positive and negative sequence controllers is proposed in (Awad et al., 2004a).In this control a DSC filter separates ISC of the grid voltage, feedback signals in dq-frame and can control them independently.

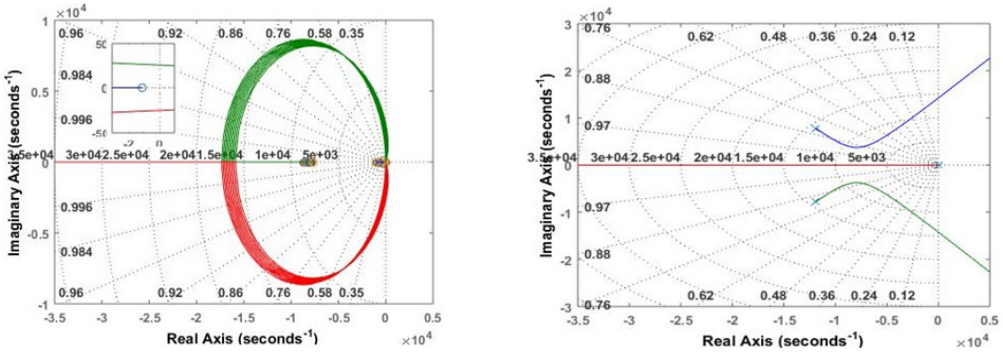
In the present work a dual role CDSC-based DVC algorithm for DVR is proposed to compensate the symmetrical and asymmetrical voltage sags and harmonics. Figure 4.3 depicts the schematic of proposed control algorithm. At first, the CDSC prefilter

extracts ISC of the fundamental grid voltage in stationary frame. The extracted ISC is transformed to the dq-frame and fed to the controller which generates fundamental component of compensation voltage. On the other hand, an extractor based on the modified CDSC strategy is designed which extracts the desired harmonic components from load voltages. The harmonic extraction block generates nonfundamental component of compensation voltage and added 180^0 phase opposition with fundamental component. Finally, the resultant is fed to pulsewidth modulation block to produce reference voltage for compensation. It has been considered that a sufficient battery energy storage system supports the real power required by the dc-link capacitor of DVR. The DVC implemented is a multiloop with a capacitor voltage and inductor current as feedback signals designed in the Synchronous Reference Frame (SRF). It consists of positive and negative sequence controllers (PSC and NSC) to compensate for balanced and unbalanced voltage sags. The voltage and current feedback loops of DVC employ proportional controllers to track the reference voltages accurately. Equations of the positive and negative sequence controllers are given in

$$\begin{aligned}
i^*_{Ldp} &= i_{load_dp} - \left(\frac{\omega C_f}{2}\right)\left(v^*_{Cqp} - v_{cqp}\right) + k_u\left(v^*_{Cdp} - v_{Cdp}\right) \\
i^*_{Lqp} &= i_{load_qp} - \left(\frac{\omega C_f}{2}\right)\left(v^*_{Cdp} - v_{cdp}\right) + k_u\left(v^*_{Cqp} - v_{Cqp}\right) \\
v^*_{iqp} &= v^*_{Cqp} + R_f i_{Lqp} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Ldp} - i_{Ldp}\right) + K_p\left(i^*_{Lqp} - i_{Lqp}\right) \\
v^*_{idp} &= v^*_{Cdp} + R_f i_{Ldp} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Lqp} - i_{Lqp}\right) + K_p\left(i^*_{Ldp} - i_{Ldp}\right)
\end{aligned} \tag{4.7}$$

$$\begin{aligned}
i^*_{Ldn} &= i_{load_dn} + \left(\frac{\omega C_f}{2}\right)\left(v^*_{Cqn} + v_{cqn}\right) + k_u\left(v^*_{Cdn} - v_{Cdn}\right) \\
i^*_{Lqn} &= i_{load_qn} - \left(\frac{\omega C_f}{2}\right)\left(v^*_{Cdn} + v_{cdn}\right) + k_u\left(v^*_{Cqn} - v_{Cqn}\right) \\
v^*_{iqn} &= v^*_{Cqn} + R_f i_{Lqn} - \left(\frac{\omega L_f}{2}\right)\left(i^*_{Ldn} - i_{Ldn}\right) + K_p\left(i^*_{Lqn} - i_{Lqn}\right) \\
v^*_{idn} &= v^*_{Cdn} + R_f i_{Ldn} + \left(\frac{\omega L_f}{2}\right)\left(i^*_{Lqn} + i_{Lqn}\right) + K_p\left(i^*_{Ldn} - i_{Ldn}\right)
\end{aligned} \tag{4.8}$$

where k_p and k_u are proportional gains of current and voltage loops, respectively, of the DVC. The PSC and NSC are shown in Figure 4.3.



(a) **(b)**

Figure 4.4: Root loci for P controller parameter tuning(a) Calculation of K_c for P controller (b) Calculation of K_v for P controller

4.3.1 Design of Controller Parameters

The objective of tuning the controller is to find the coefficients of the proposed CDSC-based DVC controller. The DVC implemented in this paper is a multiloop with a capacitor voltage and inductor current as feedback signals designed in the SRF. It consists of PSC and NSC to compensate for balanced and unbalanced voltage sags. The voltage and current feedback loops of DVC employ proportional controllers to track the reference voltages accurately. Both PSC and NSC constitutes of eight controllers (four with respect to PSC and four with respect to NSC). In this section, the tuning of two controller gains k_v and k_c among the four controllers of PSC is discussed. k_v refers to the outer loop voltage controller gain, and k_c refers to the inner loop current controller gain (PSC). An extended root locus design (RLD) (Kwon and Chang, 2016a) method is adopted to tune the controller coefficients. Figure 4.4(a) and 4.4(b) shows the extended RLD for tuning the coefficients of P controller. First, to tune the value of k_c, the root locus for k_c is drawn as shown in Figure 4.4(a) for all the values of k_v varied stepwise from its minimum stable value to maximum stable value obtained by Routh Hurwitz stability criterion. Based on the maximum relative stability, the optimal value of k_c is obtained. From the obtained value of k_c [see Figure 4.4(a)], the root locus is plotted for transfer function having gain k_v as shown in Figure 4.4(b) and the value of k_v is calculated based on its relative stability. To design the controller with high robustness, relative stability is considered for optimum tuning of controller parameters. It is essential that load voltage tracking accuracy should be sustained during voltage sags. Thus, the controller parameters are tuned

to address all the above requirements. The same procedure is followed to tune the other controller gains.

4.4 Simulation Results

In this section, performance analysis of CDSC-PLL is carried out in comparison with different PLLs viz Synchronous Reference Frame (SRF) -PLL, Delayed Signal Cancellation (DSC) -PLL and Dual Second Order Generalized Integrator (DSOGI) -PLL.

4.4.1 Time response of PLLs for step change in frequency

Figure 4.4 shows the numerical results when grid voltage undergoes a frequency step change of +3Hz. From settling time point of view i.e.., the time after which the estimated frequency reaches and remains within the tolerance band (5% considered) of its final value is around 3 cycles of fundamental frequency for CDSC-PLL. For DSOGI-PLL and DSC-PLL it is around 4 and 4.5 cycles respectively. It is observed that SRF-PLL (in Figure 4.5) the scale used is different to enhance its effect) for a given step change in frequency do not enter the 5% tolerance band even at 4 seconds. MATLAB is used for the representation of results.

4.4.2 Bandwidth of the PLL

Bandwidth of the PLL employed in the DVR involves a trade-off between two factors, the time response and the filtering performance. A larger bandwidth will result in a faster time response, which means that the PLL will need shorter time to resynchronize to the terminal voltage. A larger bandwidth also means a deteriorated filtering performance and the asymmetrical elements. As a result, range of typical bandwidth is 8 to 25 Hz (Hadjidemetriou et al., 2013). Magnitude bode diagram of different PLLs are shown in Figure 4.6. The simulation is carried out using MATLAB/SIMULINK.

4.4.3 Asymmetric harmonic response

A dynamic model has been implemented in PSCAD in order to simulate the operation of different PLLs i.e. CDSC-PLL, DSOGI-PLL, DSC-PLL, SRF-PLL and results are presented in Figure 4.7 under two phase sag with asymmetric grid voltage harmonics.

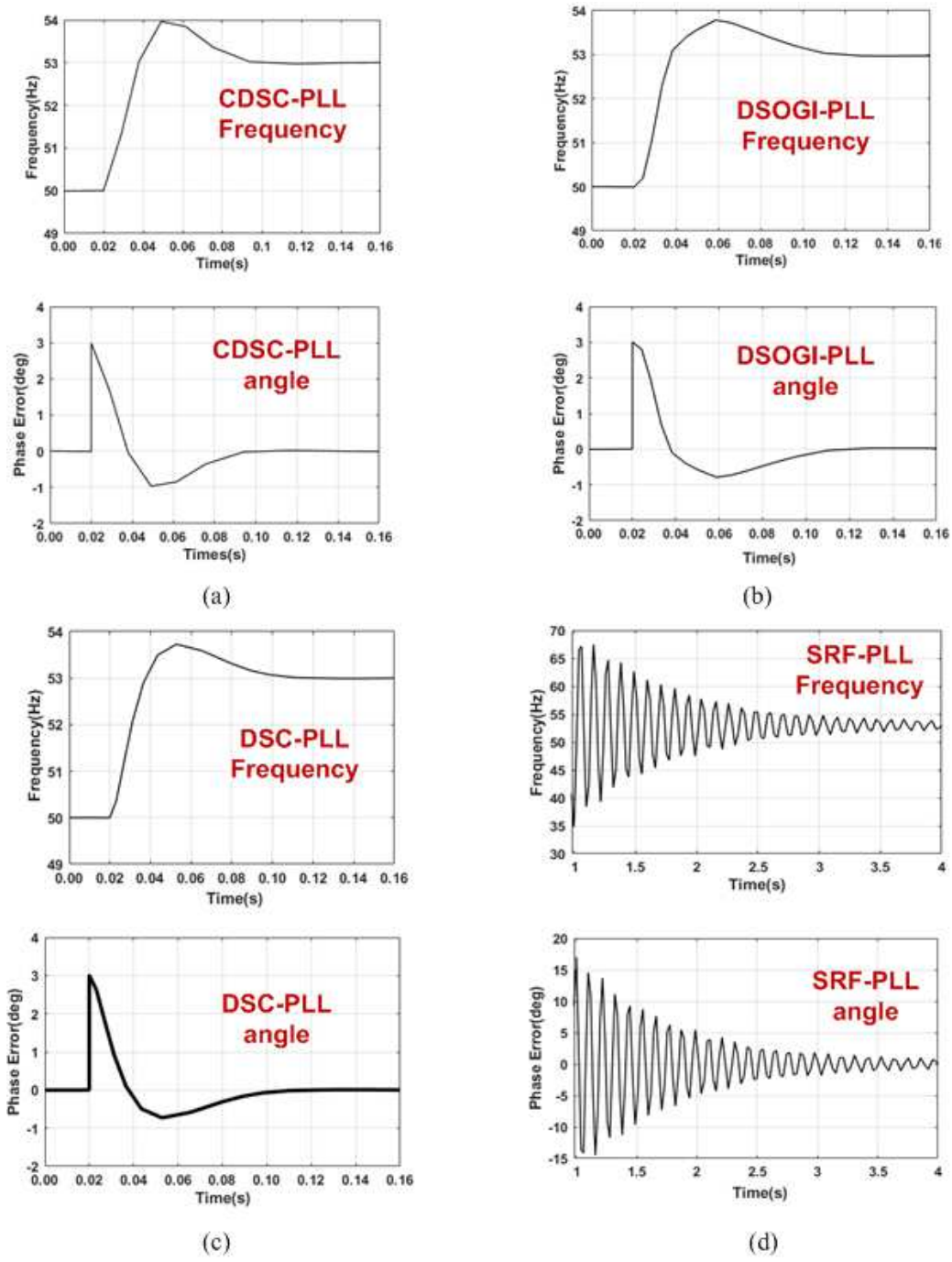


Figure 4.5: Time response of (a) CDSC-PLL, (b) DSOGI-PLL, (c) DSC-PLL, (d) SRF-PLL when grid voltage undergoes a frequency step change of +3Hz.

The operation of aforementioned PLLs is demonstrated in Figure 4.7(a)-(c), where

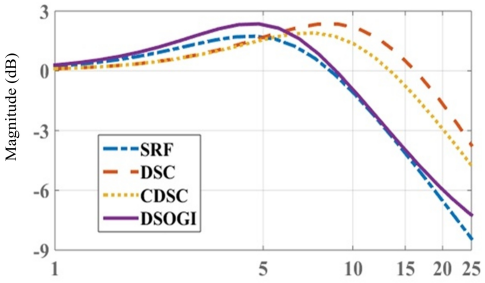


Figure 4.6: Magnitude Bode diagram of different PLLs

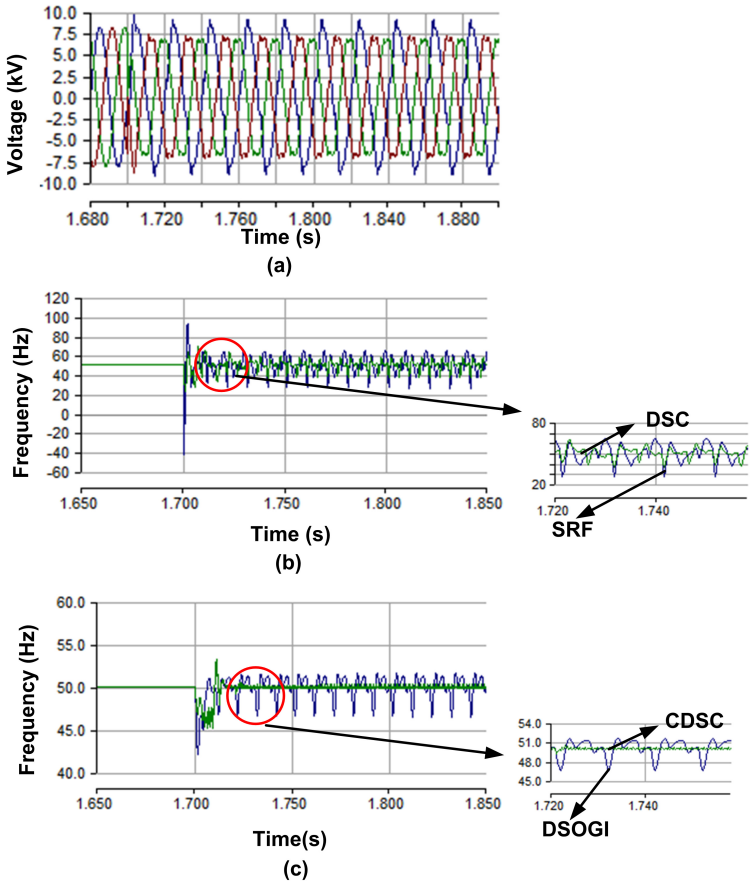


Figure 4.7: Simulation results for asymmetric harmonics with 20% sag in two phases: (a) Source voltage, (b) Frequency response of SRF-PLL and DSC-PLL, (c) Frequency response of DSOGI-PLL and CDSC-PLL.

it is noticed that time taken to detect frequency and phase angle is different for all PLLs. The moment when sag is created Figure 4.7 (b) shows that both SRF-PLL and DSC-PLL have an undershoot of more than 75% respectively. The time taken

by DSC-PLL to reach the tolerance band is 5ms but SRF-PLL oscillates above the tolerance band. Similarly, Figure 4.7 (c) depicts DSOGI-PLL and CDSC-PLL, though both PLLs take less time to reach tolerance band but possess an undershoot of 16% and 8% respectively. Therefore CDSC-PLL is the preferable solution as it is operating reliably during asymmetric voltage sags. Table4.1 summarizes the numerical analysis of different PLLs. According to that CDSC-PLL performs better when a step change of +3 Hz in frequency occurs as it takes 0.076 seconds to track the new frequency and during asymmetric harmonic case it exhibits an undershoot of 10% which is very less compared to DSOGI-PLL, DSC-PLL and SRF-PLL.

Table 4.1: Summarized performance of different PLLs

Performance parameter	**CDSC-PLL**	**DSOGI-PLL**	**DSC-PLL**	**SRF-PLL**
Settling time(s) for +3Hz change in frequency	0.076	0.15	0.19	Do not enter tolerance band
Bandwidth(Hz)	20	13.5	24	13
Asymmetric harmonic response-Undershoot(%)	10	24	61	75

Table 4.2: Test cases

Case No.	**Disturbances**		**Description**
1	Symmetric Sag (0.1s-0.3s)		30%(ph-a, ph-b, ph-c)
2	Asymmetric Sag	(a) Two Phase Sag (0.9s-1.1s)	30%(ph-b, ph-c)
		(b) Single Phase Sag (1.3s-1.5s)	30%(ph-b)
3	Symmetric odd oder harmonics with 30% balanced dip(1.7s-1.9s)		18.298%(),10%(7^{th}) (ph-a, ph-b, ph-c)
4	Asymmetric odd order harmonics with 20% dip in phase b and c (2.1s-2.3s)		(3^{rd}) (5^{th}) (7^{th}) 5.53%,7.23%,4.92% (ph-a) 8.82%,4.99%,4.89% (ph-b) 8.66%,3.68%,7.58% (ph-c)

4.4.4 Under various grid voltage disturbances

The performance of DSC, CDSC, and DSOGI pre-filters is evaluated under different test cases (Table 4.2) and specific results i.e., v_{dq} for asymmetric voltage sag, symmetric and asymmetric harmonics are presented. These pre-filters are subjected to unbalanced grid voltages as mentioned in Table.4.2 (case 2(a)) to assess their ability to filter out negative sequence voltages and extract positive sequence components of

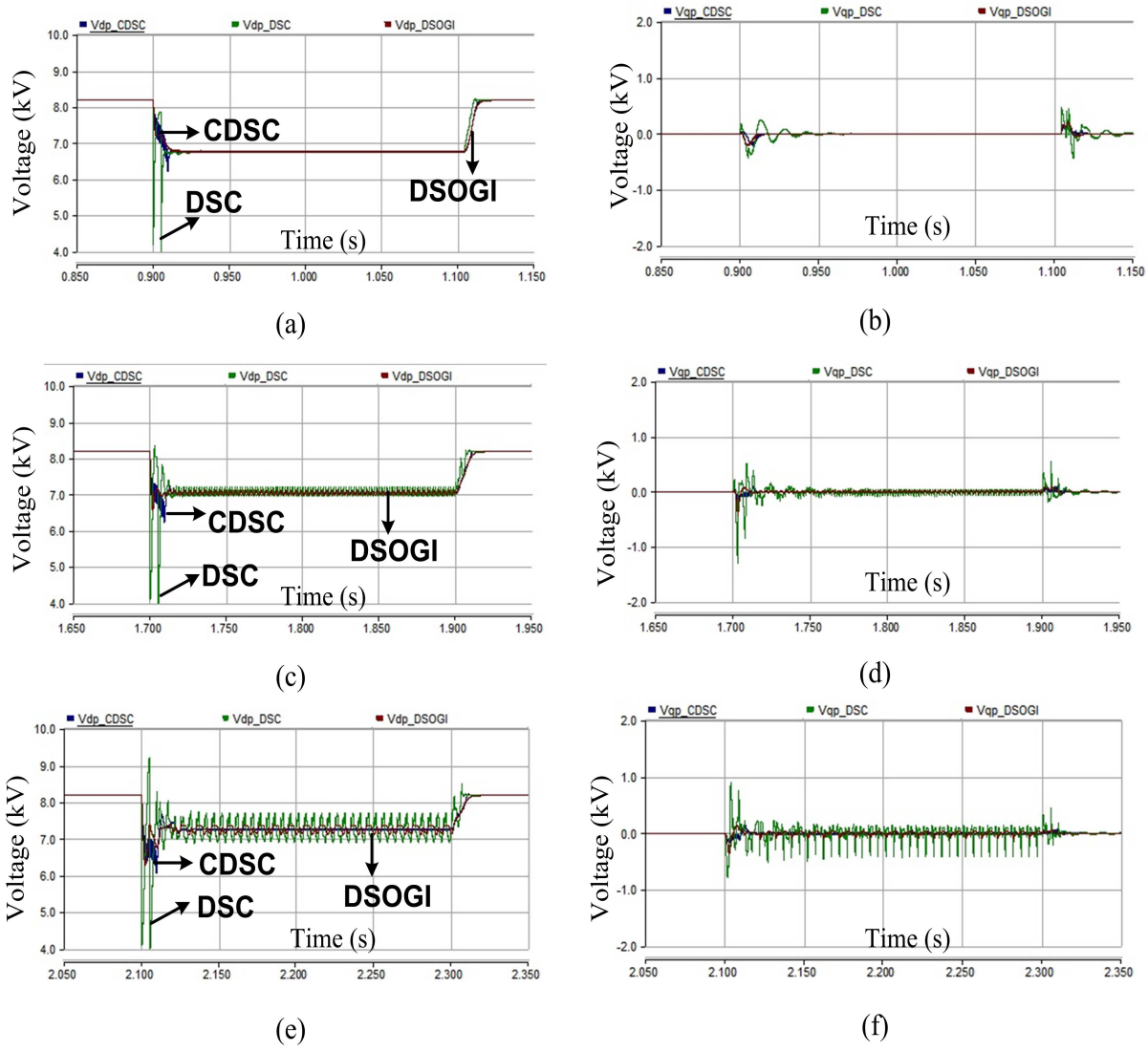


Figure 4.8: Positive sequence dq-voltages computed by DSC-PLL, DSOGI-PLL and CDSC-PLL (a), (b) v_d, v_q components under two phase sag respectively. (c), (d) v_d, v_q components under symmetric grid voltage harmonics respectively. (e), (f) v_d, v_q components under asymmetric grid voltage harmonics respectively.

the grid voltage in dq-frame v_{dq}. It can be observed from Figure 4.8(a), (b) that the dq-voltages estimated by these PLL algorithms do not contain any oscillatory terms. Similarly, the presence of symmetric voltage harmonics in the grid voltage, specified in Table.4.2 (case 3), would not affect the performance of these PLL algorithms as

shown in Figure 4.8 (c), (d) respectively. When single phase non-linear loads are connected at the PCC, the asymmetric grid voltage harmonics caused by the non-linear load, given in case 4, affects the performance of DSC and DSOGI pre-filters. This is evident from Figure 4.8 (e), (f) that v_{dq} estimated by these algorithms contain sustained oscillations. This fluctuation in dq-voltages makes it difficult to control DVR. The v_{dq} of CDSC-PLL shown in Figure 4.8 (e), (f) demonstrates the ability of CDSC operator to filter out asymmetric harmonic voltages and track the ISC of grid voltage accurately unlike the other two PLL algorithms. Further a caomparison table which portrays the advantages and disadvantages of aforementioned PLL's is given in 4.3

4.5 Simulation results of Proposed Dual Role CDSC based DVC for different voltage disturbances

A 10 kV medium voltage DVR (Godsk, 2002) is modeled in PSCAD/EMTDC to carryout simulation studies. Dual role CDSC based DVC algorithm with PDF voltage controller is implemented for DVR control. The simulation parameters are given in Table 4.3 and the proposed control algorithm is tested for different test conditions which are tabulated in Table 4.2 viz., symmetric and asymmetric voltage sags and harmonics. These test cases are chosen as theyre frequently occurring momentary voltage disturbances.

4.5.1 Compensation of symmetric and asymmetric voltage sags

- **Case 1:**A symmetric voltage sag of depth 30% is generated at t=0.1s for a period of 0.2s. Once the voltage sag occurs, DVR control detects it and generates switching pulses to the Voltage Source Inverter(VSI) to compensate for the voltage dip. As it is a symmetric voltage sag, DVR injects balanced three phase voltages (positive sequence voltages) and restores the load voltage to reference value. The waveforms of source voltage and injected voltage are shown in Figure 4.9(a). The balanced three phase voltage injected by DVR can be observed in Figure 4.9(a)

- **Case 2(a):** A two phase to ground fault initiated at t=0.9s leads to a voltage

Table 4.3: Comparison of Different PLL's

S.No.	Type of PLL	Advantages	Disadvantages
1	SRF PLL	Extracts the grid voltage and phase angle information	a) low Disturbance rejection selectivity. b) Low filtering capability. c) Poor performance during grid unbalance conditions d) Can not eliminate harmonics
2	SOGI PLLs	a) High Disturbance rejection selectivity. b) High filtering capability. c) Extracts the harmonics. d) Posses fast dynamic response	a) High computational burden. b) Cannot eliminate asymmetric harmonics.
3	DSC PLLs	a) High filtering capability. b) Extracts the harmonics. c) Posses fast dynamic response. d) Low computational burden.	a) Average disturbance selectivity. b) Cannot eliminate asymmetric harmonics.
4	CDSC PLLs	a) High filtering capability. b) Extracts the harmonics (wide range). c) Low computational burden. d) Noise immunity levels are high.	a) The dynamic response depends on the number of blocks cascaded

Table 4.4: Simulation parameters

Device	Description	Value
Supply	ACVoltage (LL rms)	10 kV
	Frequency	50Hz
	Supply impedance(Zs)	2.6 Ω, 0.006048 mH
Load(Delta)		45 kW/6670 Ω
Inveter	Switching Frequency	5kHz
	DC link Voltage	600V
Filter	Capacitance(Cf)	120 μF
	Inductance	260 μH
Injection Transformer(per phase)	Rated Power (Star)	67 KVA
	Primary voltage(V1)(LL)	2900 V
	Secondary voltage(V2)	290 V

dip of 30% in phase-b and phase-c, which lasts for a period of 0.2s till the fault is cleared at t=1.1s, whereas voltage in phase-a remains unaffected. From Figure 4.9(b) the performance of the control algorithm is unaffected even in the presence of unbalanced voltage sags as DVR injects both positive and negative sequence voltages and restores the load voltage to its reference voltage.

- **Case 2(b):**A single phase voltage sag of 30% depth is generated at t=1.3s in phase-a of source voltage for a duration of 0.2s. DVR maintains the load voltage at its reference value by injecting voltages in series with the source as shown in Figure 4.9(c).

  For the balanced and unbalanced voltage sags given in cases 1, 2(a) and 2(b) (specified in Table 4.2) it can be observed that the moment voltage sag occurs, sag detection algorithm detects dip in the voltage accurately. CDSC-PLL extracts the symmetrical components of grid voltage, which are used to generate reference voltages to be injected. DVR injects positive and negative sequences voltages so that constant voltage is maintained across the load.

4.5.2 Compensation of symmetric and asymmetric voltage Harmonics

- **Case 3:** Symmetric voltage harmonics are most commonly seen in the grid voltage.To test the effectiveness of the PLL and control algorithm, a non-linear load is connected upstream at the voltage source at t=1.7s for a period of 0.2s to generate symmetric odd order harmonics along with an unbalanced voltage sag

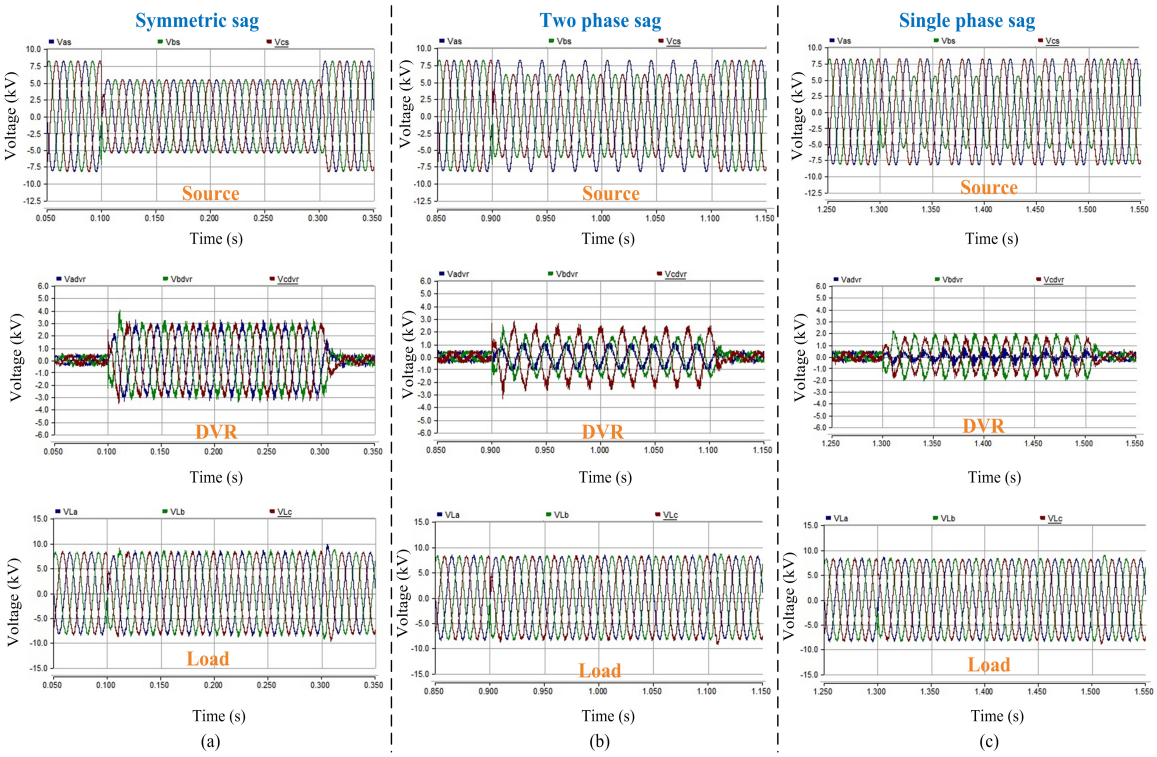


Figure 4.9: Source, DVR and load voltages under (a) symmetric sag (b) Two phase sag (c) single phase sag

of 20% in phase b and c. Figure 4.10(a) shows the source voltage, DVR injected voltage and load voltage respectively. Figure 4.10(b) shows the zoomed view of source, DVR injected and load voltages respectively for clarity. Fifth and seventh harmonic are found out to be 18.298%, 10% respectively at the source voltage with total THD of 21.47% as shown in Figure 4.10(c). It can also be observed that the percentage of third harmonics harmonics are found to be same in all the three phases confirming the presence of symmetric harmonics in the grid voltage. While the DVC control tracks the fundamental reference voltages, CDSC extractor cancel out the fifth and seventh harmonics present in the load voltage. From load voltage THD waveform shown in Figure 4.10(d), it can be observed that fifth harmonic is brought down to 2.94%, seventh harmonic is reduced to 1.56% and overall THD is reduced to 3.89%.

- **Case 4:** Two different non-linear loads are connected between different phases at t=2.1s for a period of 0.2s to generate asymmetric odd harmonics along with an unbalanced voltage sag of 20%. Under such non-linear load, voltage in phase

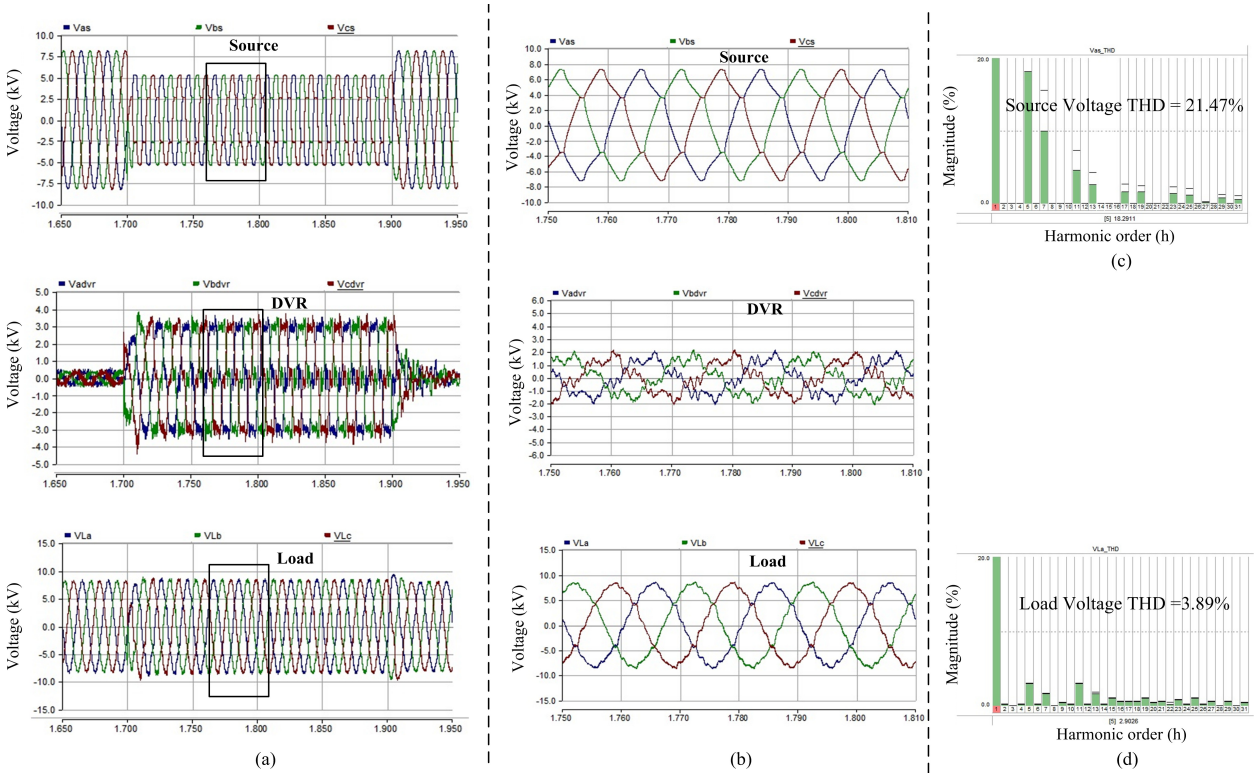


Figure 4.10: Compensating balanced sag with symmetric odd harmonics: (a) source, DVR and load voltages, (b) zoomed view under symmetric harmonics(c), (d) source and load THD waveform

b contains a third harmonic of 5.53%, fifth harmonic of 7.23%, and seventh harmonic of 4.95% with overall THD of 13.07% as shownin Figure 4.11(c). The imbalance in the percentage of harmonics which are seen in the three phases of grid voltages as specified in Table 4.2 shows that asymmetric voltage harmonics are present in the grid voltage. Unlike DSC-PLL, CDSC-PLL accurately tracks symmetric components of grid voltage even under asymmetric harmonics. DVC algorithm compensates for voltage sag and restores the fundamental of load voltage to nominal value as seen in Figure 4.11(a). Third, fifth and seventh harmonic controllers would compensate for the dominant lower order harmonics. The load voltage THD waveform in Figure 4.11(a), shows that the third, fifth and seventh harmonics are restricted to 0.99%, 1.45%, and 0.52% respectively. As a result, the load voltage THD is improved (3.7%) which is evident from the zoomed view of load voltages seen in Figure 4.11(b).

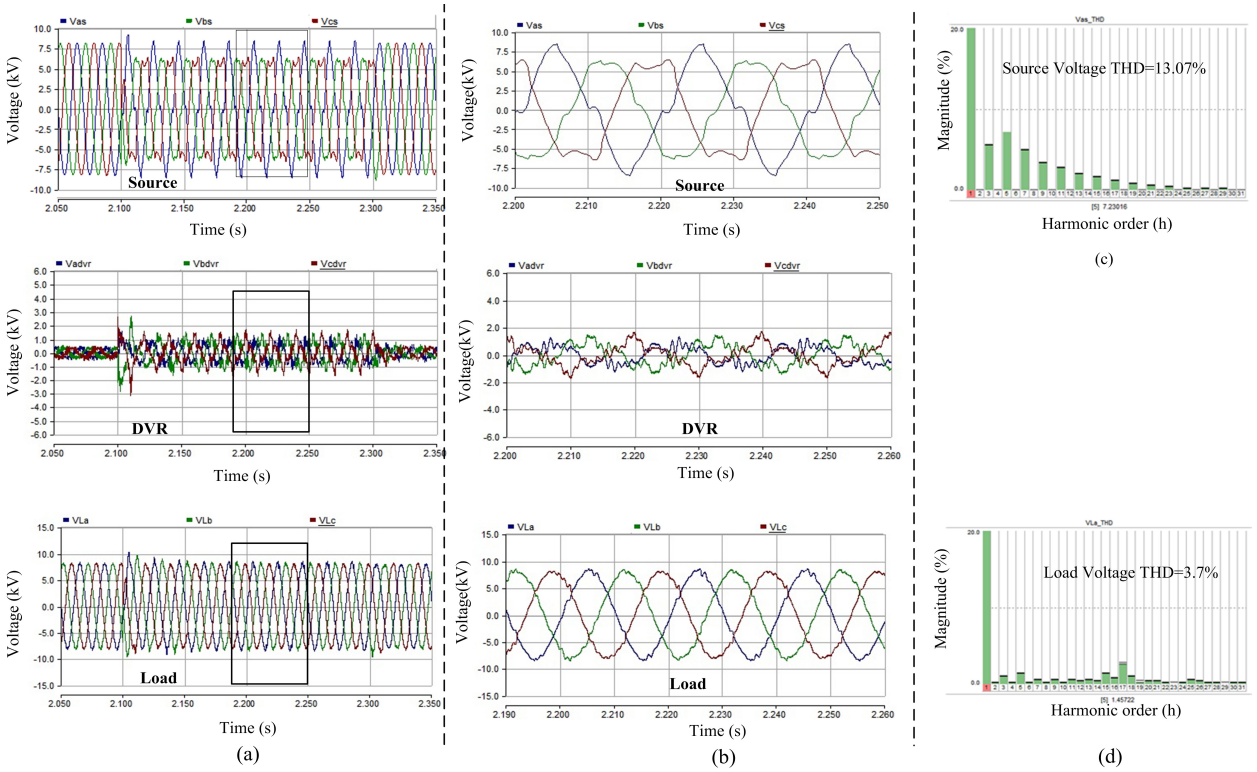


Figure 4.11: Compensating unbalanced sag with asymmetric odd order harmonics (a) source, DVR and load voltages, (b) zoomed view under asymmetric harmonics (c), (d) source and load THD waveform

4.5.3 Compensation of voltage swell

In this sub section the simulation results for compensation of voltage swell with proposed control technique is discussed. Generally in distribution system the voltage sag phenomenon is more prominent, thus the report mainly focus on symmetric and asymmetric voltage sags and harmonics. However, to show the efficacy of the proposed control technique for compensating voltage swell the respective simulation results are shown in Figure 4.12 . A voltage swell of 25% is generated at t=2.4s in all the three phase PCC voltages for a duration of 0.2s as shown in Figure 4.12(a). DVR injects the voltage 180^0 out of phase with the PCC voltages to mitigate voltage swell. The load voltages as shown in Figure 4.12(c) is maintained constant during the swell period. Thus, it can be concluded that the proposed control method is also suitable for compensating voltage swells.

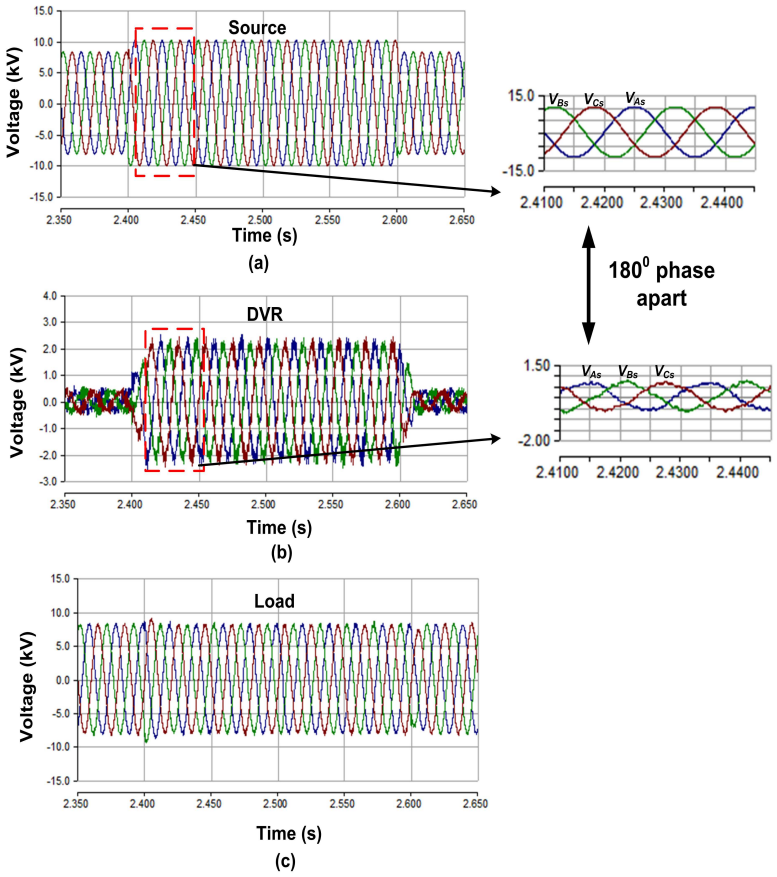


Figure 4.12: DVR compensation under voltage swell (a) source voltage (b) DVR voltage (c) load voltage

4.6 Experimental results of CDSC-PLL under different voltage disturbances

A robust PLL algorithm is necessary for effective reference generation and control of DVR. In simulation studies it is found that CDSC-PLL performs better in all the test cases considered. Hence, CDSC-PLL is implemented in Altera cyclone-II FPGA board (The experimental setup is discussed in Appendix-1). Prior to the testing of CDSC-PLL for different voltage disturbances the performance of dual role CDSC for symmetric and asymmetric harmonics case is validated and respective results are presented in the following subsection.

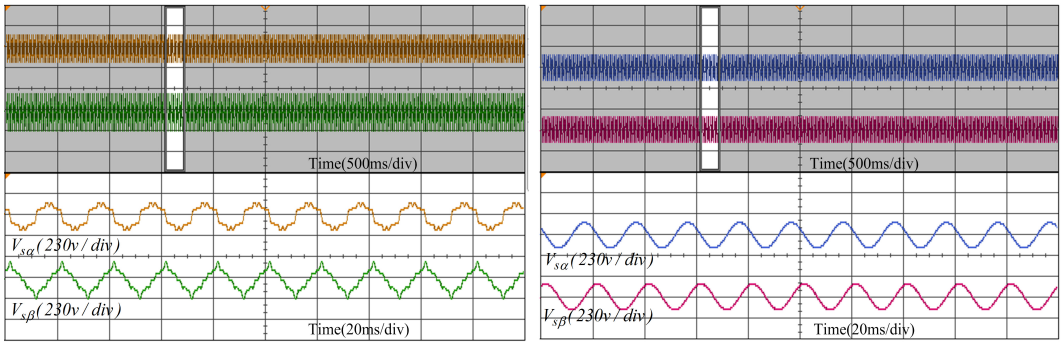


Figure 4.13: Source voltage waveforms under symmetric harmonics in $\alpha\beta$-frame: (a) before prefilter, (b) after prefilter

4.6.1 Performance of CDSC-Prefilter

In this section the performance of CDSC prefilter is analysed during symmetric and asymmetric harmonics case. Firstly, the source is distorted with the symmetric harmonic and the respective source voltage V_S waveform in $\alpha\beta$-frame is shown in Figure 4.13. The CDSC prefilter is fed with the distorted $V_{s\alpha\beta}$ which consists of 4 DSC blocks i.e., n=4,8,16,32. In this case the focus is mainly on 3^{rd}, 5^{th} and 7^{th} harmonics as they are dominant in the system. Figure 4.14 shows the output of respective DSC blocks. It can be inferred that the CDSC prefilter has eliminated the harmonics in the $V_{s\alpha\beta}$ as observed from the output of DSC_8 block which consists of fundamental component alone.

In the second case the $V_{s\alpha\beta}$ is distorted with asymmetric harmonics as shown in the Figure 4.15. This $V_{s\alpha\beta}$ is fed as input to the CDSC prefilter to extract the fundamental component. Figure 4.15 shows the output of respective DSC blocks. It can be observed that as the distorted $V_{s\alpha\beta}$ passes through the DSC_8 block all the harmonics present are not eliminated which is evident from Figure 4.15(b) and the resultant output(from DSC_4) passes to DSC_8 block. Figure 4.15(c) depicts the output of DSC_8 block and it can be observed that the fundamental is extracted which is harmonic free and the same waveform passes through DSC_{16} block. At this point the input to the DSC_{16} block is fundamental so it just act as buffer and produces the same fundamental waveform as seen from Figure 4.15(d).

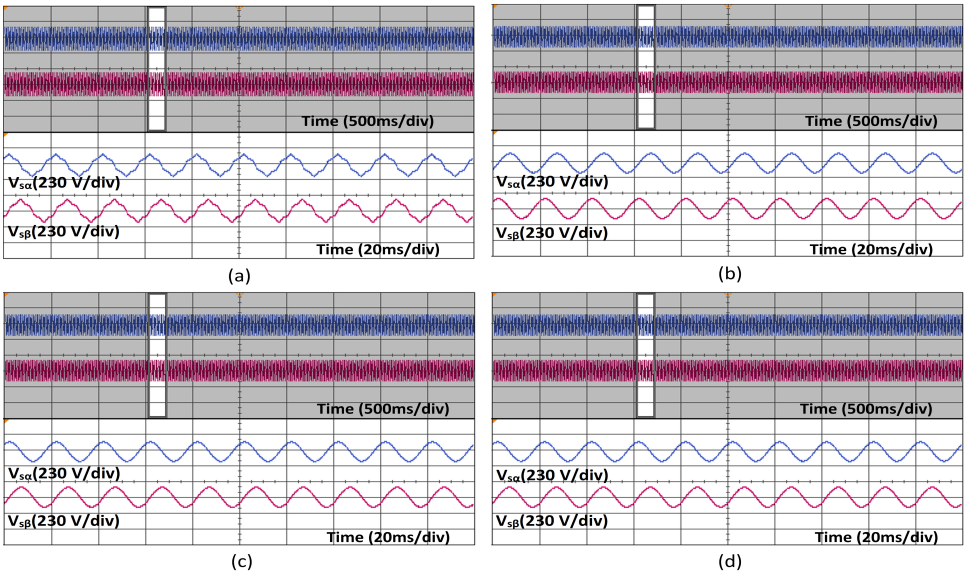


Figure 4.14: The output waveforms of respective DSC blocks of prefilter under symmetric harmonics in $\alpha\beta$-frame:(a)DSC_4, (b) DSC_8, (c) DSC_{16}, (d) DSC_{32}

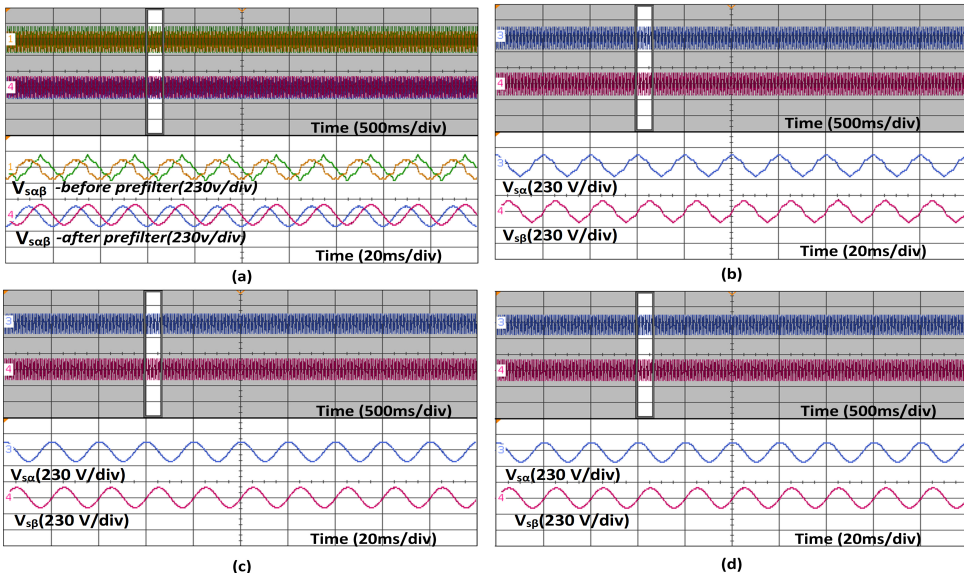


Figure 4.15: The output waveforms of respective DSC blocks of prefilter under asymmetric harmonics in $\alpha\beta$-frame (a) before and after prefilter, (b) DSC_4, (c)DSC_8, (d)DSC_{16}

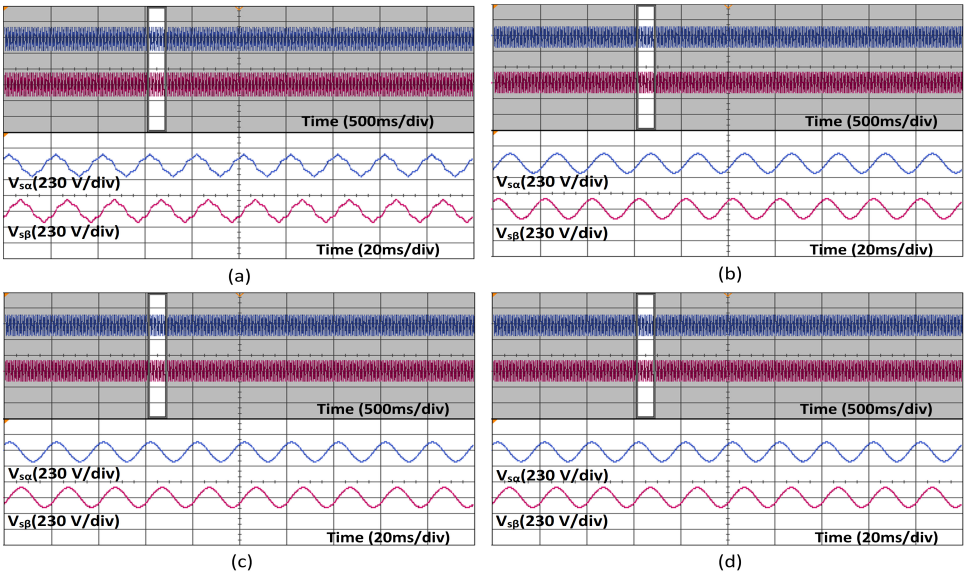


Figure 4.16: CDSC-extractor operation under symmetric harmonic case in $\alpha\beta$-frame (a)3^{rd} harmonic extractor output, (b) 5^{th} harmonic extractor output, (c)7^{th} harmonic extractor output

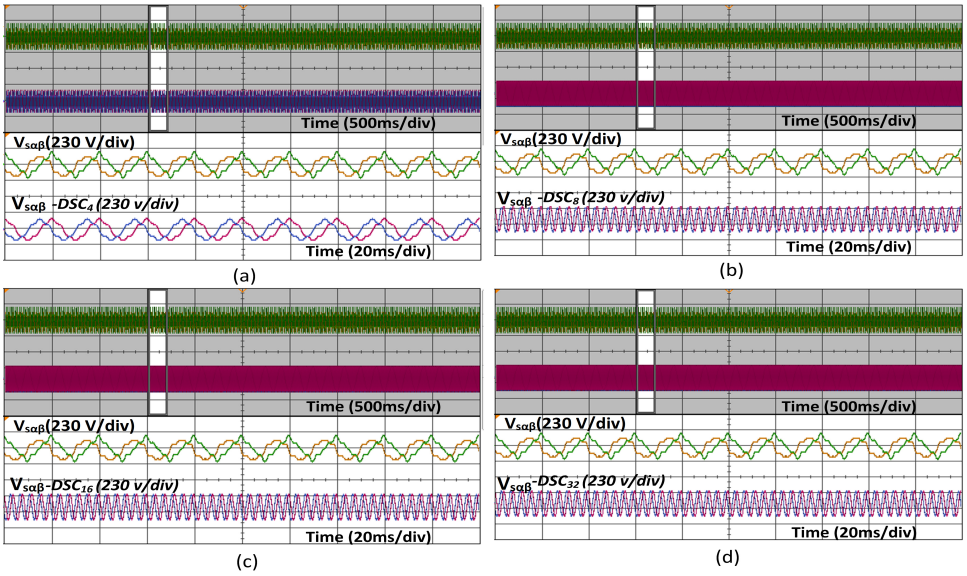


Figure 4.17: Operation of $CDSC^5$ extractor block to extract 5^{th} harmonic under symmetric harmonic in $\alpha\beta$-frame (a) DSC_4, (b)DSC_8, (c)DSC_{16}, (d)DSC_{32}

4.6.2 Performance of CDSC Extractor

As mentioned earlier that focus is mainly on dominant harmonics so extractor is designed for extraction of 3^{rd} ,5^{th} & 7^{th} harmonics. Firstly, consider the load is

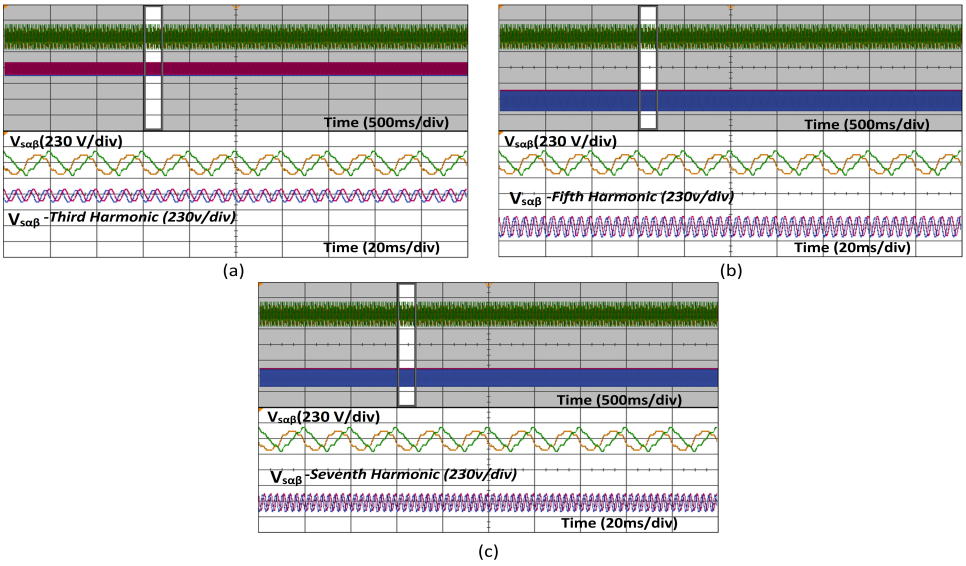


Figure 4.18: CDSC-extractor operation under asymmetric harmonic case in $\alpha\beta$-frame (a)3^{rd} harmonic extractor output, (b) 5^{th} harmonic extractor output, (c)7^{th} harmonic extractor output

supplied from source voltage which is distorted by the symmetric harmonics. The CDSC extractor is fed with the distorted input and it should extract the dominant harmonics by eliminating the other harmonics. Figure 4.16(a) shows the output of the CDSC third harmonic extractor where it can be observed that designed extractor is able to abstract the desired harmonic. Similarly, Figure 4.16(b),(c) shows the respective outputs of 5^{th} and 7^{th} harmonic extractor and it can be clearly seen that the desired harmonic extraction is achieved in proper manner.

To understand the operation of extractor let us consider the extraction of 5^{th} harmonic i.e., consider the 5^{th} CDSC extractor block which consists of blocks n=2,4,8,16,32. By observing the harmonic range of DSC_4 (i.e., h=-5,-1,3,7,11...) the 5^{th} harmonic can be extracted by providing gain 1 and rest can be eliminated by providing gain zero. Thus, from Figure 4.17(a) the output of DSC_4 block consists of 5^{th} harmonic and fundamental component. Similarly, from the harmonic range of DSC_8 (i.e., h=-7,1,9....) the fundamental component present in the output of DSC_4 block can be eliminated by passing through DSC_8 block by providing zero gain.Thus from Figure 4.17(b) the output of DSC_8 block consists of only 5^{th} harmonic component. Similarly, Figure 4.18 shows the operation of CDSC-extractor during asymmetric case and same observations can be seen in this case also. Finally, it can be concluded that single DSC block is not sufficient to eliminate all the desired harmonics and thus dual

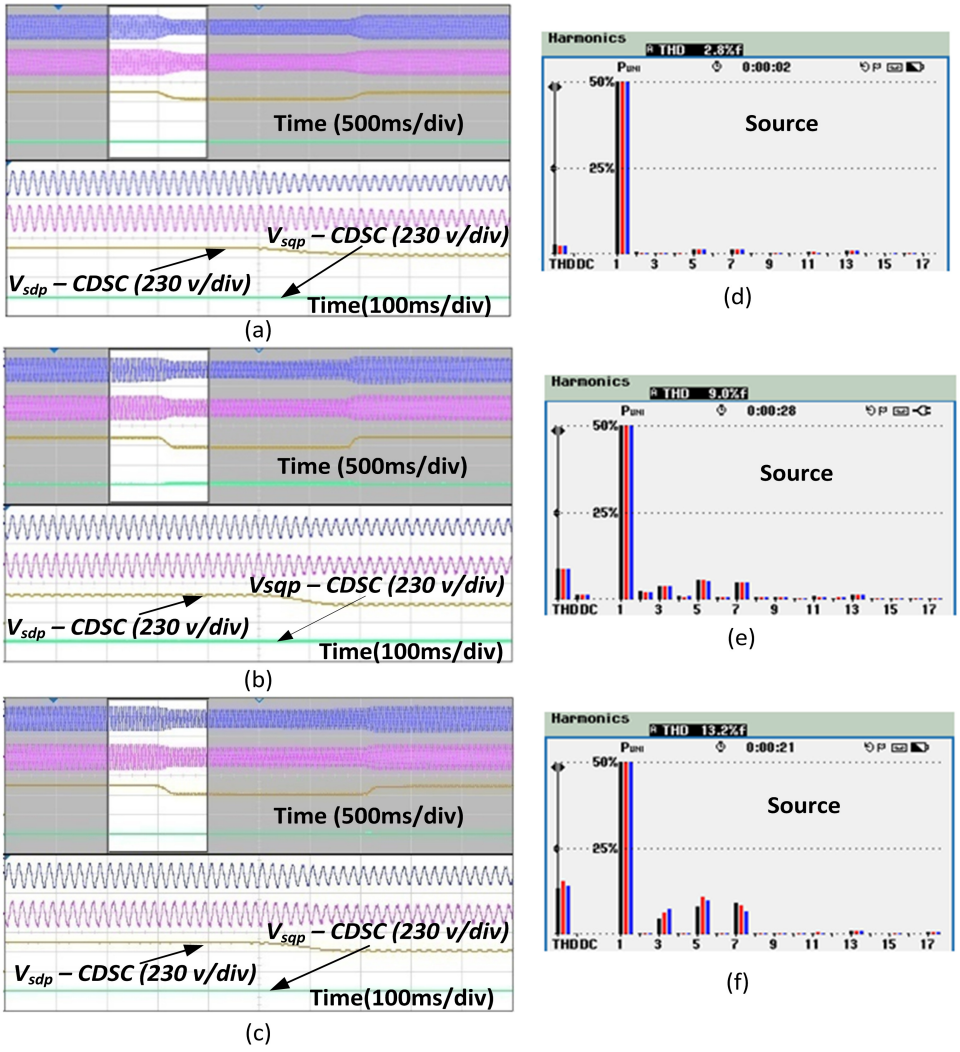


Figure 4.19: Source voltages and estimated dq_{sp}- voltages of CDSC-PLL under different test conditions: (a) two phase sag, (b) balanced sag with symmetric harmonics, (c) balanced sag with asymmetric harmonics, (d)-(f) harmonic spectrum of source voltage under two phase sag, symmetry and asymmetric harmonics.

role CDSC when configured as prefilter eliminates all the desired harmonics (symmetric and asymmetric) and extracts the fundamental while configured as extractor abstracts the desired harmonics eliminating fundamental component also.

4.6.3 Performance of CDSC-PLL

Case 1: Two phase sag

The CDSC-PLL algorithm is subjected to two phase sag to test its ability of eliminating the negative sequence voltages. During sag condition the negative sequence components present in the grid voltage leads to oscillating double frequency components in dq-voltages but CDSC prefilter is able to cancel out oscillating component to keep V_{sdq} (feedback source voltage) ripple free as shown in Figure 4.19(a). The source voltage is not distorted, and respective harmonic spectrum is given in Figure 4.19(d).

Case 2 : Asymmetric and symmetric harmonics

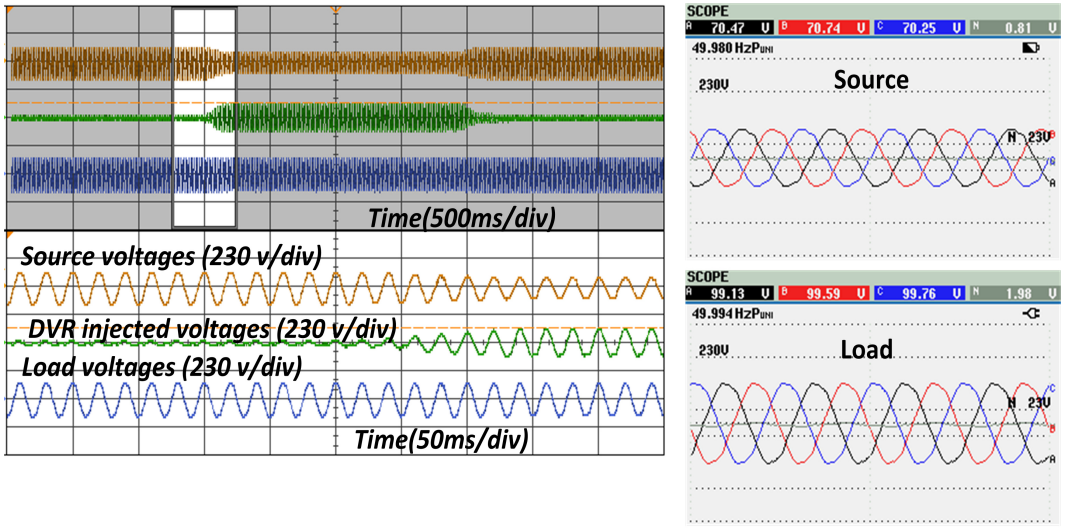
A balanced dip of 30% is generated in the supply voltage with symmetric and asymmetric harmonics. The absence of ripple in V_{sdq} (feedback source voltage) which is output of CDSC-PLL shown in Figure 4.19(b), (c) indicates the effectiveness of its prefilter in eliminating harmonics.Figure 4.19(e) shows the respective symmetric harmonic contents in source voltage and it possess a THD of 9.0%. Similarly, the asymmetric harmonic portion in source voltage is given in Figure 4.19(f) where its THD content is 13.2%.

4.6.4 Dynamic performance of DVR under asymmetric and symmetric voltage sags

Case a: A three phase voltage dip of 30% is initiated by using a three-phase auto transformer for a duration of two seconds which can be observed from supply voltage waveforms shown in Figure 4.20. DVR mitigates the voltage sag and restores the load voltage to a constant value as shown in Figure 4.20.

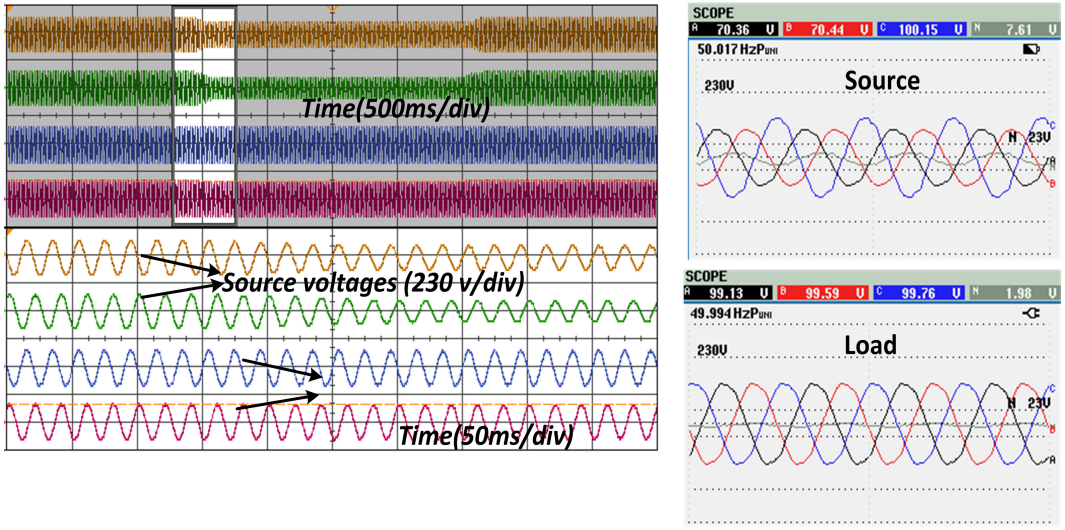
Case b: Unbalanced voltage sag is created by reducing the voltage in phase-a and phase-b by 30% as shown in Figure 4.21. DVR compensates for both negative and positive sequence voltages and maintains a constant voltage which is evident from the load voltage waveform of phase-a and phase-b as depicted in Figure 4.21

Case 2(b): The response of a DVR for a 30% dip in phase b is portrayed in Figure 4.22. The supply voltage drops to 70V in phase b as shown in Figure 4.22. The control algorithm responds immediately after the sag and injects voltage as seen in Figure 4.22 to keep the load voltage unchanged which is apparent from the load voltages depicted in Figure 4.22.



(a) (b)

Figure 4.20: Experimental results: (a)dynamic response of DVR under three phase sag (b) steady state voltage waveform of source and load



(a) (b)

Figure 4.21: Experimental results: (a)dynamic response of DVR under two phase sag (192 v/div) (b) steady state voltage waveform of source and load

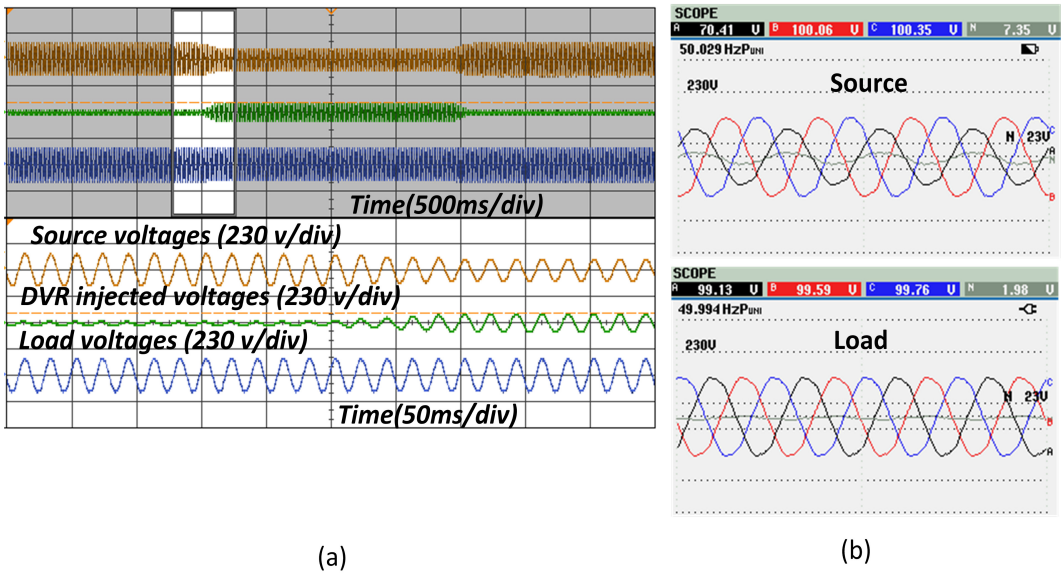


Figure 4.22: Experimental results: (a)dynamic response of DVR under single phase sag (b) steady state voltage waveform of source and load

4.6.5 Dynamic performance of DVR under asymmetric and symmetric voltage harmonics

As mentioned earlier that CDSC based DVC scheme also mitigates harmonics in load voltages. The location of laboratory where DVR prototype developed is six storeyed Information Technology (IT)/EEE building of NITK Surathkal, Mangalore. It consists of two feeders: one feeder for lighting and UPS load, the other feeder for AC loads. The experiment is carried out during peak hours as the non-linear loads viz., computers, UPS etc., which are connected in the parallel feeder are in maximum usage and sufficient to create the symmetric and asymmetric harmonics situation in the system. Under such non-linear loads, phase-a voltage contains a third harmonic of 3.8%, fifth harmonic of 6.2%, and seventh harmonic of 5.8% as shown in Figure 4.23(b). Also, a symmetrical dip of 30% is introduced in source voltages along with harmonics. CDSC pre-filter extracts the ISC accurately even under asymmetric harmonics. DVC algorithm compensates for the voltage sag and restores the fundamental of load voltage to nominal value as seen in Figure 4.23(a). The effectiveness of the CDSC extractor can be verified from the load voltage harmonics as shown in Figure 4.23(c) where it is observed that the third, fifth and seventh harmonics are restricted

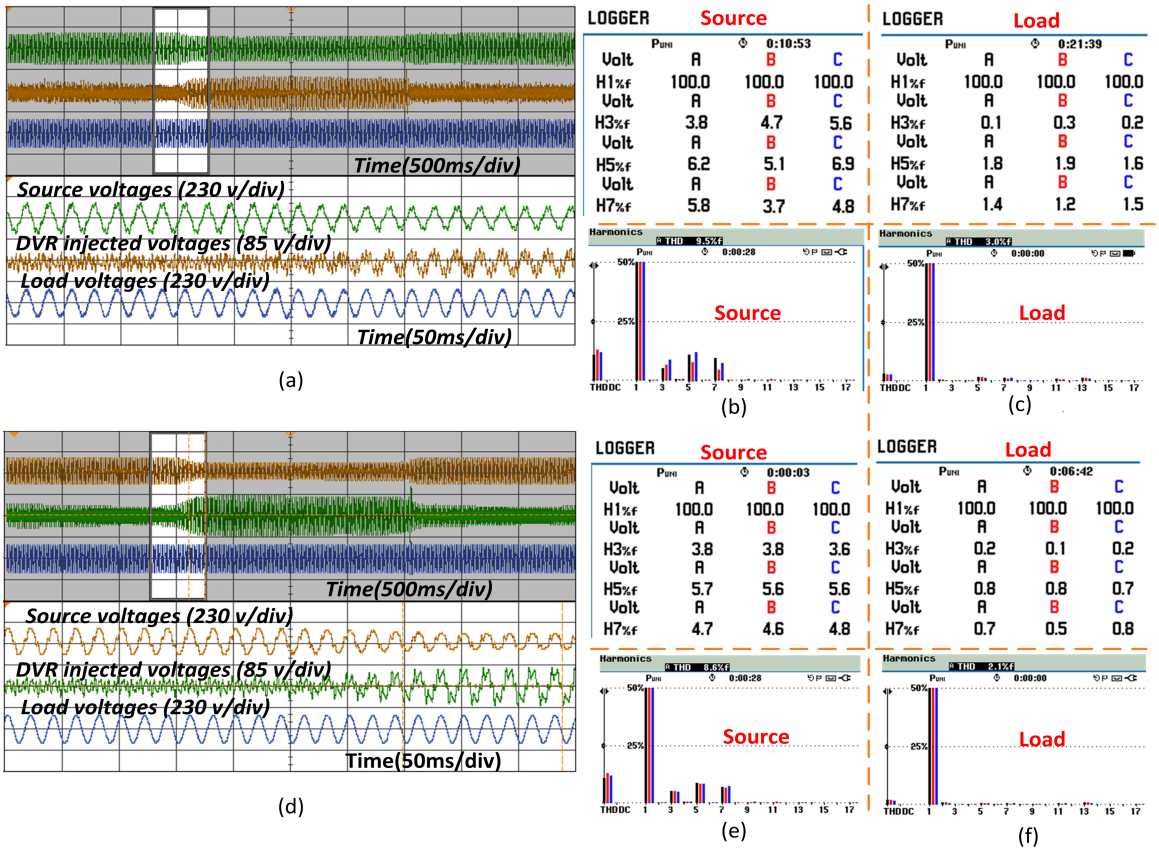


Figure 4.23: Experimental results:(a),(d) Dynamic reponse of DVR under balanced sag with asymmetric and symmetric harmonics, (b)-(c), (c)-(f) Harmonic spectrum of source and load voltages during asymmetric and symmetric harmonics respectively

to 0.1%, 1.8% and 1.4% respectively. It can be concluded from Figure 4.23(d) that the control algorithm also works effectively during symmetric harmonics case where the source voltage contains a third harmonic of 3.8%, fifth harmonic of 5.7% and seventh harmonic of 4.7%(Figure 4.23(e)). Finally, the load voltage third, fifth and seventh harmonics are restricted to 0.2%, 0.8% and 0.7% respectively as shown in Figure 4.23(f).

4.7 Conclusion

This chapter presented the flexible control strategy for the effective control of DVR. It is based on the CDSC operator which plays a dual role as a prefilter and as an

extractor. Therefore,the main contribution of this chapter is evaluation of performance of dual role CDSC-based DVC algorithm for compensating voltage sags and simultaneously mitigating the harmonics from load voltage.

- ISC of the grid voltages were obtained using a CDSC prefilter, which is customized to filter out symmetric and asymmetric voltage harmonics.
- CDSC-based DVC algorithm with positive and negative sequence controllers is implemented in the dq-frame to track the DVR reference voltages.
- The proposed control scheme is implemented in FPGA digital controller and its performance is evaluated under symmetric and asymmetric voltage sags and harmonics.
- From the experimental studies it is noticed that load voltage THD was reduced to 3.0% (from 14.1%) in asymmetric harmonic case and to 2.1% (from 17.1%) in symmetric harmonics case by adding an extractor based on the modified CDSC strategy to the control algorithm which is designed to extract the dominant lower order harmonics from the load voltage.

Based on the simulation studies and experimental results, the proposed algorithm operates effectively even when the grid voltage is distorted with variations such as balanced, unbalanced sags, and during the presence of asymmetric and symmetric voltage harmonics.

Chapter 5

Design and performance analysis of proposed PDF based voltage controller for DVR under distorted grid conditions

Contents

5.1 Introduction

In the previous chapter the DVR system is tested with DVC algorithm to compensate voltgae disturbances. In this control structure the conventional *Proportional* controller (P) is employed in the voltage control. So in the current chapter a *Pseudo Derivative Feedback* (PDF) based voltage controller is implemented for effective operation of DVR under voltage disturbances. This chapter address the issues in conventional P and PI multiloop controller with and without feedforward path then proposes PDF control strategy for DVR. Firstly the chapter discuss about multi loop conventional control schemes viz., P and PI controller. Then the efficacy of proposed controller is illustrated by comparative study with conventional P and PI controller using time response and relative stability analysis.

5.2 Evolution of proposed controller

5.2.1 Block diagram model of DVR

The dynamic characteristics of DVR pretty much depends on the filter and connected load (Vilathgamuwa et al., 2002c),(Khodabakhshian et al., 2013). To reduce the complexity in modelling of the DVR a simple LC filter is considered as shown in 5.1 (Khodabakhshian et al., 2013). To derive the state space equation of the circuit shown in Figure 5.2, per unit analysis is considered to avoid the complication involved in transforming the impedances, voltages and currents from one side of the transformer to another side. All the impedances, voltages and currents are first converted into per unit in their respective side and then transferred to inverter side. The differential state space equation for the Figure 5.2 in per unit is given by:

$$V_{inv} = V_{cf} + I_{lf} r_f + L_f \frac{di_f}{dt} \tag{5.1}$$

$$V_{dvr} = V_{cf} + I_t r_t + L_f \frac{di_t}{dt} \tag{5.2}$$

$$I_{C_f} = C_f \frac{dV_{C_f}}{dt} \tag{5.3}$$

$$I_{C_f} = C_f \frac{dV_{C_f}}{dt} \tag{5.4}$$

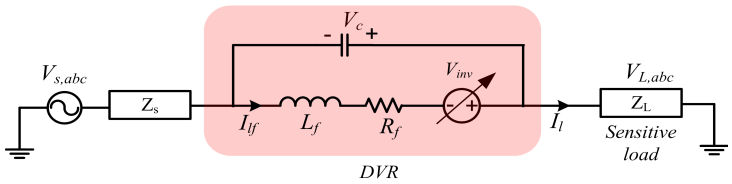


Figure 5.1: Equivalent circuit (time domain) model of DVR

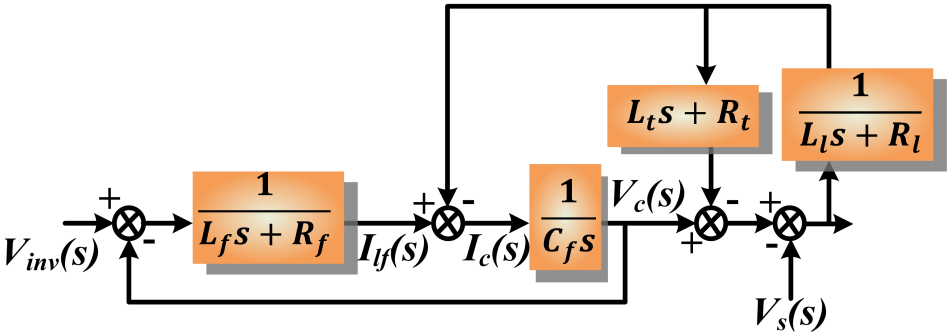


Figure 5.2: Block diagram representation of basic model of DVR

$$V_l = V_s + V_{dvr} \tag{5.5}$$

$$I_{l_f} = I_t + I_{C_f} \tag{5.6}$$

$$I_l = I_s = I_t \tag{5.7}$$

Using the above (5.2) to (5.7) the basic DVR can be modelled as shown in Figure 5.2.

5.2.2 Proposed voltage controller

A generalized PDF (Wang et al., 2016), (Ohm, 1994), (Phipps et al., 2006) control system comprises two parts an integral term(k_1/s) in forward path and proportional term (K_2) in feedback path. In this scheme, the proportional term acts on output directly and the integral term acts on the difference of reference and output voltage (i.e. error signal). The basic control equation of PDF controller is expressed as

$$u_s^* = \frac{k_1}{s} * e(s) - \frac{k_2}{s} * y(s) \tag{5.8}$$

The block diagram of proposed PDF voltage feedback control scheme with DVR model is illustrated in Figure 5.3. The load voltage for this configuration is given by

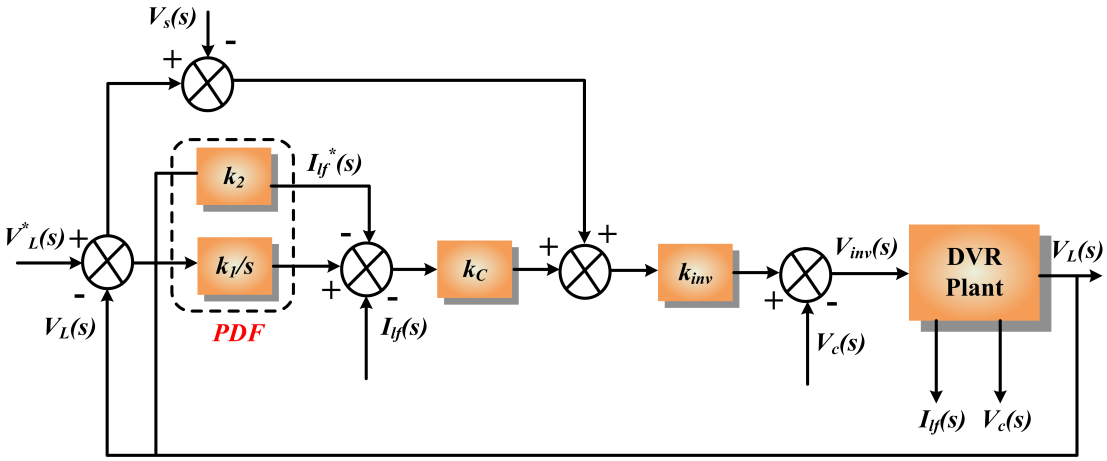


Figure 5.3: Block diagram representation of multiloop feedforward controller with PDF controller

$$v_1(s) = G_{a1}(s)v_l^*(s) + G_{b1}(s)v_s(s) \tag{5.9}$$

where $G_{a1}(s)$ and $G_{b1}(s)$ are the transfer functions with respect to reference load voltage and source voltage respectively and is given by:

$$G_{a1}(s) = \frac{v_l(s)}{v_l^*(s)}|v_s = 0 \tag{5.10}$$

and

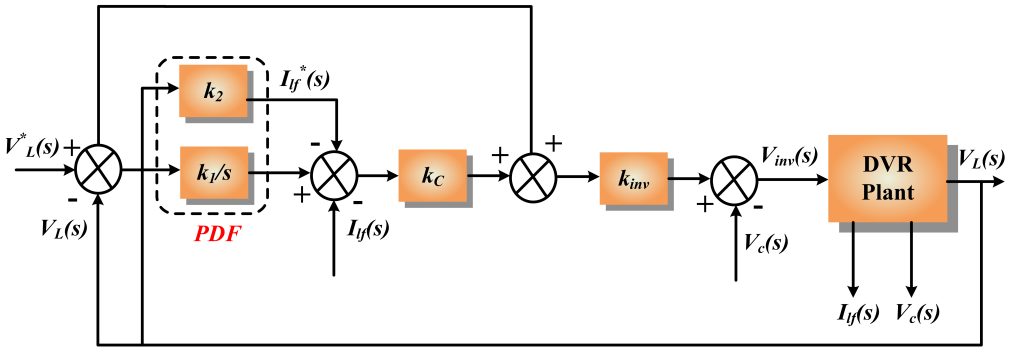
$$G_{b1}(s) = \frac{v_l(s)}{v_s(s)}|v_l^*(s) = 0 \tag{5.11}$$

using Figure 5.3(a) $G_{a1}(s)$ is given by

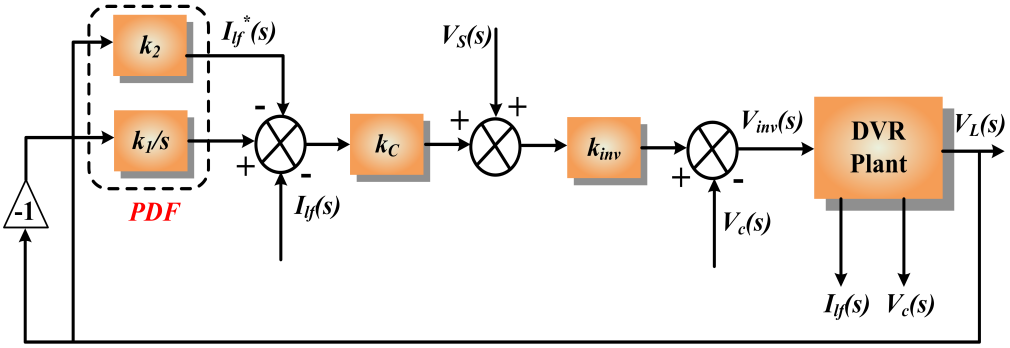
$$G_{a1} = \frac{\frac{K_1}{s}k_c k_{inv}G_1G_2 + k_{inv}G_1G_2}{D_n} \tag{5.12}$$

where

$$D_n = 1 + \frac{K_1}{s}k_c k_{inv}G_1G_2 + K_2k_c k_{inv}G_1G_2 + k_c k_{inv}G_1 + G_1G_2 + G_2G_2 + G_3G_4 + k_c k_{inv}G_1G_2G_3 + k_c k_{inv}G_1G_3G_4 \tag{5.13}$$



(a)



(b)

Figure 5.4: Block diagram for calculation of (a) $G_{a1}(s)$ (b) $G_{b1}(s)$

$$G_1 = \frac{1}{L_f s + r_f}; \quad G_2 = \frac{1}{C_f s}; \quad G_3 = \frac{L_t s + r_t}{L_l s + r_l} \quad and \quad G_4 = \frac{1}{L_l s + r_l} \tag{5.14}$$

substituting the value of G_1, G_2, G_3, G_4 in G_{a1} then

$$G_{a1} = \frac{n_{a12}s^2 + n_{a11}s + n_{a10}}{d_{a14}s^4 + d_{a13}s^3 + d_{a12}s^2 + d_{a11}s + d_{a10}} \tag{5.15}$$

where $n_{a12} = k_{inv}L_l$; $n_{a11} = k_1k_ck_{inv}L_l$; $n_{a10} = k_1k_ck_{inv}r_l$; $d_{a14} = C_fL_f(L_l + L_t)$;

$d_{a13} = C_f(L_fr_l + L_lr_f) + k_ck_{inv}C_f(L_l + L_t) + C_f(L_tr_f + L_fr_t;)$

$d_{a12} = C_fr_f(r_l + r_t) + k_ck_{inv}C_f(r_l + r_t) + k_2k_ck_{inv}L_l + L_l + L_f;$

$d_{a11} = k_2k_ck_{inv}r_l + k_1k_ck_{inv}L_l + k_ck_{inv} + r_l + r_f; \quad d_{a10} = k_1k_ck_{inv}r_l;$

similarly from Figure 5.3(b) the G_{b1} is given by

$$G_{b1} = \frac{1 + k_ck_{inv}G_1 + G_1G_2 - k_{inv}G_1G_2}{D_n} \tag{5.16}$$

substituting the value of G_1, G_2, G_3 and G_4 from (5.15) in (5.16)

$$G_{a1} = \frac{n_{b14}s^4 + n_{b13}s^3 + n_{b12}s^2 + n_{b11}s + n_{b10}}{d_{b14}s^4 + d_{b13}s^3 + d_{b12}s^2 + d_{b11}s + d_{b10}} \tag{5.17}$$

where
$n_{b14} = C_f L_f L_l$; $n_{b13} = C_f(L_l r_f + L_f r_l) + k_c k_{inv} C_f L_l$; $n_{b12} = k_c k_{inv} C_f r_l + C_f r_l r_f + L_l - k_{inv} L_l$; $n_{b11} = (1 - k_{inv}) r_l$ *and* $n_{b10} = 0$; The value of d_{b10}, d_{b11}, d_{b12}, d_{b13} and d_{b14} is same as d_{a10}, d_{a11}, d_{a12}, d_{a13} and d_{a14} respectively.

5.2.3 Existing Controller Schemes

In this section four basic multiloop control structure with and without feedforward path for DVR control is considered as shown in Figure 5.4 to show the effectiveness of proposed control scheme. The closed loop transfer function of controllers shown in Figure 5.4 are tabulated in Table.5.1

It is essential for the DVR that load voltage should track its reference value (V_1^*) and should be unaffected by the change in the source voltage (V_s). By comparing the transfer function of controllers (Table.5.1) it can be easily observed that addition of the feedforward path to the controller adds the term $k_{inv}(L_l s + r_l)$ and $k_{inv} s(L_l s + r_l)$ in the numerator of transfer function with respect to the reference value in P and PI controller. Furthermore, it reduces the terms $k_{inv}(L_l s + r_l)$ and $k_{inv} s(L_l s + r_l)$ in the numerator of transfer function with respect to the source voltage in P and PI controller, which means that it upsurges the DVR capability to track its reference value and downturn the effect of source voltage. Also, it can be observed from the transfer function that it does not change the characteristics equation of the controller; hence it does not affect the stability of the system. Thereby it signifies that the multiloop controller with feedforward path is better than multiloop controller without feedforward path. Therefore, in the current thesis the analysis of proposed controller(PDF), P and PI voltage controller is carried out by considering the feedforward path in the control structure.

*The co-efficients in the Table.5.1 are given at the end of this chapter.

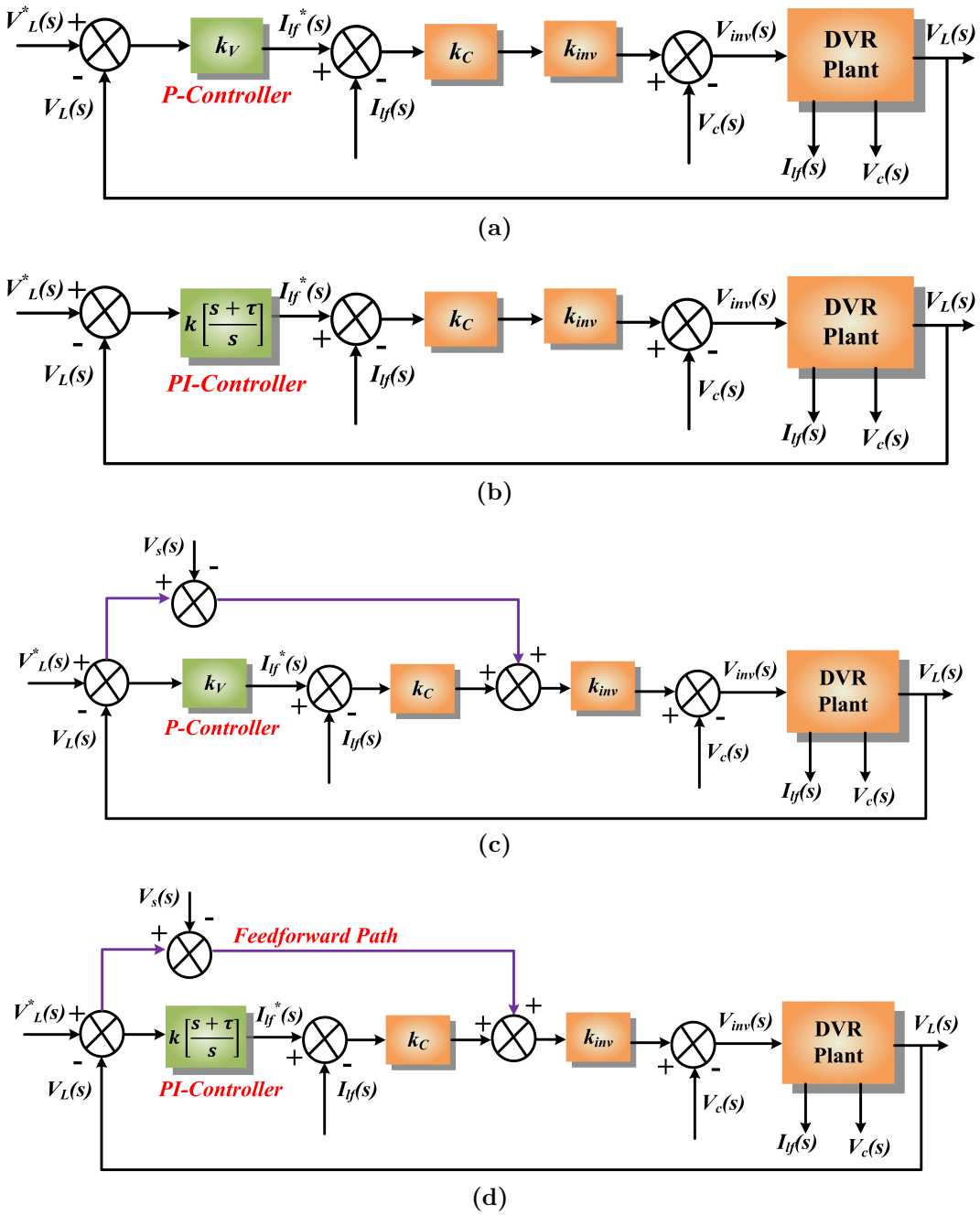


Figure 5.5: Block diagram representation of (a) multiloop controller with P controller(b) multiloop controller with PI controller (c)multiloop feedforward controller with P controller (d) multiloop feedforward controller with PI controller

Table 5.1: Closed loop transfer functions of existing controllers

Voltage/ Current Controller	Feed forward path	With respect to reference load voltage	With respect to source voltage
P/P	No	$G_{a2} = \frac{n_{a21}s+n_{a20}}{d_{a13}s^3+d_{a12}s^2+d_{a11}s+d_{a10}}$	$G_{b2} = \frac{n_{b23}s^3+n_{b22}s^2+n_{b21}s+n_{b20}}{d_{b23}s^3+d_{b22}s^2+d_{b21}s+d_{b20}}$
PI/P	No	$G_{a3} = \frac{n_{a32}s^2+n_{a31}s+n_{a30}}{d_{a34}s^4+d_{a33}s^3+d_{a32}s^2+d_{a31}s+d_{a30}}$	$G_{b3} = \frac{n_{b34}s^4+n_{b33}s^3+n_{b32}s^2+n_{b31}s+n_{b30}}{d_{b34}s^4+d_{b33}s^3+d_{b32}s^2+d_{b31}s+d_{b30}}$
P/P	Yes	$G_{a4} = \frac{n_{a41}s+n_{a40}}{d_{a43}s^3+d_{a32}s^2+d_{a41}s+d_{a40}}$	$G_{b4} = \frac{n_{b43}s^3+n_{b42}s^2+n_{b41}s+n_{b40}}{d_{b43}s^3+d_{b42}s^2+d_{b41}s+d_{b40}}$
PI/P	Yes	$G_{a3} = \frac{n_{a52}s^2+n_{a51}s+n_{a50}}{d_{a54}s^4+d_{a53}s^3+d_{a52}s^2+d_{a51}s+d_{a50}}$	$G_{b5} = \frac{n_{b54}s^4+n_{b53}s^3+n_{b52}s^2+n_{b51}s+n_{b50}}{d_{b54}s^4+d_{b53}s^3+d_{b52}s^2+d_{b51}s+d_{b50}}$

5.3 Parameter Tuning and Comparative Analysis

5.3.1 Parameter tuning

The objective of this section is to find the gain parameters of P, PI and PDF controllers for achieving the faster-dynamic response and enhancing the relative stability of DVR. Generally, root locus method is used to design the parameters of controller. The conventional root locus method (Kwon and Chang, 2016a) is a single parameter design method i.e. it cannot track the optimal value of multiple controller parameters (such as K_v, K_c and ζ in PI controller) simultaneously. So, an extended Root Locus Design (RLD) (Kwon and Chang, 2016b) method is adopted to tune the controller parameters. Figure 5.5 shows the extended RLD for tuning the parameters of PDF controller. To tune the value of K_c, the root locus for K_c is drawn for each value of K_1 and K_2 varied stepwise from its minimum stable value to maximum stable value obtained by Routh Hurwitz(RH) Stability Criterion as shown in Figure 5.5(a). Based on maximum relative stability the optimal value of K_c is obtained. Similarly, for tuning K_2, the root locus of K_2 is plotted for the obtained value of K_c and each value of K_1 is varied stepwise within its stable range as shown in Figure 5.5(b). Based on maximum relative stability the optimal value of K_2 is obtained.

From the obtained values of K_c (Figure 5.5(a)) and K_2 (Figure 5.5(b)) the root locus is plotted for transfer function having gain K_1 as shown in Figure 5.5(c) and its value is calculated based on relative stability. The above procedure which is used for tuning theparameter of PDF is followed for P and PI controller and their respective extended-RLD is shown in Figure 5.5(d)-(h).

Table.5.2 showcase the tuned gains of the controller along with their relative sta-

bility. It indicates that the relative stability of PDF is much larger than P and PI controller. The preceding subsection discuss the performance analysis of controller in terms of overshoot and settling time. Thus, controller gains obtained in this subsection are utilized for the time response analysis.

5.3.2 Time response analysis

To study the dynamic performance of DVR with P, PI and PDF controllers the considered system is implemented in dq-frame. The supply voltage (V_s) is subjected to 50% sag (extreme case) and the voltage response is plotted as shown in Figure 5.6

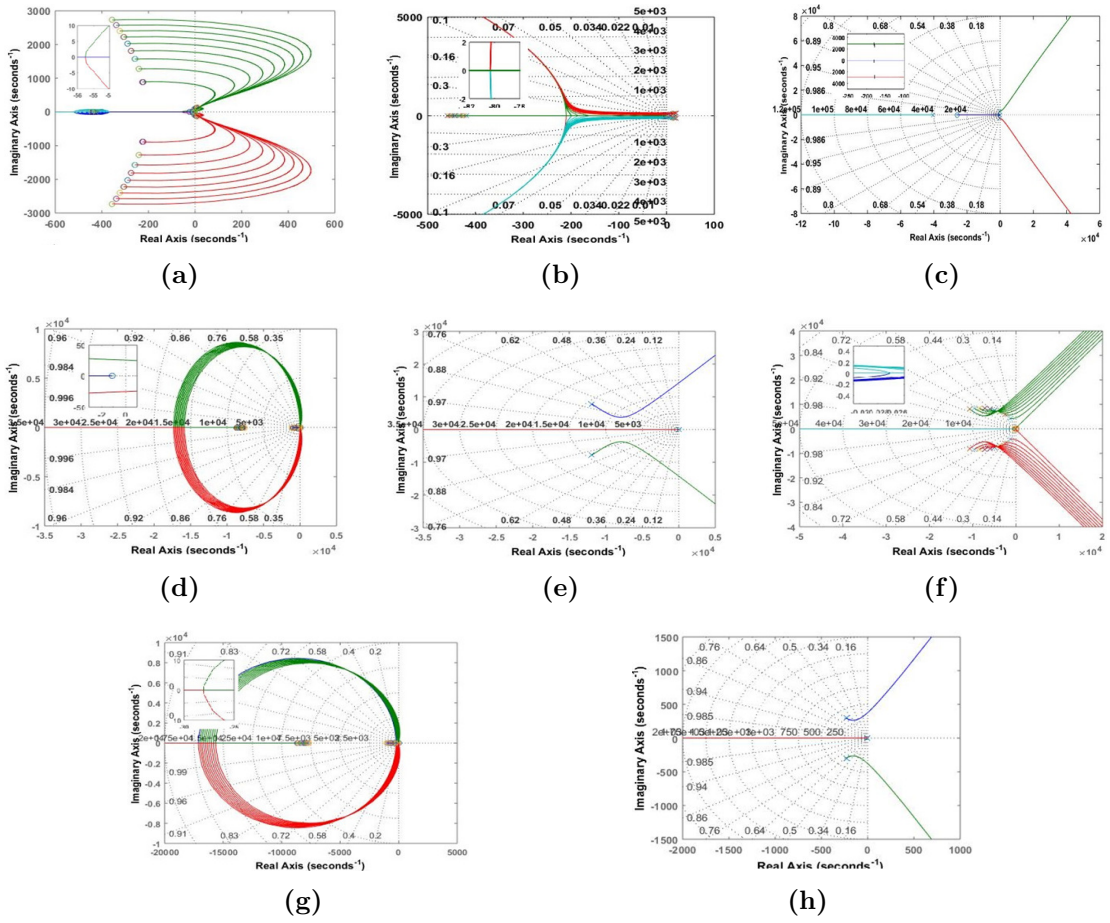


Figure 5.6: Root loci for PDF, P and PI controller parameter tuning (a) Calculation of K_c for PDF controller (b)Calculation of K_2 for PDF controller (c) Calculation of K_1 for PDF controller (d) Calculation of K_c for P controller (e) Calculation of K_v for P controller (f) Calculation of τ for PI controller (g) Calculation of K_c for PI controller (h) Calculation of K_v for PI controller

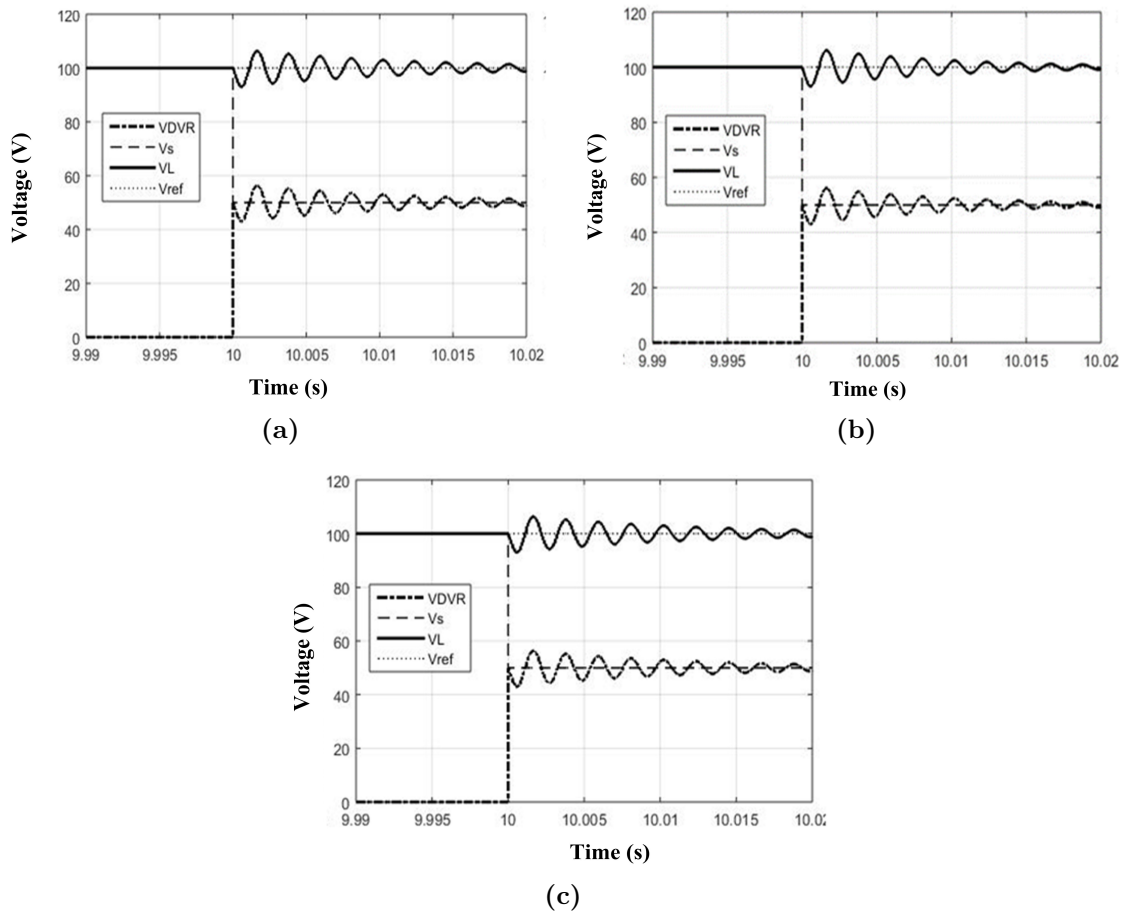
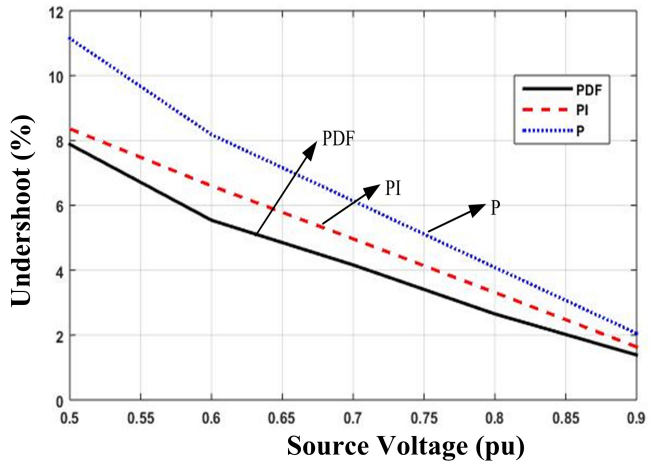


Figure 5.7: Voltage response of controller with feedforward path on 50% sag(a) P controller (b) PI controller (c) PDF controller

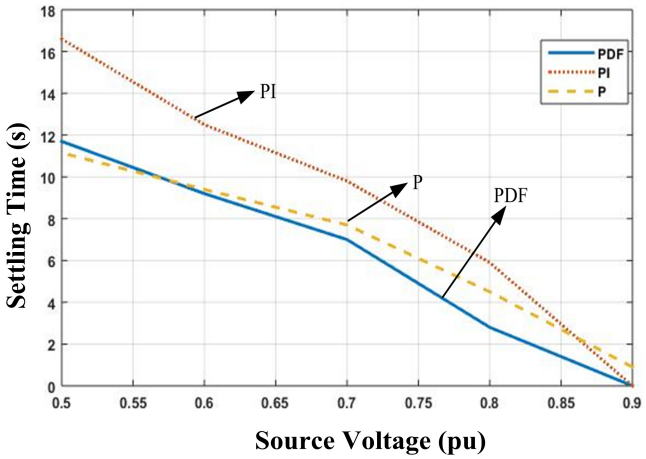
Table 5.2: Stability analysis of controller

Parameters	**PDF controller with FF path**	**PI controller with FF path**	**P controller with FF path**
Gains	k_c, k_v and k_f	k_c, k_v and τ	
Relative Stability	2.97	3.5	$2e^{-05}$
Damping Factor	1	1	1

by assuming PLL as an ideal one (i.e. there is no delay involved in tracking the phase angle) and assuming PLL pre-filter is perfect (i.e. *dq* voltages are perfect DC). From Figure 5.6, it can be observed that the instant when the sag is created DVR injects and tries to compensate the load voltage, but the DVR and load voltage is subjected to some oscillation before settling down to its final value. The maximum deviation from its final value and the time taken by the load voltage to settle within its final value depends on the type of controller used. In case of P and PI controller the maximum deviation of load voltage from its reference value is 11.15% and 8.36%



(a)



(b)

Figure 5.8: Time Response of System with Source Voltage Variation: (a) Undershoot (b) Settling Time

respectively. For PDF controller, the maximum deviation is around 7.88% which is less than that of P and PI controller as summarized in Table.5.3. It can be easily seen that though the P controller has better settling time, but its stability margin is very less (Table.5.2) and some slight variation in the system parameters may leads to its instability. PI controller has better relative stability, but its sluggish dynamic response increases the overall response time of DVR and thereby degrades its performance. The proposed controller has better dynamic response as compared to PI with decent relative stability. Further, its undershoot in load voltage is less as compared to both P and PI controllers.

Table 5.3: Time Response of P, PI and PDF controller with FF path for Voltage Sags

Supply Voltage (pu)	Undershoot(%)			Settling Time(ms)		
	PDF	PI	P	PDF	PI	P
0.9	1.385	1.635	2.05	0	0	0.9
0.8	2.65	3.31	4.085	2.8	5.9	4.5
0.7	4.161	4.965	6.137	7	9.8	7.7
0.6	5.54	6.6	8.18	9.2	12.5	9.4
0.5	7.88	8.36	11.15	11.7	16.6	11.15

5.4 Simulation results of Proposed PDF based voltage control of DVR under different voltage disturbances

A 10 kV medium voltage DVR is modeled in PSCAD/EMTDC to carryout simulation studies. Dual role CDSC based DVC algorithm with PDF voltage controller is implemented for DVR control. The simulation parameters are same as considered in the previous chapter (Table.4.3) and the proposed control algorithm is tested for different test conditions viz., symmetric and asymmetric voltage sags and harmonics. These test cases are chosen as they are frequently occurring momentary voltage disturbances. Firstly, the simulation results of comparative analysis of load dq voltages between proposed PDF voltage controller and existing (P and PI) controllers are presented. Further based on the comparative results PDF voltage controller is adopted.

To prove the robustness of the PDF controller a real-time simulation of 10 kV, 1MVA medium voltage DVR is implemented using PSCAD in this section. Figure 5.8 shows dq load voltage response (V_s source voltage, V_l load voltage) of PDF, PI and P controllers for symmetric and asymmetric voltage sags.The later part of subsection explains the performance of PDF controller subjected to symmetric and asymmetric sags further the detailed readings of comparative analysis are tabulated in Table.5.4.

Firstly, balanced three-phase symmetric sag is generated by initiating the three-phase symmetric fault at t=0.1s. The grid voltage drops to 70% of its nominal value as seen in Figure 5.8. The proposed control scheme is able to restore the load voltage to prefault value within 17.5ms which is shown in Figure 5.8(a). In second scenario (Figure 5.8(b)) a two-phase fault is created at t=0.9s. It results a voltage drop of 30% of its nominal value in

phase-b and phase-c creating an unbalanced sag situation. It can be clearly observed that though there is unbalance sag in source voltage and the proposed DVR control scheme maintains the load voltage to its nominal value within 12.5 ms as shown in Figure 5.8(b). Figure 5.8(c) depicts the third scenario where DVR control scheme is tested for single-phase sag in phase-b at t=1.3s. The grid voltage of phase-b drops to 70% of its nominal value and the proposed control scheme for DVR maintains the load voltage constant within 12.7 ms. The summary of the above analysis is the PDF controller posses undershoot of 17.39% and settling time of 17.5 ms during symmetric sag. On the other hand during asymmetric sag (single phase) the undershoot and settling time for PDF controller are 3.52% and 12.7 ms respectively. From the zoomed view it can be observed that the PDF controller has smooth response compared to P and PI. From the Figure 5.8 it is observed that transients in the load voltage i.e., the delay time occurred in v_{ld} waveform when the fault is initiated is due to PLL dynamics which are considered in the real-time system. The study of interest in the present analysis is time response of respective controller when subjected to symmetric and asymmetric voltage sags. Thus encircled portion in the Figure 5.8 is considered as it gives good insight of controller response for further comparative analysis. Table.5.4 provides the performance analysis of PDF,PI and P controllers for symmetric and asymmetric sags by using PSCAD simulations. It is observed that the undershoot of PDF controller is less compared to other controllers but on the other hand the settling time of PDF is slightly less than the P controller. However, the relative stability margin of PDF is more compared to PI controller.

Table 5.4: PSCAD simulation results for P, PI and PDF controller with FF path for symmetric and asymmetric voltage sags

Controllers	**Balanced sag**		**Two phase sag**		**Single phase sag**	
	Under-shoot(%)	**Settling time(ms)**	**Under-shoot(%)**	**Settling time(ms)**	**Under-shoot(%)**	**Settling time(ms)**
P	19.9	15	11.37	12	7.2	13
PI	19.7	20	11.145	12	7.45	13.37
PDF	17.39	17.5	9.046	12.5	3.52	12.7

5.5 Experimental Results

A 100V, 0.5kVA scaled down low voltage DVR prototype is developed in laboratory to conduct experimental studies. Hardware configuration of the DVR prototype con-

sists of a voltage source, Voltage Source Inverter (VSI) and a resistive load. The inductance of the transformer and a capacitor connected at its secondary acts as LC-filter to eliminate the higher frequency harmonics generated by the VSI. PDF voltage controller based multiloop with feedforward path control algorithm is implemented in Altera cyclone-II FPGA controller using Quartus GUI. The experimental studies are conducted for balanced and unbalanced voltage sags and the results are presented. Figure 5.10 portrays the dynamic response (dq) of source voltages for symmetric and asymmetric voltage sag (three phase and two phase). In Figure 5.11 three phase auto transformer is employed to create symmetric voltage sag which lasts for two seconds. The DVR starts injecting the voltage during corresponding voltage sag events and maintains constant load voltage(dq) as shown in Figure 5.11(a),(b). From the experimental studies it is observed that the P & PI controller-based system, during 30 % sag condition posses an undershoot of 21% &17 % in the load voltage during sag initiation. Whereas PDF controller system posses an undershoot of 12.7 %. Similarly, Figure 5.12 shows the load voltage(dq) response of P, PI and PDF controller-based system for two phase sag. Three single phase auto transformers are emplyed to create asymmetric voltage sag (two phase sag) for duration of two seconds. It is observed that P & PI based controller system exhibits an overshoot of 14.8% & 12% respectively. On the other hand, PDF controller-based system posses an undershoot of 10.6%. For all the above cases the P and PI controller-based system significantly performs low compared to PDF controller.

5.6 Conclusion

This chapter discuss about the design and development of proposed PDF based voltage control of DVR under distorted grid conditions.

- A comparative analysis of performance parameters are carried out between PDF and existing controllers (P and PI) through simulation studies.
- P controller has slightly similar time response as proposed controller. However, the stability margin of the P controller is very less thereby any small variation on the parameter leads to the instability of the system.
- The relative stability of PI controller is better compared to P controller but its

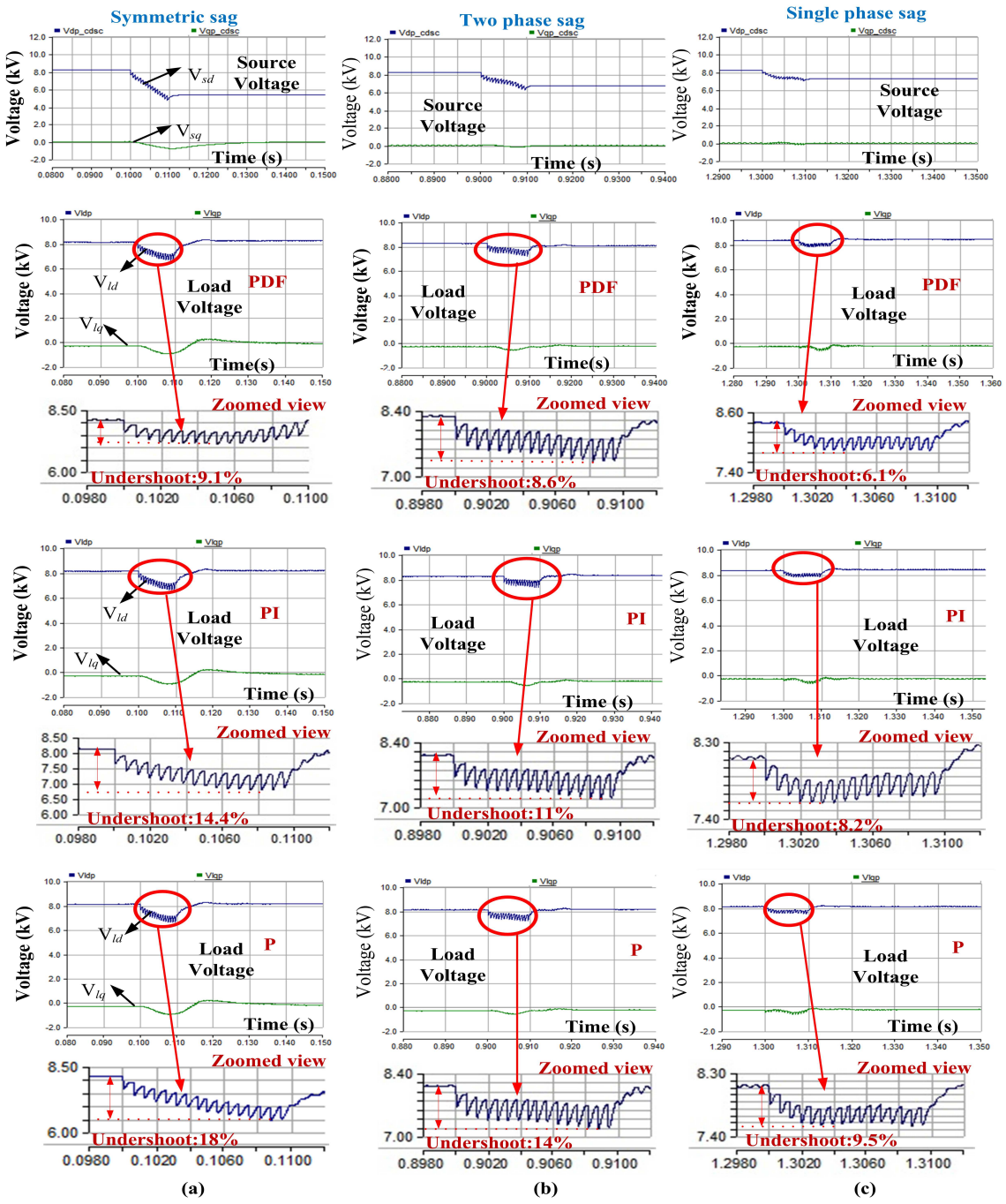


Figure 5.9: *dq* voltages response of source and load voltages of PDF, PI and P controller-based DVR system for different types of sags: (a) Three phase sag (b) Two phase sag and (c) Single phase sag

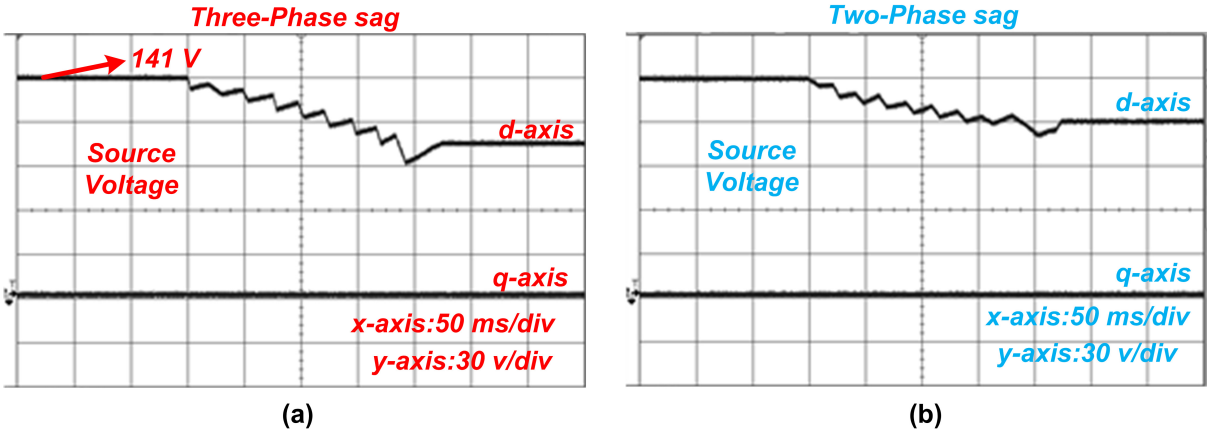


Figure 5.10: Source dq voltages under symmetric and asymmetric (two phase) sag

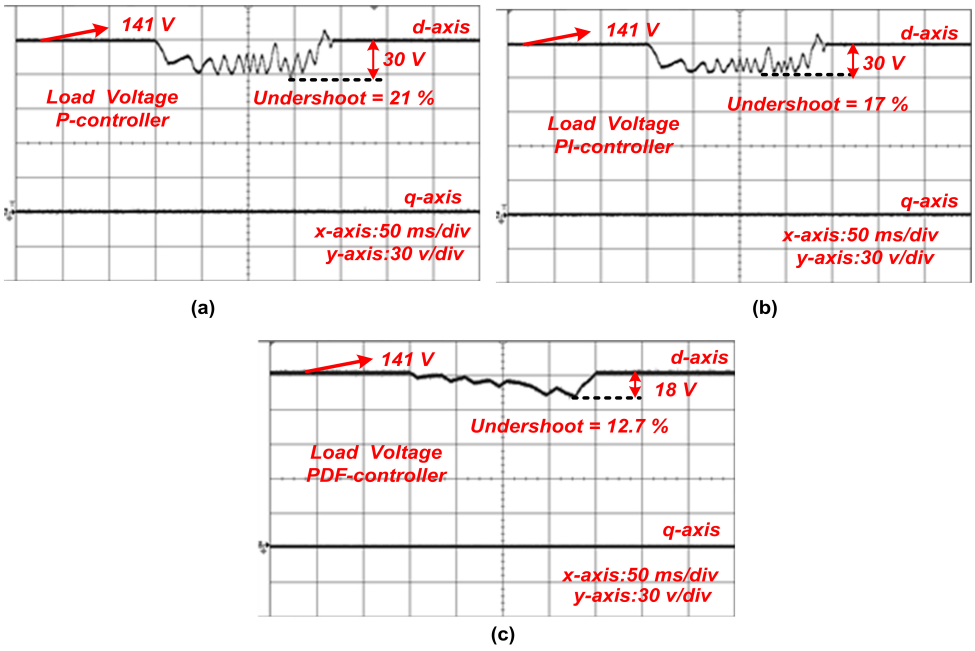


Figure 5.11: load dq voltages of P, PI, PDF controllers under three phase sag

sluggish dynamic response increases the overall settling time and undershoot in load voltage and thereby degrades its performance.

- The proposed controller has better dynamic response as compared to PI with decent relative stability.

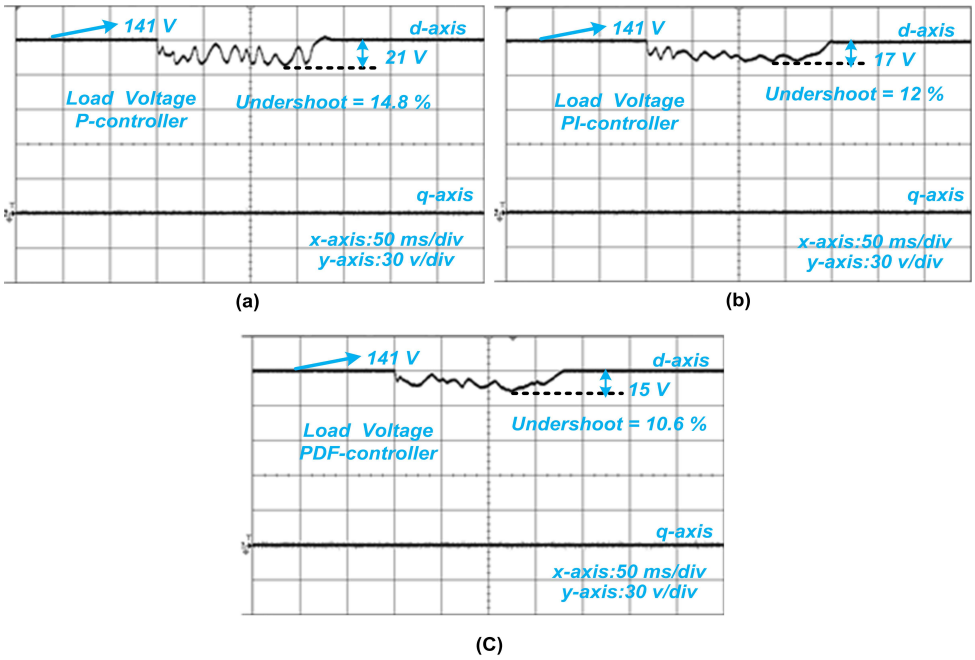


Figure 5.12: load dq voltages P, PI, PDF controllers under two phase sag

- The efficacy of proposed controller is verified by adopting MV-DVR system through simulations (PSCAD) and experimental studies on low voltage laboratory prototype DVR.
- It is observed that during symmetrical asymmetrical voltage sags the proposed PDF based voltage control of DVR exhibits a less undershoot of 12.7% & 10.6 % respectively.

Chapter 6

Design of control algorithm for operating DVR as FCL and TDVR

Contents

6.1 Introduction

In this chapter two aspects of DVR operation is discussed. Firstly the design of control algorithm for operating DVR as Fault Current Limiter (FCL) is discussed and followed by the design of control algorithm for operating DVR without transformer i.e., Transformerless DVR (TDVR). The chapter is organised as follows: firstly the flux charge based FCL is presented then followed by the design of proposed Virtual Impedance (VI) based FCL is presented. Later section deals with discussion of simulation results of the VI based FCL operation of DVR. In the second half of the chapter the description of TDVR system is presented. Then the design of Uncertainity and Disturbance Estimator based control of DVR is presented. Finally the discussion of simulation and experimental results of UDE based TDVR system is presented.

6.2 Flux Charge based fault current limiter

Large fault currents will flow through the DVR during a downstream fault before the opening of a circuit breaker. This large fault current will cause PCC voltage drop, which would affect the MV or LV loads on the other feeders connected to PCC. Furthermore, if not controlled properly, DVR might also contribute to the PCC voltage sag in the process of compensating the missing voltage, thus further worsening the fault situation. Thus in this section Flux-charge-model (Li et al., 2007e) feedback algorithm is implemented for controlling the DVR so that it would act as a large virtual inductance in series with the distribution feeder. A fault detection unit is first implemented by measuring the grid side line current (for over-current detection) and load voltage (fault recovery detection). The fault detection unit functions to bring the DVR into active mode when an over-current is sensed and turn the DVR into passive mode after detection of a fault recovery. Upon the occurrence of a downstream fault, the DVR is controlled as a virtual inductor in series with the distribution feeder

to limit the fault current and restore the PCC voltage. Flux-charge-model control consists of two loops mainly an outer flux-model and an inner charge-model loop as shown in Figure 6.1. The control variable used for the outer flux-model is the inverter filtered terminal flux.

Limitations The pure integration of measured voltage may cause saturation of the virtual flux because of the potential DC offset. To demonstrate this phenomenon the flux-charge based FCL is implemented in PSCAD and the respective results are shown in Figure 6.2. It can be observed that from Figure 6.2(a) the pure integration of flux ($\phi = \int v_{DVR}.dt$) during the period of three phase fault is approximately in saturated condition as the rate of integration is very less. Moreover from Figure 6.2(b) it can be observed that the patterns of DVR injected voltages are highly distorted due to the saturation phenomenon of flux variable. Thus, to avoid this problem, a virtual impedance based fault current limiter is proposed for DVR to protect the PCC voltages during the downstream faults.

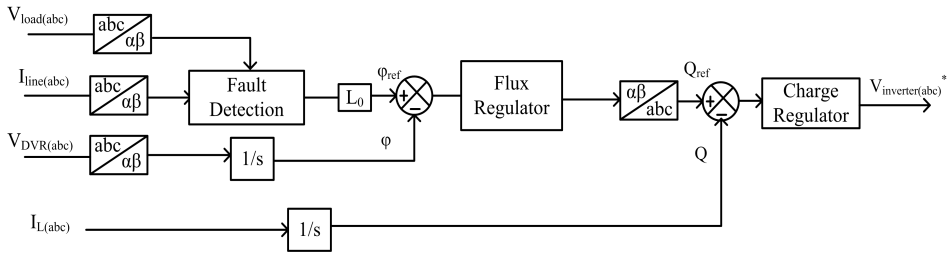


Figure 6.1: Control block diagram of flux-charge based control algorithm

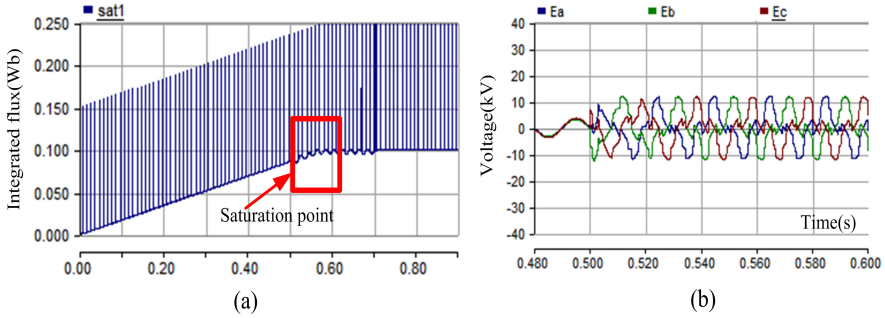


Figure 6.2: Limitations of flux-charge based FCL control algorithm (a) Saturation of flux, (b) DVR injected voltages

6.3 Design of virtual impedance parameter(Z_v)

In this subsection the design of virtual impedance parameter (Z_v) is calculated using the general constraints of transmission line characteristics (Lu et al., 2018), (Wang et al., 2015), (He and Li, 2011). A set of constraint equations are formed and iterated by using the MATLAB to fetch the optimum value of Z_v. The procedure is as follows: Let Z_1 and Z_v represent the vectors of line impedance and virtual impedance which can be written as

$$Z_1 = |Z_1| \angle \theta_1 \tag{6.1}$$

and

$$Z_v = |Z_v| \angle \theta_v \tag{6.2}$$

The DVR will act as virtual impedance to the system during downstream fault and moreover the total impedance of the system i.e, Z_{eq} (Z_1+Z_v) should not change its characteristics by addition of this virtual impedance. Thus the designed Z_v should be such that even after addition the Z_{eq} should be inductive in nature. Using this condition the constraint (6.3) is formed which is used to design the Z_v value. The phasor diagram in Figure 6.3 is used for the further analysis.

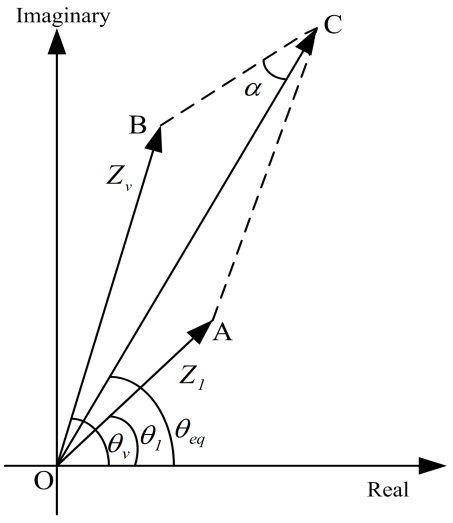


Figure 6.3: Phasor diagram of the impedances $|Z_1|$ and $|Z_v|$

$$90^0 - \theta_{eq} \leq \theta_{eqm} \tag{6.3}$$

In (6.3) the θ_{eqm} is the maximum acceptable phase difference, which is considered to be 2^0 (Lu et al., 2018) here as to maintain the inductive characteristics of transmission line. From Figure 6.3 by using the cosine law in the triangle $\triangle OBC$, it is derived that:

$$|Z_{eq}| = \sqrt{\left(|Z_1|^2 + |Z_v|^2 - 2\,|Z_1|\,|Z_v|\,cos(90^0 - \theta_v + \theta_1)\right)} \tag{6.4}$$

Meanwhile, by using the sine law in the same triangle, it yields that:

$$\alpha = arcsin\left[\frac{|Z_v|}{|Z_{eq}|} sin(\theta_v - \theta_1)\right] \tag{6.5}$$

where $\alpha = \angle COB$

$$\theta_{eq} = \alpha + \theta_1 \tag{6.6}$$

For a given system, $|Z_1|$ and θ_1 commonly vary within a certain range that is determined by the practical condition of the transmission line. The selection of $|Z_v|$ and θ_v should make sure that for arbitrary $|Z_1|$ and θ_1 within their ranges, the equivalent line impedance $|Z_{eq}|$ should be significantly inductive, i.e., the criteria established by combining (6.3)- (6.6) should be satisfied. In the given system, assuming that $|Z_1|$ varies within the range of $0.5 \quad \Omega \quad to \quad 1 \quad \Omega$ and θ_1 varies within the range of 80^0 to 87^0 (Lu et al., 2018). By using MATLAB the above equations are coded in m-script to search the suitable $|Z_v|$ and θ_v and it can be reached that

$$|Z_v| = 1.40 \quad \Omega \quad and \quad \theta_v = 89^0 \tag{6.7}$$

From the above obtained value of Z_v the respective R_v and L_v values are obtained as $R_v = 24m\Omega, L_v = 0.00139mH (Z_v = R_v + jX_v)$.

6.4 Proposed Virtual Impedance based Downstream Fault Current Limiting (DFCL) control algorithm for DVR

A virtual impedance (VI) based DFCL is proposed to suppress the fault current during downstream fault conditions. Since three-phase faults have the highest impact on system operation, the proposed method is mainly designed for alleviating the

influence of symmetrical three-phase faults. Compared to the existing methods of implementing DFCL control algorithms, the VI-DFCL features lower capital and maintenance costs. No extra superconducting devices or extra inverters are required to limit the fault current. Meanwhile, virtual impedance can be also used as damping impedance at different harmonic frequencies so that the certain harmonic components can be eliminated which is an additional feature.

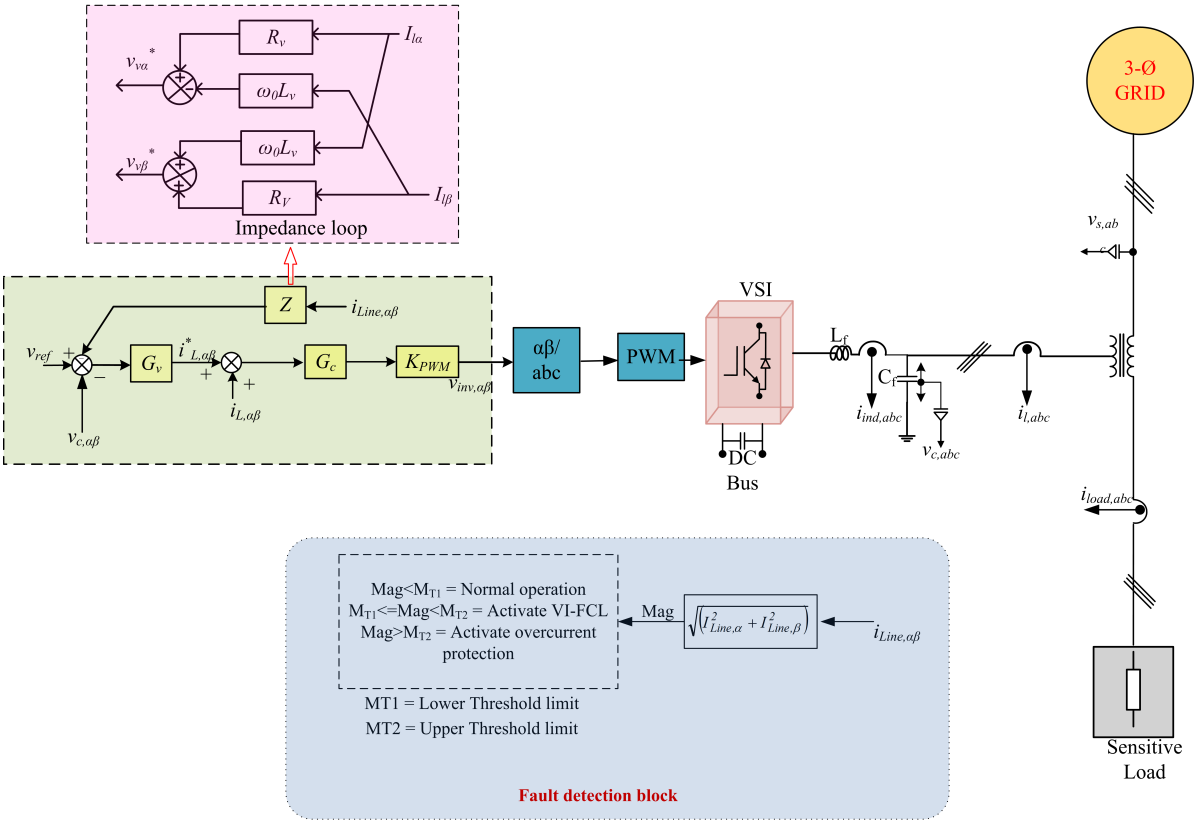


Figure 6.4: Control block diagram of virtual impedance implementation

As shown in the Figure 6.4 when the load current surpasses threshold limit the virtual impedance block gets activated. A multiloop control scheme is adopted where the outer loop uses a P+Resonant (PR) controller for voltage control and for inner current loop a proportional controller is employed. From the block diagram the following equations are derived

$$V(s) = G(s).V_{ref}(s) - Z_{out}(s).I(s) \tag{6.8}$$

$$Z_{out}(s) = \frac{N(s)(1 + k_{ind}M(s))}{1 + M(s)N(s) + k_{ind}H_v(s)M(s)N(s) + k_{ind}M(s)} \tag{6.9}$$

where $M(s) = 1/(L_f s + R_f), \quad N(s) = 1/C_f(s)$ The proportional-resonant controller (PR) controllers used in the inner voltage control loop is given as

$$G_v(s) = k_{pv} + \frac{k_v s}{s^2 + \omega^2} \tag{6.10}$$

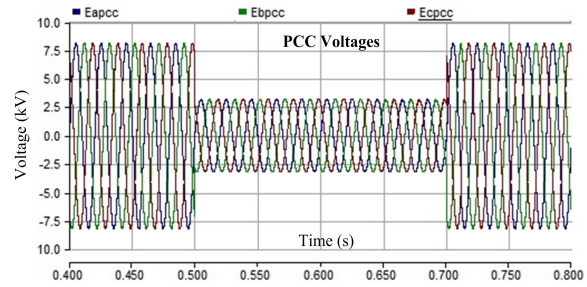
where k_{pv} is the proportional gain and k_f is the gain at the selected harmonic frequency, ω (in rad/s), is the cut off frequency of the resonant controller. ω controls the bandwidth of the resonant controller and hence response of the controller and its filtering ability depends on the choice of ω. Usually a cut off frequency of 0.5Hz-2Hz will be chosen for these controllers.

6.5 Simulation Results

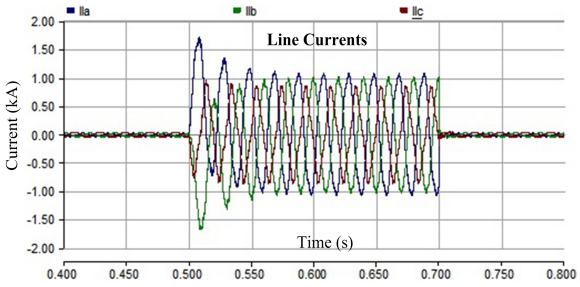
Simulations using PSCAD/EMTDC have been carried out for a 10-kV system to test the proposed DFCL control algorithm which is based on virtual impedance. The simulations are performed for a symmetrical and asymmetrical downstream faults. The DVR is connected in series with the distribution feeder and are introduced into the system from 0.5 s to 0.7 s.

6.5.1 Simulation results when virtual impedance based DFCL for DVR is in bypass mode

Figure 6.5 show PCC voltages and the line currents respectively, with DVR bypassed. The PCC voltages shown in the Figure 6.5a drop to about more than 50% of the nominal voltage. It is obvious that downstream fault causes extremely high currents (1.5 kA) as shown in Figure 6.5b which are due to very low source and line impedance.



(a)



(b)

Figure 6.5: During three-phase short circuit with DVR bypassed: (a) PCC voltages, (b) Line current

6.5.2 Simulation results of virtual impedance based DFCL for DVR during activation mode

The system voltages and currents with DVR actively controlled by proposed DFCL control algorithm which is based on virtual impedance are shown in Figure 6.6 and Figure 6.7. Now the system is subjected to a symmetrical three phase fault during aforementioned time intervals. As expected, the PCC voltages are restored which can be seen from Figure 6.6(b), by limiting the fault currents (5.2 A as seen from zoomed view). The DVR cuurents shown in the Figure 6.6(c) are measured after filter capacitor. The injection transformer turns ratio is 1:10 thus the currents at the secondary side of the transformer will be 52 A. Figure 6.6(a),(d) shows the load voltages and DVR injected voltages respectively. Therefore, the loads on other parallel feeders connected to PCC will not be affected.

The system is also tested for asymmetrical fault conditions by creating two phase short circuit fault in phase-b and phase-c. Due to the occurrence of the fault the VI-FCL control mode is activated and DVR acts as virtual impedance to limit the fault current. Figure 6.7(a)-(d) shows the performance of proposed VI based FCL during

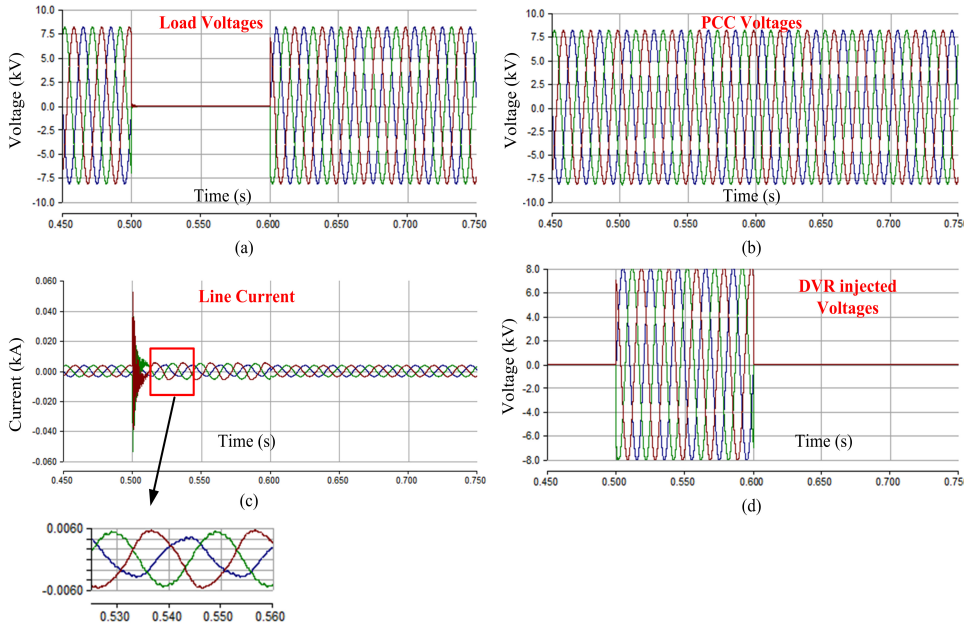


Figure 6.6: VI based FCL for DVR during three-phase short circuit with (a)Load Voltages, (b)PCC voltages (c) DVR side line current, (d) DVR injected voltages

asymmetrical fault conditions. The fault currents are asymmetrical with slow decay of DC component. As said above during the fault period the currents are limited to 5.2 A from Figure 6.7(c). From Figure 6.7(b) it is observed that the PCC voltages are maintained constant even during the asymmetrical fault conditions.

Thus from the above analysis it is concluded that the proposed VI based FCL works efficiently during symmetric and asymmetric faults and to limit the fault current and to restore the PCC voltages

6.6 Description of TDVR system

In conventional DVR there are several issues namely, cost, weight, and losses related with the series injection transformer which constraints its applications to heavy area. To overcome these limitations of the conventional DVR, a TDVR scheme with reduced cost, weight, size, and losses has been proposed. This section presents a uncertainity and disturbance estimator control scheme for TDVR to maintain load voltage at a constant value during voltage disturbance viz., sag and swells.

The power circuit diagram of the single-phase TDVR compensated system is

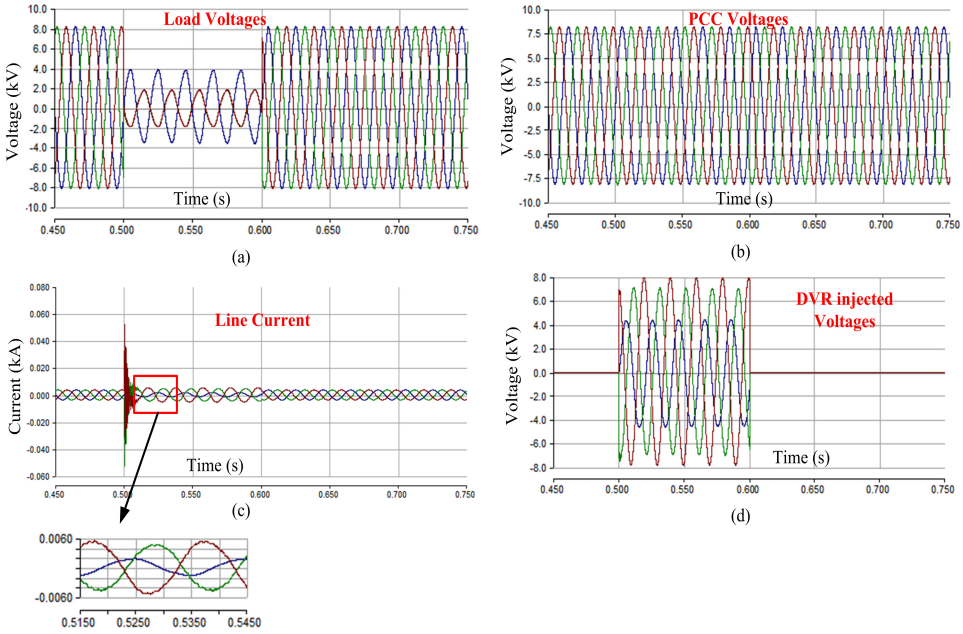


Figure 6.7: VI based FCL for DVR during two-phase short circuit with (a)Load Voltages, (b)PCC voltages (c) DVR side line current, (d) DVR injected voltages

shown in Figure 6.8. The source voltage is represented by V_s. The resistance and inductance of the source are represented by R_s and L_s, respectively. The source, load, filter, and series capacitor currents are represented by i_s, i_l, i_f, and i_{se}, respectively. The TDVR consists of a halfbridge VSI, an output filter (L_f and C_{se}), and neutral-point clamped dc capacitors. The voltage across the filter capacitor(v_{se}) connected in series with the line is controlled to maintain the desired voltage at the load point.

The equivalent circuit of the TDVR at any time of operation is shown in Figure 6.9. The term u is the switching variable. The upper and lower switches, S_u and S_l, respectively, are operated in a complementary way, i.e., if (u = 1) then upper switch is ON and lower switch will be OFF. Similarly, if (u =-1) then the lower switch is ON and upper switch is OFF. A voltage of V_{dc} is maintained across each of the dc-link capacitor C_{dc}. A voltage of v_{se} is generated across the series capacitor by the proper operation of the VSI to maintain the load voltage sinusoidal with constant magnitude.

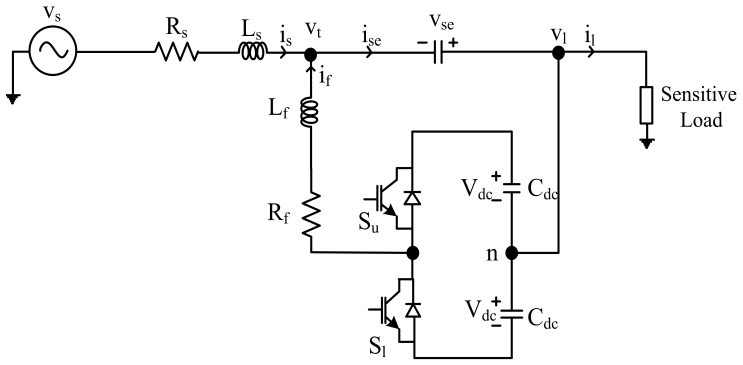


Figure 6.8: Single-phase TDVR compensated distribution system

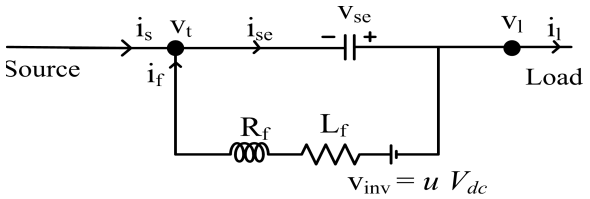


Figure 6.9: Equivalent circuit of TDVR in distribution system

6.7 Description of proposed control algorithm

In (Kumar and Mishra, 2015) a predictive control approach is proposed for the TDVR to compensate the voltage disturbances. In this method the prediction of the reference capacitor voltage is essential which is dependent on the filter parameters.Therefore, the performance of the predictive control is subject to degradation when the reference capacitor voltage prediction is not accurate due to the variations in the filter parameters. In (Komurcugil and Biricik, 2017) sliding mode control scheme is proposed for TDVR. Though sliding mode controllers are insensitive to parameter variations they could cause large input gains, which can be considered as serious limitation.

Uncertainty and Disturbance Estimator (UDE) based control method was proposed in (Zhong and Rees, 2004), (Zhong et al., 2010), (Ren et al., 2017), which has good abilities of reference tracking, uncertainty and disturbance rejection, and is considered as a replacement of the time-delay control. The UDE-based control method is based on the assumption that, by using an appropriate filter, an unknown continuous band-limited signal can be estimated and thereby making it a practical robust controller. The design procedure is simple as the accurate model of uncertainties and external disturbances is not required. During the past few years, the UDE-based

control method has attracted considerable attention. The main advantages are as follows:

- A simple control structure is obtained, which consists of three parts: differential feedforward, model inversion, and PI regulator.

- The PI regulator parameters (proportional and integral gains) are expressed in the desired closed-loop bandwidth and the approximate lumped disturbance bandwidth, which make it possible to achieve a satisfactory performance by using a quite simple and straightforward tuning algorithm.

The equivalent circuit of TDVR shown in Figure 6.9 is a second order circuit. In this circuit, the current through the filter inductor and the voltage across the series capacitor are taken as the state variables. The dynamics of this system are given by the following differential equations:

By applying KVL following equations are obtained

$$V_{inv} = L_f \frac{di_f}{dt} + R_f i_f - V_{se} \tag{6.11}$$

$$i_s = -C_{se} \frac{dV_{se}}{dt} - i_f \tag{6.12}$$

Before developing the proposed UDE-based voltage control scheme, the differential equations governing the equivalent circuit by taking filter parameter uncertainties into account is derived first. Using nominal parameters, (6.11) & (6.12) can be rewritten as follows:

$$\frac{di_f}{dt} = -\frac{R_{f0}}{L_{f0}} i_f + \frac{1}{L_{f0}} V_{se} + \frac{1}{L_{f0}} V_{inv} + f_{i_f}(t) + D_{i_f}(t) \tag{6.13}$$

$$\frac{dV_{se}}{dt} = -\frac{1}{C_{se0}} i_s - \frac{1}{C_{se0}} i_f + f_{V_{se}}(t) + D_{V_{se}}(t) \tag{6.14}$$

where f_{if} and f_{Vse} represent uncertain dynamics caused by the parameter variations, and $D_{if}(t)$ and $D_{Vse}(t)$ are unknown external(load) disturbances respectively. Here uncertainties in filter parameter variations are considered for deriving control equation. Uncertain dynamics in above equation are expressed as

$$f_{i_f}(t) = -\frac{\Delta R_f}{L_{f0}} i_f - \frac{\Delta L_f}{L_{f0}} \frac{di_f}{dt} \tag{6.15}$$

$$f_{V_{se}}(t) = -\frac{\Delta C_{se}}{C_{se0}} \frac{dV_{se}}{dt} \tag{6.16}$$

where $\Delta R_f = R_f - R_{f0}$, $\Delta L_f = L_f - L_{f0}$, $\Delta C_{se} = C_{se} - C_{se0}$ "0" denotes nominal parameter value.

Let $X = [i_f, v_{se}]^T$ is the state vector, $u = [V_{inv}, i_s]^T$ is the control input vector, $f = [f_{if}, f_{vse}]^T$ is the unknown dynamics vector. The mathematical model of (6.13),(6.14) can be expressed in state space format as shown below

$$\dot{x(t)} = Ax(t) + Bu(t) + f(t) + d(t) \tag{6.17}$$

where $A = \begin{bmatrix} -\frac{R_f}{L_f} & \frac{1}{L_f} \\ -\frac{1}{C_{se}} & 0 \end{bmatrix}$; $B = \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{C_{se}} \end{bmatrix}$ Now a reference model along with error dynamics is to be modelled and it can be defined with the response of linear time-invariant (LTI) reference model as

$$\dot{x_m(t)} = A_m x_m(t) + B_m c(t) \tag{6.18}$$

where $x_m = [i_{fm}, V_{sem}]^T$, is the reference state vector, $c = [i_f^*, V_{se}^*]^T$ is the reference command vector $A_m = \begin{bmatrix} -\alpha & 0 \\ 0 & -\alpha \end{bmatrix}$; $B_m = \begin{bmatrix} \alpha & 0 \\ 0 & \alpha \end{bmatrix}$ The control objective is to determine a control input vector u(t) such that x(t) asymptotically tracks its reference trajectory $x_{m(t)}$, i.e., the tracing error asymptotically converges to zero.

$$e(t) = x_m(t) - x(t) \tag{6.19}$$

Since B is invertible, control input vector is given by

$$u(t) = B^{-1} \left[A_m x_m(t) + B_m c(t) - Ax(t) - f(t) - d_0(t) - d(t) \right] \tag{6.20}$$

by substituting (6.20) into (6.17)

$$\dot{x(t)} = A_m x_m(t) + B_m x(t) \tag{6.21}$$

by subtracting (6.21) from(6.18)

$$\dot{e}(t) = A_m e(t) \tag{6.22}$$

According to (6.18), the lumped disturbances, including the uncertain dynamics vector f(t) and the unknown disturbance vector d(t), can be defined as

$$u_{de}(t) \triangleq f(t) + d(t) \tag{6.23}$$

Following the design procedures presented in (Zhong and Rees, 2004), if a filter $g_f(t)$ is chosen appropriately, $u_{de}(t)$ can be approximated by

$$\overset{\Lambda}{u}_{de}(t) = u_{de}(t) * g_f(t) \tag{6.24}$$

where * is a convolution operator.

$$u(t) = B^{-1}\left[A_m x(t) + B_m c(t) - Ax(t) - d_0(t) - u_{de}(t) * g_f(t)\right] \tag{6.25}$$

from (6.18), $u_{de}(t)$ can be expressed as

$$u_{de}(t) = \dot{x_m}(t) - [Ax(t) + Bu(t) + d_0(t)] \tag{6.26}$$

substituting (6.26) into (6.25) results in

$$u_{de}(t) = B^{-1}\left[A_m x(t) + B_m c(t) - Ax(t) - d_0(t) - \left[\dot{x_m}(t) - Ax(t) - Bu(t) - d_0(t)\right] * g_f(t)\right] \tag{6.27}$$

and the UDE based control law can be derived as

$$u(t) = B^{-1}\left[\ell^{-1}\left\{\frac{1}{1-G_f(s)}\right\} * (A_m x(t) + B_m c(t)) - Ax(t) - d_0(t) - \ell^{-1}\left\{\frac{sG_f(s)}{1-G_f(s)}\right\} * x(t)\right] \tag{6.28}$$

Strictly, filter $G_f(s)$ must be designed as a proper filter with unity gain and zero phase shift over the spectrum of the lumped disturbances $u_{de}(t)$ and zero gain elsewhere. However, it is hard to fully meet this demand. Here, a first-order low-pass filter is chosen because it is simple enough and can cover the spectrum of the major uncertainty and disturbance by setting an appropriate bandwidth i.e.,

$$G_f(s) = \frac{\beta}{s+\beta} \tag{6.29}$$

where β is the bandwidth of $G_f(s)$. It is also worth noting that

$$\frac{1}{1-G_f(s)} = 1 + \frac{\beta}{s} \tag{6.30}$$

and

$$\frac{sG_f(s)}{1-G_f(s)} = \beta \tag{6.31}$$

Considering (6.30) and (6.31), the UDE based control law (6.28) can be written in the s-domain form as shown below and respective control block diagram is shown in Figure 6.10.

$$U(s) = B^{-1}\left[(A_m X_m(s) + B_m C(s)) - (AX(s) + D_0(s)) + (\beta I - A_m)E(s) - \frac{\beta}{s}A_m E(s)\right] \tag{6.32}$$

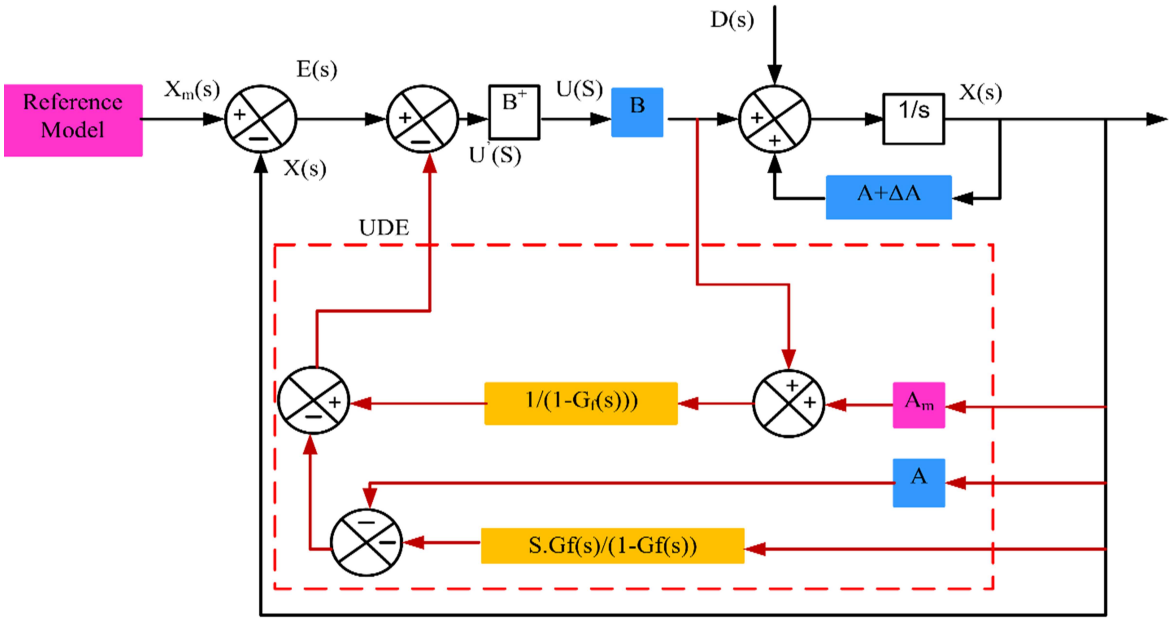


Figure 6.10: Control block diagram of UDE scheme

6.8 Simulation results of proposed Uncertainty Disturbance Estimator (UDE) control based TDVR to compensate voltage sags

The dynamic performance of TDVR to compensate voltage sags with the proposed control scheme is tested using MATLAB software. The source voltage of 230 V(rms) is considered as 1 pu. Further the efficacy of the proposed control scheme for parameter mismatch is also validated and respective results are presented.

Figure 6.11 shows the results of voltage sag compensation by TDVR. Firstly, up to 0.08 sec the source voltage as shown in Figure 6.11(a) is in its nominal condition and therefore the injected voltage is zero. From 0.08 s to 0.17 s a symmetric voltage sag of 0.3 pu occurs in the source voltage. During this time interval, the TDVR injects the required voltage to maintain the load voltage at prefault level as shown in Figure 6.11(a).

From 0.1 sec to 0.15 sec, the source voltage undergoes two phase voltage sag as shown in Figure 6.11(b). The TDVR produces the necessary voltage to increase the load voltage to the prefault value. The small disturbances on the load voltage as seen in Figure 6.11 is due to the LC filter transients that has been used at the output of the inverter. Similarly, Figure 6.11(c) depicts the voltage sag in phase-a and it is observed that the load voltage is maintained constant. The waveforms confirm that the UDE control scheme works effectively for symmetric and asymmetric voltage sags.

6.8.1 Dynamic performance of TDVR with UDE control scheme under parameter mismatch conditions

In the previous section the simulation results for compensation of voltage sags by TDVR based on UDE control law are presented. To prove the robustness of the proposed control scheme the dynamic performance of TDVR compensating symmetric and asymmetric voltage sags under mismatch conditions of TDVR filter parameters are analyzed. The main causes for variation of filter parameters are due to tolerance of filter components(ageing effect), operating conditions. Thus it is necessary to design the controller which is robust to parameter varriation. The filter parameters are varied to 30% (increase) from its nominal value(L_f:4 mH to 5.2 mH and C_{se}:925μF to 1020μF). Figure 6.12(a) shows the performance of proposed UDE control scheme

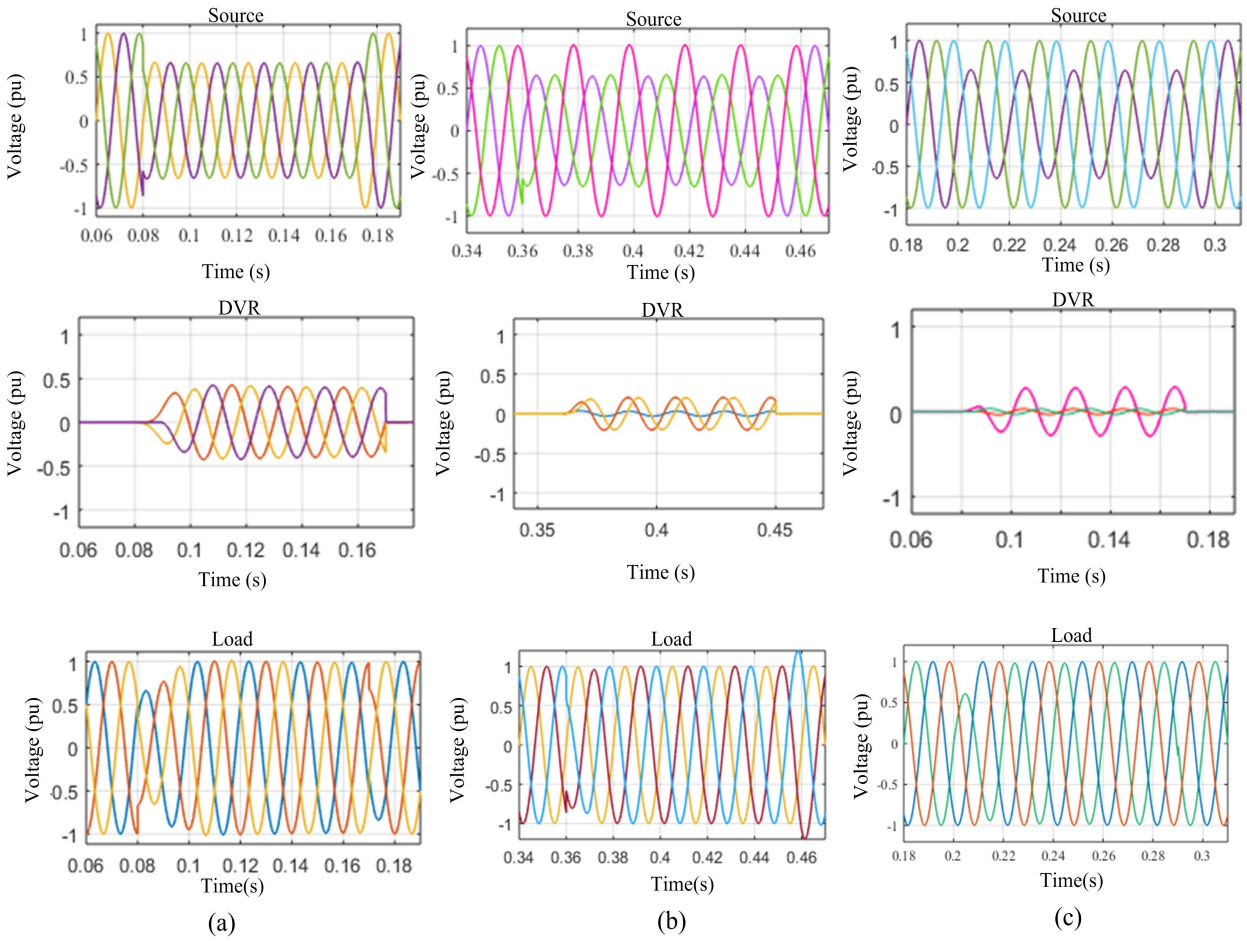


Figure 6.11: Simulation results of TDVR compensating voltage sags: (a) Three-phase sag, (b) Two-phase sag, (c) Single phase-sag

under the filter parameter mismatch conditions. Initially the filter parameters are maintained at nominal values. The symmetric voltage sag is initiated at 0.08 s with nominal L and C values and the parameter variation i.e., step change in the filter parameters (both L and C) is given at 0.16 s and continued up-to 0.24 s where the voltage sag duration is completed. During this time it is observed that the load voltage as seen in the Figure 6.12(a) shows that though the parameters are varied the load voltage is maintained at constant value and similar observations are made for Figure 6.12(b).Thus the aformentioned results prove the robustness of UDE control law to parameter mismatch conditions and to the voltage disturbances(voltage sags).

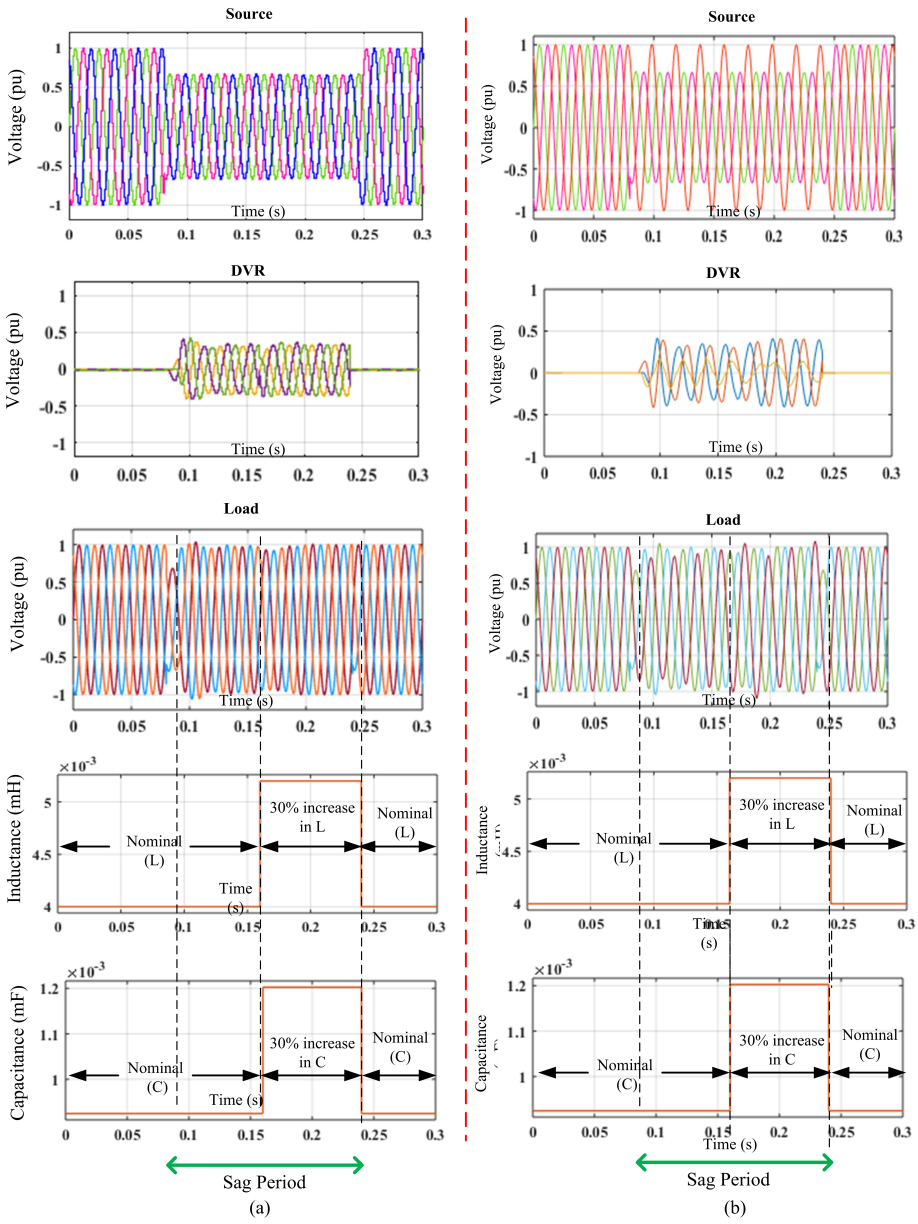


Figure 6.12: Perfromance of UDE control scheme under 30% variation of filter parameters: (a) Dynamic performance of TDVR under symmetric sag (b)Dynamic performance of TDVR under two phase sag

6.8.2 Comparison of UDE based TDVR system with conventional PI controller based TDVR system

To verify the robustness of the proposed UDE based TDVR system, a comparative time response analysis is performed with conventional PI controller based TDVR system. The simulation parameters remains the same as mentioned earlier. The analysis is carried out for two cases i.e.., three phase sag and two phase voltage sag as shown in Figure 6.13. It is observed from Figure 6.13 that the load voltage response of UDE based TDVR system for three phase sag takes30 ms to reach its final steady state while the PI controller based system takes 36 ms. On the other hand the UDE based system exhibits an under shoot of 25.8% while the PI controller exhibits 30%. Similarly Figure 6.14 depicts the dynamic analysis of the TDVR system for filter LC variation to prove the efficacy of the UDE controller. The analysis is carried out for both balanced and unbalanced sag and the observations are tabulated in the Table 6.1 & 6.2. It is observed that the settling time and undershoot of the UDE controller under voltage disturbances remains same whereas the PI controller based system exhibits a settling time of 45 ms and an undershoot of 30% for three phase voltage sag. Moreover the as observed from the Figure 6.14 the load voltage response of PI controller based TDVR system do not settle to its prefault value during the voltage sag. From this analysis it can be concluded that the UDE performance is better even in parameter uncertainities conditions.

Table 6.1: Time response analysis of PI and UDE controller based TDVR system for symmetric and asymmetric voltage sags

Controllers	**Balanced sag**		**Two phase sag**	
	Under-shoot(%)	**Settling time(ms)**	**Under-shoot(%)**	**Settling time(ms)**
UDE	25.8	30	17	20
PI	30	36	19.3	25

Table 6.2: Time response analysis of PI and UDE controller based TDVR system for symmetric and asymmetric voltage sags under parameter mismatch

Controllers	**Balanced sag**		**Two phase sag**	
	Under-shoot(%)	**Settling time(ms)**	**Under-shoot(%)**	**Settling time(ms)**
UDE	25.8	30	17	20
PI	30.8	45	19.3	33

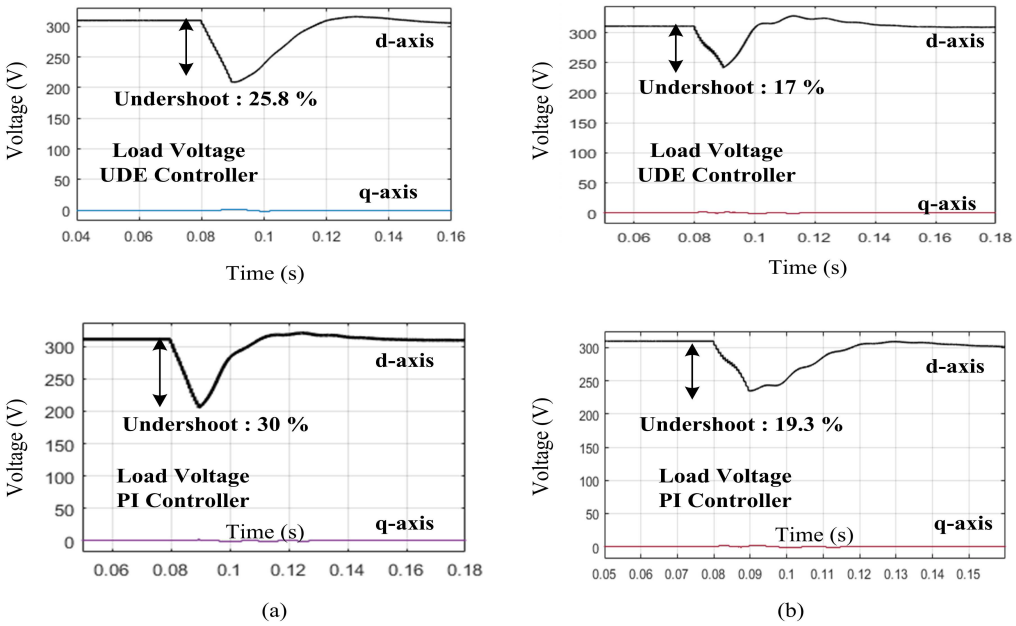


Figure 6.13: Load Voltage response of TDVR system for UDE and PI controller under : (a) Three phase sag, (b) Two Phase sag

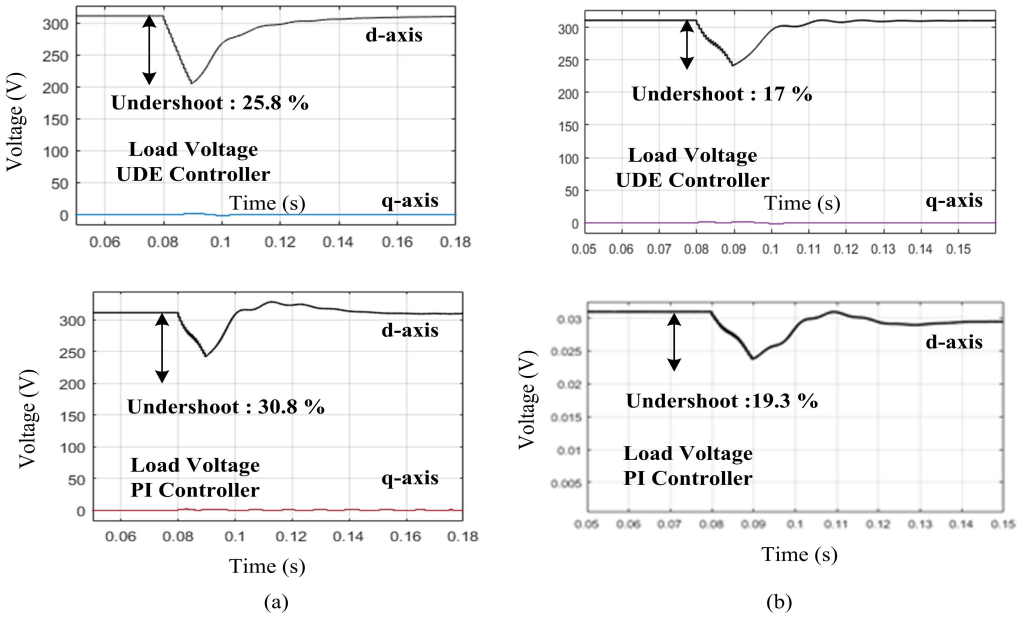


Figure 6.14: Load Voltage response of TDVR system for UDE and PI controller during filter parameter mismatch under : (a) Three phase sag, (b) Two Phase sag

6.9 Experimental results

The UDE control scheme is implemented on FPGA board to control a reduced scale experimental setup with a source voltage of 50 V(rms). The power circuit of custom made TDVR with SEMIKRON-made IGBT based VSI, an output filter, Hall effect voltage and current transducers, signal conditioning circuit (as shown in Figure.6.15). The reference load voltage magnitude is set at 50 V. The experiments are conducted for three phase and two phase voltage sag with resistive load. For comparison, the conventional PI voltage control is also implemented for voltage control of TDVR system along with UDE voltage controller. Figure 6.16 also depicts the dynamic response (dq) of load voltages for PI and UDE controllers. In Figure 6.16(a) three phase sag is created which lasts for 2 s. The DVR initates the injection process and maintains the load voltage constant to the prefault value which can be observed from Figure 6.16. The PI controller based system (Figure 6.16(b)) posses an undershoot of 33.9% whereas the UDE controller based system(Figure 6.16(a)) posses an undershoot of 20.4%.Similarly during the two phase voltage sag the DVR is able to inject the voltage and maintains the constant load voltage. Similarly during the two phase voltage sag as shown in Figure 6.16(b) the PI controller based system posses an undershoot of 21.9 % whereas the UDE controller based system posses an undershoot of 14.4% (Figure 6.16)(b). Thus the above results validate that the UDE based voltage control scheme tracks the reference voltage effectively while maintianing the load voltages constant. Figure 6.17 shows three-phase representation of UDE-based DVR system for symmetric voltage sag. In Figure 6.17, the symmetric sag is initiated which lasts for 2 s. It is observed that the TDVR starts injection when sag is initiated and maintains the load voltage constant to the prefault value.

6.10 Conclusion

In this chapter design of control algorithm for operating DVR as fault current limiter and as TDVR is discussed. The following points summarize the chapter

a) Firstly the flux charged based control is presented which posses the demerit of problems arising due to the pure integration of flux variable which leads to saturation.

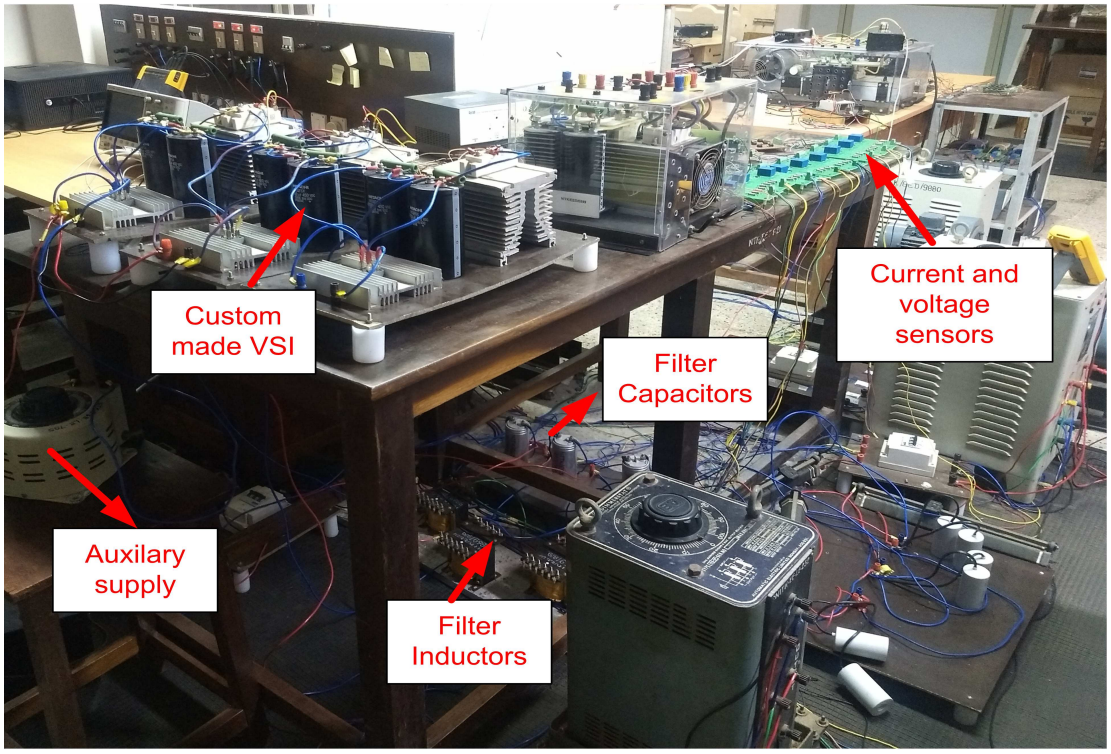


Figure 6.15: TDVR Experimental setup

b) To overcome this problem virtual impedance based control is proposed where the DVR acts as series impedance to limit the fault current and protects the PCC voltages during the downstream faults. Further the design of virtual impedance parameter is discussed in detail.

c) Meanwhile,the simulation studies are carried out for both symmetric and asymmetric faults to test the efficacy of the proposed VI based FCL.

d) The results demonstrate that by using the proposed VI-DFCL the fault currents are limited to 52 A (at the secondary side of the transformer) which is only 1.6 times the rated line current (compared to 1 kA) when VI-DFCL based control of DVR is bypassed which proves the efficacy of the proposed VI-DFCL control algorithm for DVR.

e) The modelling of TDVR system is discussed and the description of proposed controller is explained. The proposed controller includes one differential feedforward term, model inversion to cancel known model dynamics and PI regulator

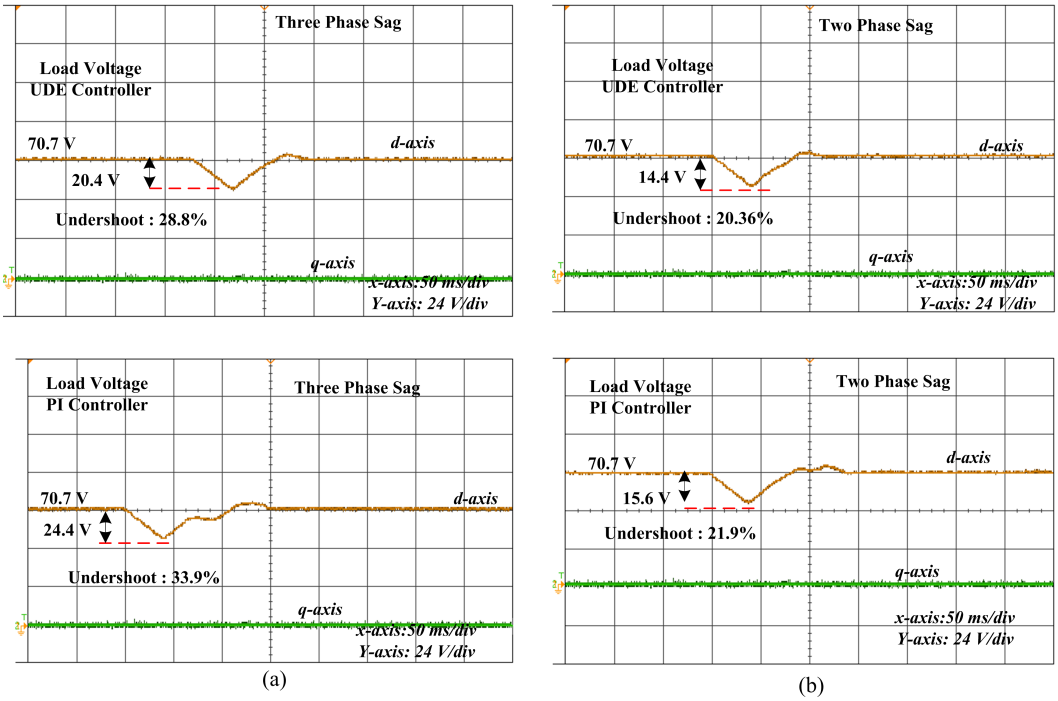


Figure 6.16: Load Voltage response of TDVR system for UDE and PI controller under : (a) Three phase sag, (b) Two Phase sag

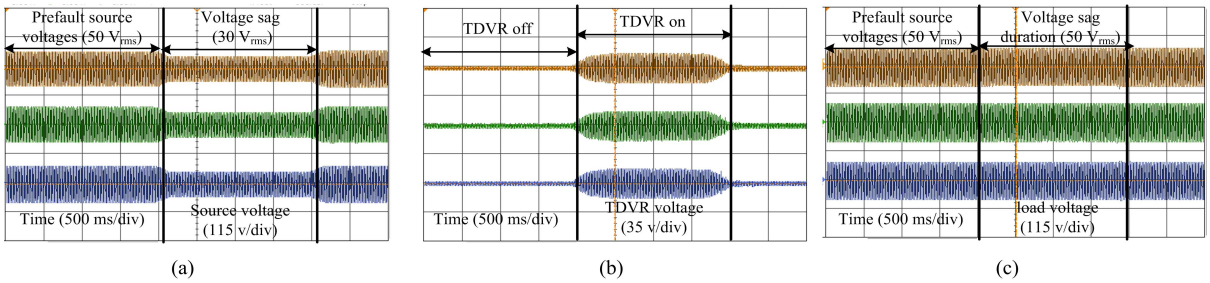


Figure 6.17: Three-phase representation of experimental results of UDE-based TDVR system under three phase sag: (a) Source voltage, (b) TDVR voltage, (c) Load voltage

to compensate the tracking error between the reference state vector and the actual state vector.

Chapter 7

Perfromance analysis of series Interfacing Converter (IC) in hybrid AC/DC Microgrid

Contents

7.1 Introduction

In this chapter various control strategies required to achieve the different modes of operating (multifunctional operation) series converter in hybrid microgrid is analysed. To achieve the following goals, the IC control system is designed in such a way that the IC operates in bidirectional mode:

- effective power management between ac utility grid and dc subgrid.
- to maintain the dc-bus voltage of the dc subgrid stable.

Taking into account, the aforementioned IC objectives the key considerations for IC control system are

- evaluating the power management between ac utility grid and dc subgrid.
- generating the improved reference signals of IC for both ac utility and dc subgrid coordinately.
- maintaining ac and dc bus voltages during faults at either side.

Firstly in this chapter different operating modes of hybrid microgrid is presented then followed by the discussion of control schemes for various operating modes of series converter.

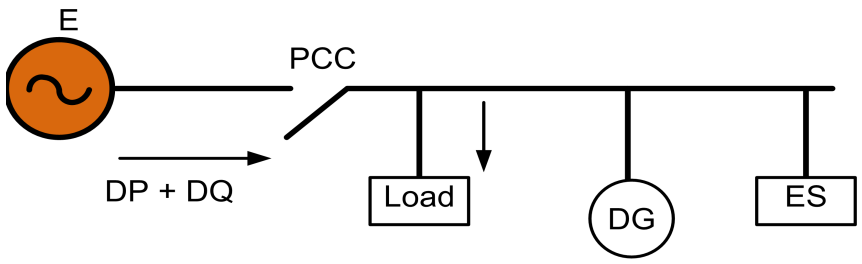


Figure 7.1: Power exchange between distribution network and microgrid

7.2 Operation Modes

A microgrid may operate either in grid-connected or in islanded mode, and grid-connected operation is further divided into power-matched operation and power-mismatched operation according to power exchange. As shown in Figure 7.1, the microgrid is connected to the distribution network via a PCC, the active and reactive power flowing through the PCC is, respectively, ΔP and ΔQ. When $\Delta P = 0$ and $\Delta Q = 0$, the current through PCC is zero, indicating that the DG output and load reach a balance and no power exchange occurs between the distribution network and microgrid. This is the most economic operation mode of the microgrid, known as power matched. When $\Delta P \neq 0$ or $\Delta Q \neq 0$, the current through the PCC is not zero, indicating that power exchange occurs between the distribution network and the microgrid. This mode is known as power-mismatched operation. In this mode, if $\Delta P < 0$, the excessive active power from DG's after meeting load demand is injected to the distribution network; if $\Delta P > 0$, the electricity from DGs is insufficient for meeting load demand, requiring the distribution network to provide the deficit. Likewise, reactive power is excessive if $\Delta Q < 0$ and deficient if $\Delta Q > 0$. All these operations are power mismatched operation variants.

7.2.1 Grid-connected operation

In grid-connected mode, the microgrid is connected to and exchanges power with the distribution system of the utility grid via PCC. Figure 7.2 shows the schematic diagram of transfer between operation modes.

- When the microgrid is shutdown, it can be transfered to grid-connected mode directly by grid connection control. Similarly, when it is in grid connected mode,

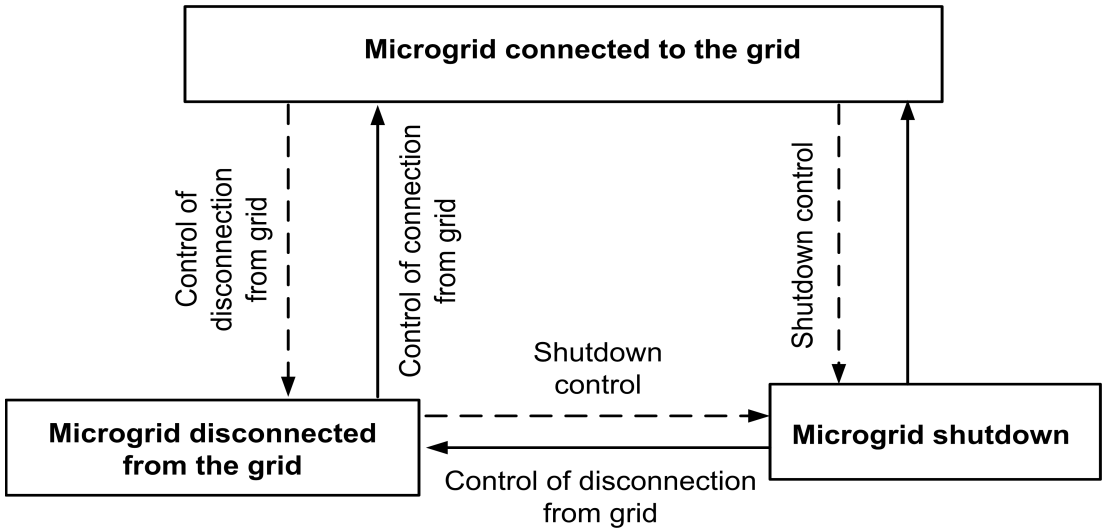


Figure 7.2: Transfer between operation modes

it can be disconnected from the grid by shutdown control.

- When the microgrid stops operation, it can transfer to islanded mode directly by disconnection control, and when it is in islanded operation, it can be connected to the grid-by-grid connection control.
- When the microgrid operates in parallel with the grid or in islanded mode, the microgrid can be shut down by shutdown control.

7.2.2 Islanded operation

Islanded operation means that the microgrid is disconnected from the distribution system of the main grid at the PCC following a grid failure or as scheduled, and that the DGs, ESs, and loads within the microgrid operate independently. In islanded mode, since the electricity produced by the microgrid itself is generally small and insufficient to meet the demand of all loads, it is necessary to prioritize loads based on their importance and ensure uninterrupted supply to important loads.

- **Stability:** regulation of the voltage and frequency of the microgrid operating at different modes. Moreover, it ensures a stable and reliable power network both in the ac- and dc-side of the microgrid.
- **Protection:** monitoring of energyflow and critical devices, and fault management of the grid.

- **Power balance:** optimal load sharing and DG supply coordination.
- **Transition:** seamless transition between microgrid modes of operationi.e. islanding to grid-tied mode or vice versa.
- **Power Transmission:** exchange of power between the microgrid and the utility grid.
- **Synchronization:** synchronization of the microgrid with the power network for an optimal transmission of power.
- **Optimiztion:** depending on the conditions of the microgrid and the utility grid (e.g. market situation, power demand/ supply or energy forecast), management of the systems to reduce costs, improve energy efficiency, etc.

7.3 Proposed Interlinking Converter in Hybrid AC/DC microgrid

An advanced hybrid dc/ac station is combination of ac and dc sources which controls the ac and dc energy flows, coming from the grid utility and local renewable DGs and feeds ac and dc loads. The main topology of the proposed hybrid ac/dc MG formed by integrating the dc subgrid with IC is shown in Figure 7.3. The presented hybrid ac/dc system is composed of a bidirectional energy conversion station using an IC with an ac distribution line with ac loads (linear and non-linear) and ac sources , a dc subgrid with dc loads, dc sources and a storage system. In Figure 7.3, a conventional three phase three-leg IGBT (insulated gate bipolar transistor)-based converter is implemented to operate in bidirectional mode. The different modes of operation investigated in the present thesis are discussed as follows. The different modes of operation investigated in the present report are discussed below.

7.3.1 AC Voltage control (Mode-1 & Mode-2)

This mode deals with proposed control scheme for IC during upstream and downstream faults. Figure 7.4(a),(b) represents the scenario of upstream and downstream faults where the series converter acts as custom power device to inject appropriate voltage into the system. During upstream faults (source side) the proposed control

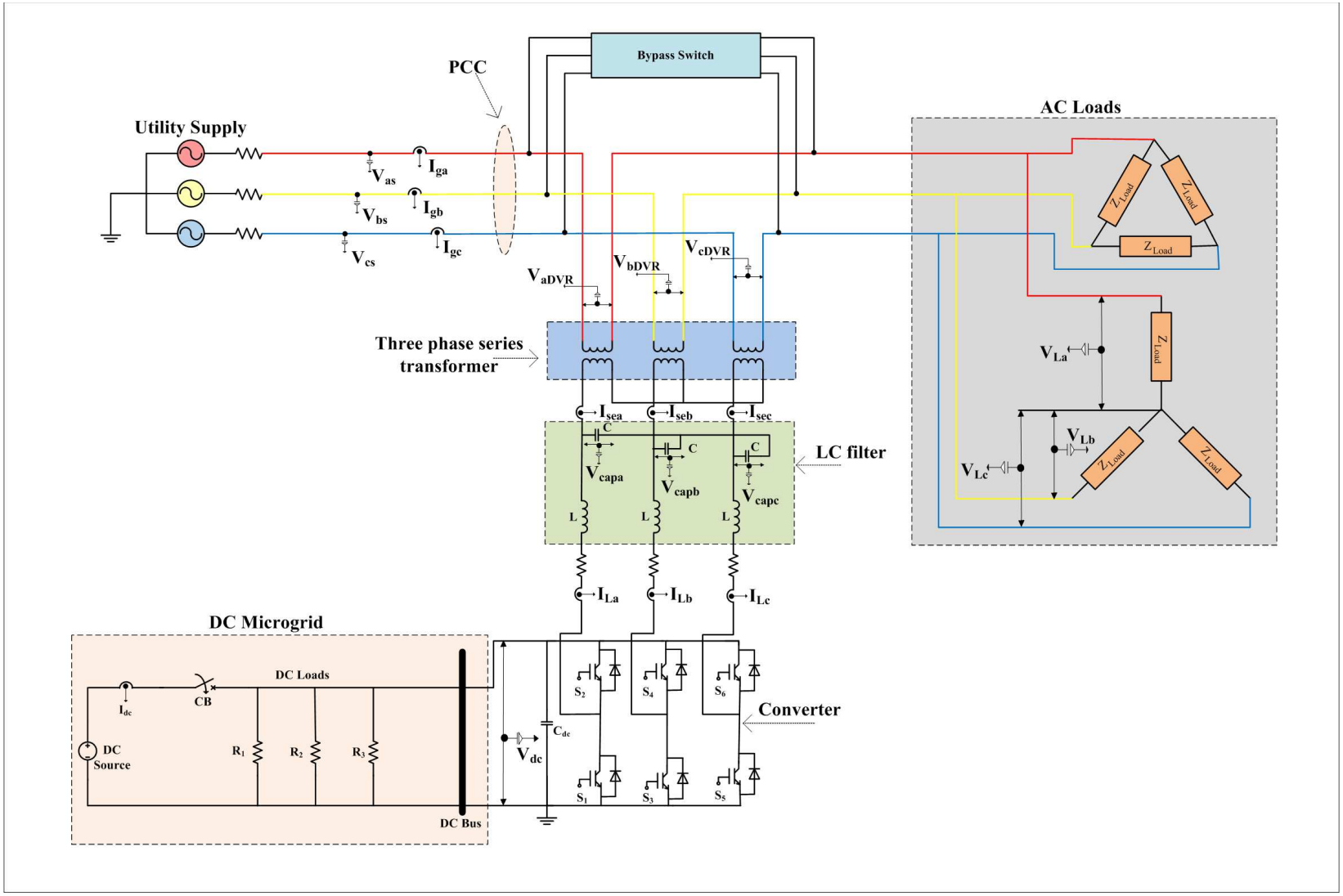


Figure 7.3: Simple Representation of Hybrid AC/DC System

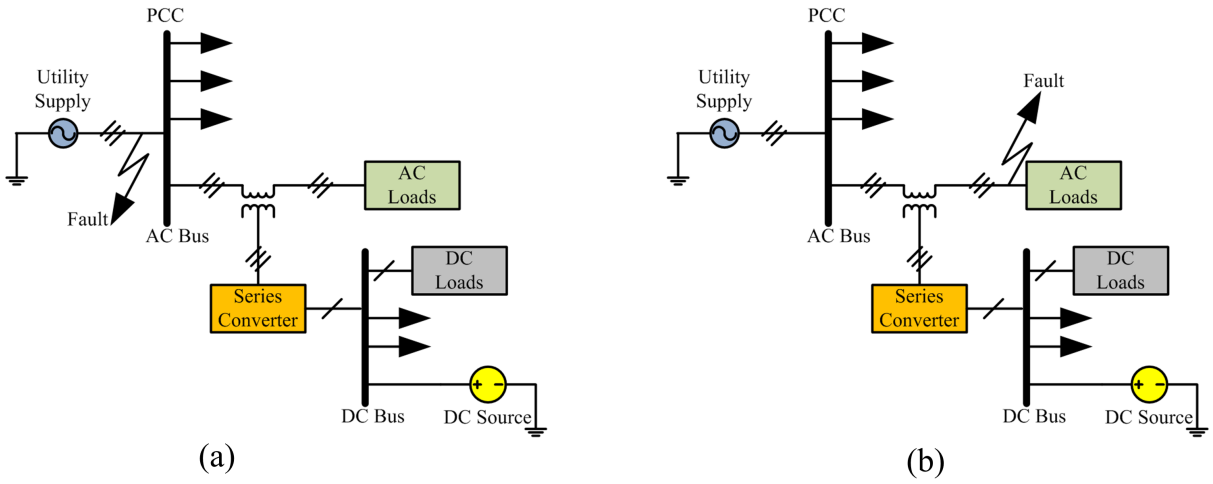


Figure 7.4: AC Voltage Control: (a) Upstream Fault, (b) Downstream fault

scheme compensates for symmetric and asymmetric voltage sags. On the other hand, for downstream faults a fault current limiting function (FCL) is proposed to protect the PCC voltages and thereby the loads in other parallel feeders are not disturbed.

7.3.2 DC Voltage control (Mode-3):

Unlike the above case in this mode the system is analysed during the faults at DC microgrid side (Figure 7.5). During this mode the voltage at DC bus decreases causing disturbance to the connected DC loads. When the DC voltage decreases less than the threshold limit IC enters to mode-3 operation and acts as rectifier where the supply is drawn from utility side to supplement the DC voltage at desired level.

7.3.3 Power management control(Mode-4 and Mode-5):

- **Mode 4:** In this mode power management of hybrid microgrid is analysed by assuming a situation where the power at DC microgrid is reduced. Now the aim is to support DC loads and thus sustain stable hybrid microgrid operation by power management from AC to DC grid (Figure 7.6(a)). Thus, the role of IC in this mode is to achieve bidirectional power flow.

- **Mode 5:** Similar to the above case mode-5 depicts the operation of IC during the excess power at DC side (Figure 7.6(b)). Thus, power management control

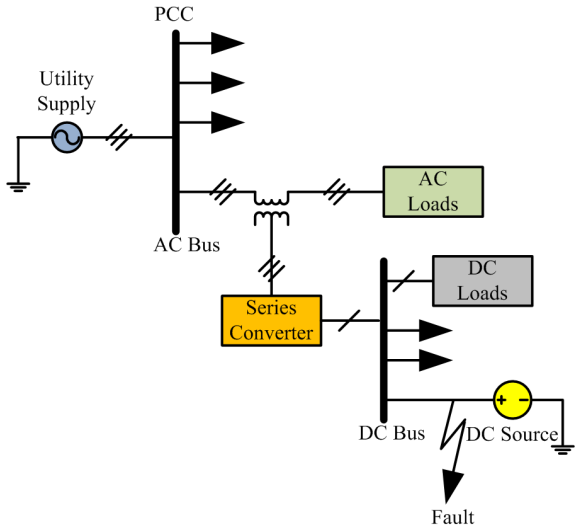


Figure 7.5: DC Voltage control(Mode-3)

utilizes the IC to transfer the active power to the AC load and maintain the system in stable condition.

7.4 Control strategies for multifunctional IC

In this section various control strategies required to achieve the multifunctional operation of IC in hybrid microgrid is analysed.

7.4.1 DVR Operation

In the DVR mode the main control objective is to maintain the load voltage constant during upstream faults and to maintain the PCC voltages during the downstream fault.

- **Upstream Fault:** Firstly, to compensate upstream fault a modified DVC algorithm with positive and negative sequence controllers is employed (Awad et al., 2004b). CDSC filter is employed to extract ISC of the grid voltage and feedback signals in stationary frame as shown in Figure 7.7. These voltages are converted into positive and negative dq-frames while the phase angle for transformation is provided by CDSC-PLL. Modified DVC consists of positive and negative controllers with capacitor voltage and inductor current feedback. Voltage and

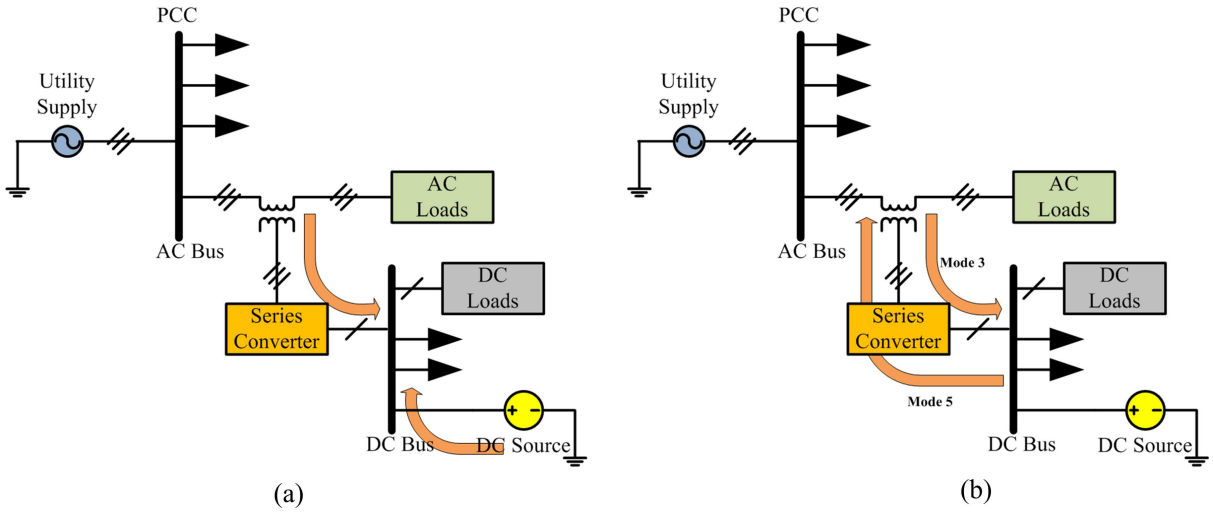


Figure 7.6: Power Management control : (a) Mode-4, (b) Mode-4

current loops employ proportional deadbeat gains k_u, k_p respectively to achieve faster dynamic response. The mathematical equations and design of controller gains are discussed elaborately in (Karthikeyan et al., 2019). When voltage sags occurs CDSC PNSE extracts ISC of the grid voltage and other control signals. The modified DVC tracks both fundamental positive and negative sequence voltages to restore the load voltage to a nominal value.

- **Downstream fault:** Secondly, to compensate the downstream fault a virtual impedance based DFCL is employed (Karthikeyan et al., 2018). by involving additional virtual impedance loops, impedances are introduced into the system during the faults to emulate the physical inductance and resistance in the line. Further, in normal operation, these impedance loops are disabled to avoid unnecessary voltage drop. Upon the occurrence of downstream fault, the DVR is controlled as virtual impedance in series with distribution feeder line to limit the fault current and restore the PCC voltages. A multiloop control scheme is adopted where the outer loop uses a P+Resonant (PR) controller for voltage control and for inner current loop a proportional controller is employed. The mathematical equations and design of impedance parameters are discussed in detail (Karthikeyan et al., 2018).

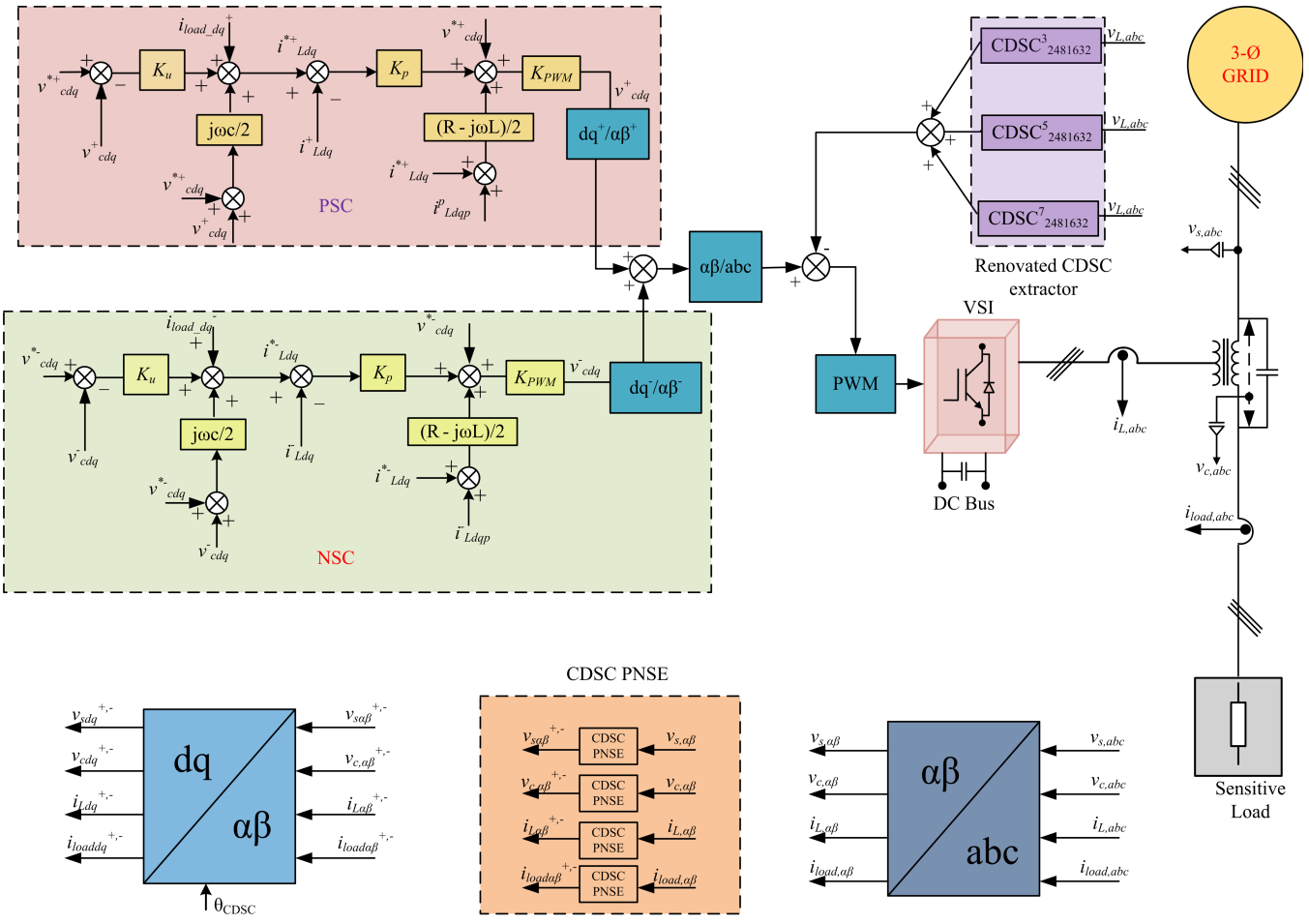


Figure 7.7: Control block diagram of DVR

7.4.2 DC Voltage Control

In this control, dual synchronous reference frames are used, measuring the positive sequence in the positive SRF and the negative sequence in the negative SRF (Hong-Seok Song and Kwanghee Nam, 1999). In the positive SRF, which rotates counter clockwise, the positive sequence appears as dc, while the negative sequence appears as 100 Hz. In contrast, in the negative SRF, which rotates clockwise, the negative sequence appears as dc, while the positive sequence appears as 100 Hz. By eliminating 100 Hz components using a notch filter in each SRF, the positive and negative sequence currents are measured separately, and utilized for constructing two feedback controllers.The extracted positive and negative sequence currents are used as feedback with proportional integral (PI) controllers in the loop, namely the dual current

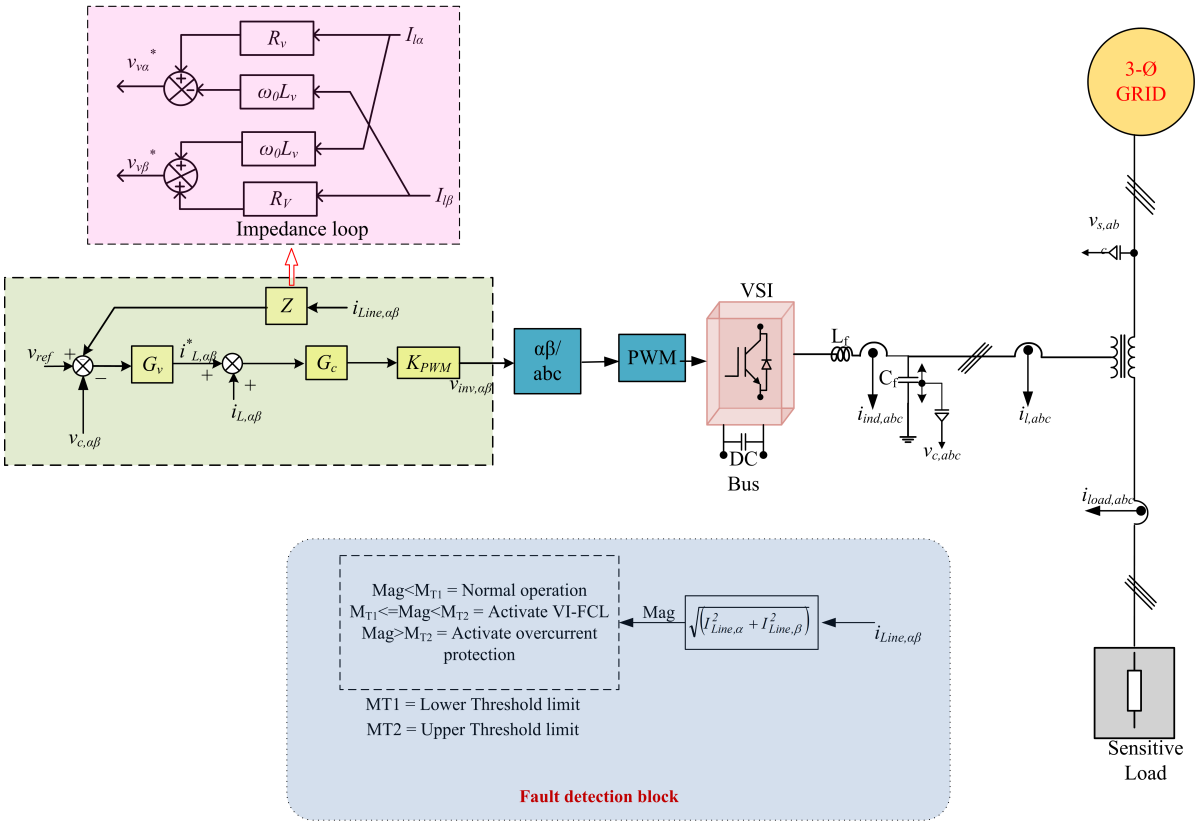


Figure 7.8: Control block diagram of virtual impedance implementation

controller. One regulates only the positive sequence current in the positive SRF, and the other regulates only the negative-sequence current in the negative SRF. This approach allows the negative-sequence current to be controlled completely in its own SRF as a dc signal. Thus, there is no reason to increase the control gain at the risk of making the system unstable.

The apparent power drawn from the utility grid through series interlinking converter is given by S = P + jQ, where real power P and reactive power Q are:

$$P(t) = P_0 + P_{c2}cos(2\omega t) + P_{s2}sin(2\omega t) \tag{7.1}$$

$$Q(t) = Q_0 + Q_{c2}cos(2\omega t) + Q_{s2}sin(2\omega t) \tag{7.2}$$

where

$$\begin{aligned}
P_0 &= 1.5\left(E_d^p I_d^p + E_q^p I_q^p + E_d^n I_d^n + E_q^n I_q^n\right)\\
P_{c2} &= 1.5\left(E_d^p I_d^n + E_q^p I_q^n + E_d^n I_d^p + E_q^n I_q^p\right)\\
P_{s2} &= 1.5\left(E_q^n I_d^p - E_d^n I_q^p - E_q^p I_d^n + E_d^p I_q^n\right)\\
Q_0 &= 1.5\left(E_q^p I_d^p - E_d^p I_q^p + E_q^n I_d^n - E_d^n I_q^n\right)\\
Q_{c2} &= 1.5\left(E_q^p I_d^n - E_d^p I_q^n + E_q^n I_d^p - E_d^n I_q^p\right)\\
Q_{s2} &= 1.5\left(E_d^p I_d^n + E_q^p I_q^n - E_d^n I_d^p - E_q^n I_q^p\right)
\end{aligned} \tag{7.3}$$

The terms E_d^p, E_q^p, E_d^n, E_q^n are positive and negative sequence dq components of the voltage across series windings which are interfaced with the converter. The terms I_d^p, I_q^p, I_d^n, I_q^n are positive and negative sequence dq components of the current which is fed to the converter. The high-order coefficients P_{c2}, P_{s2}, Q_{c2}, Q_{s2} are caused by the voltage unbalance. Real power P is delivered to the dc link and determines the dc voltage level. Hence, if P(t) varies with time for P_{c2}, P_{s2} not being equal to zero, then the dc link voltage fluctuates, i.e. 100 Hz ripple appears. Therefore to keep constant dc level, coefficients P_{c2}, P_{s2} have to be nullified. One also needs to nullify the dc component Q_0 of the reactive power to achieve the unity power factor in an average sense. By expressing power coefficients in the matrix form the following equations are obtained

$$\begin{bmatrix} \frac{2}{3}P_0 \\ \frac{2}{3}Q_0 \\ \frac{2}{3}P_{s2} \\ \frac{2}{3}P_{c2} \end{bmatrix} = \begin{bmatrix} E_d^p & E_q^p & E_d^n & E_q^n \\ E_q^p & -E_d^p & E_q^n & -E_d^n \\ E_q^n & -E_d^n & -E_q^p & E_d^p \\ E_d^n & E_q^n & E_d^p & E_q^p \end{bmatrix} \begin{bmatrix} I_d^p(t) \\ I_q^p(t) \\ I_d^n(t) \\ I_q^n(t) \end{bmatrix} \tag{7.4}$$

Removing dc link voltage ripple and achieving the average zero reactive power necessitates to make $\frac{2}{3}\begin{bmatrix} P_0 & Q_0 & P_{s2} & P_{c2} \end{bmatrix}^T = \begin{bmatrix} \frac{2}{3}P_0 & 0 & 0 & 0 \end{bmatrix}^T$

$$\begin{bmatrix} I_d^p(t) \\ I_q^p(t) \\ I_d^n(t) \\ I_q^n(t) \end{bmatrix} = \begin{bmatrix} E_d^p & E_q^p & E_d^n & E_q^n \\ E_q^p & -E_d^p & E_q^n & -E_d^n \\ E_q^n & -E_d^n & -E_q^p & E_d^p \\ E_d^n & E_q^n & E_d^p & E_q^p \end{bmatrix} \begin{bmatrix} \frac{2}{3}P_o \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7.5}$$

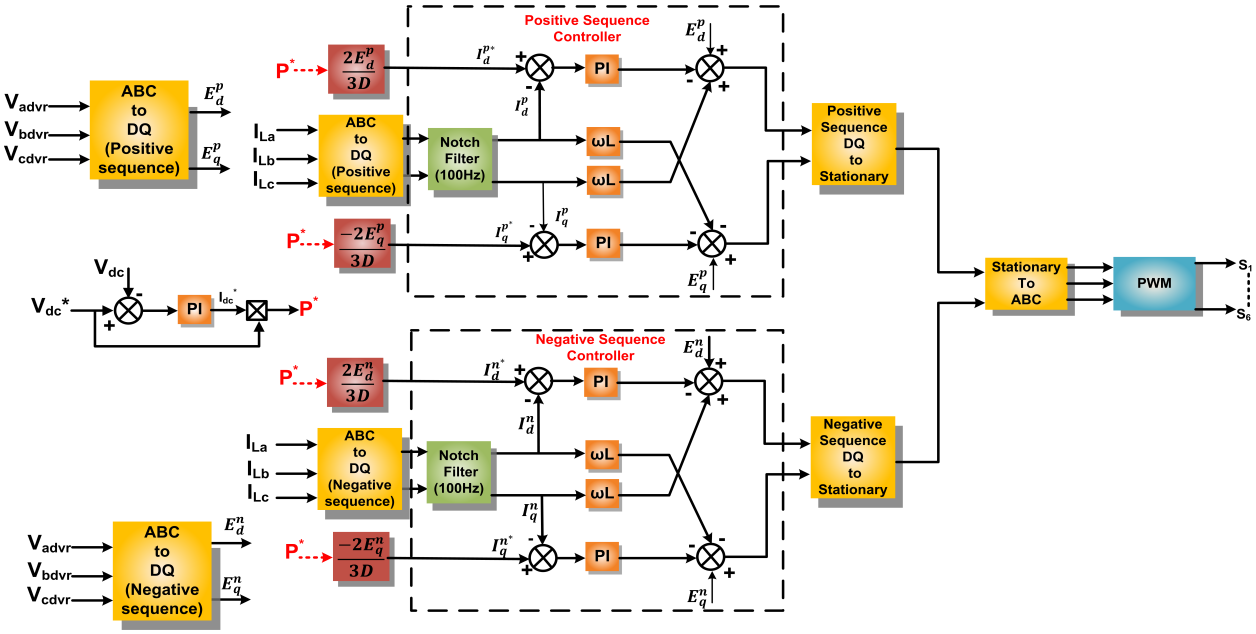


Figure 7.9: Control scheme of the PWM dual controller based series converter for the rectification mode

$$\begin{bmatrix} I_d^p(t) \\ I_q^p(t) \\ I_d^n(t) \\ I_q^n(t) \end{bmatrix} = \frac{2P_0}{3D} \begin{bmatrix} E_d^p \\ E_q^p \\ -E_d^n \\ -E_q^n \end{bmatrix} \tag{7.6}$$

where $D = \left[\left(E_d^{p2}\right) + \left(E_q^{p2}\right)\right] - \left[\left(E_d^{n2}\right) + \left(E_q^{n2}\right)\right]$ and $D \neq 0$.

Figure 7.9 shows the control scheme of the PWM dual controller based series converter for the rectification mode. This independent control strategy allows to regulate the real power completely, thus achieving the constant dc-link voltage.

7.4.3 Control of series converter for power transfer capability improvement

The series converter can control the distribution line real and reactive power flow simultaneously (Gyugyi, 1992). To do so, the series converter injected voltage is decomposed into dq components using Park's transformation. The d-axis component in quadrature with the bus voltage controls the line reactive power flow. The q-axis component in phase with the bus voltage regulates the transmission line real power

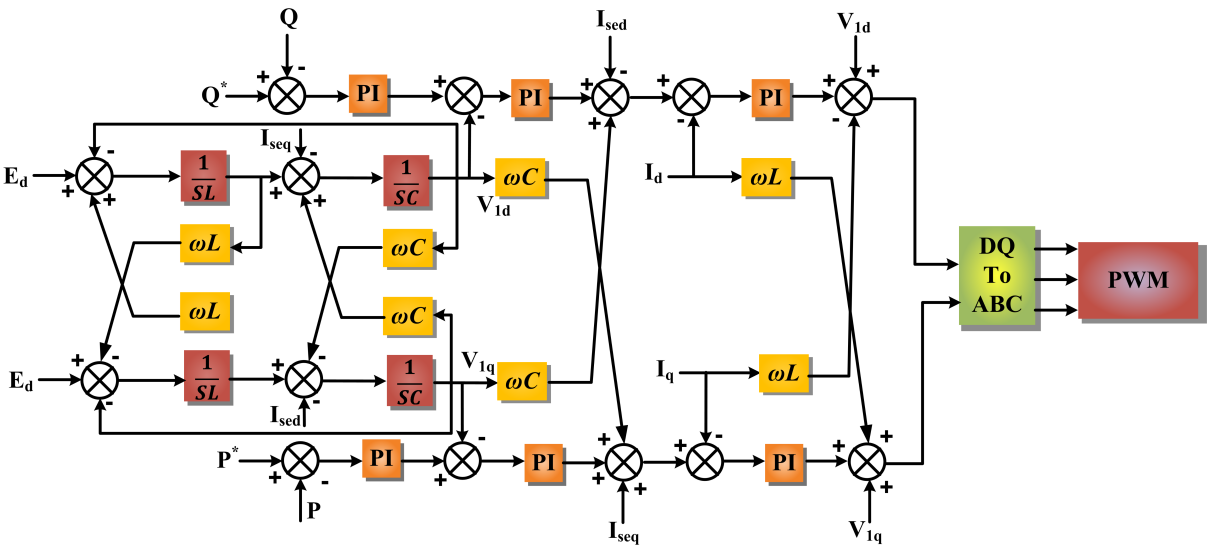


Figure 7.10: Control scheme of cross-coupling controller for power transfer capability improvement

flow. Considering the variation of the parameters of the transmission line, a cross-coupling controller.which is more robust is implemented for this converter. The block diagram of control scheme of series converter is shown in Figure 7.10.

The whole control system is composed of three loops, outer power loop, the voltage in middle and the current as inner loop. Every loop includes the corresponding state feedback decoupling terms. The control scheme can eliminate the inference which exists in voltage and current between the dq axis. With appropriate design of the control system, the real and reactive power flow (P,Q) in the line can respond to fast changes of the real power reference P^* and the reactive power reference Q^* and reach the desired values. The series transformer is used to inject an independently controlled voltage in quadrature with the line current for the purpose of increasing or decreasing the overall voltage drop across the line and thereby controlling the transmitted power.

7.5 Simulation results and discussion

In this section simulation results of operating modes discussed earlier for series interfacing converter in hybrid AC/DC microgrid is presented. A model of series converter is developed in PSCAD/EMTDC to carry out simulation studies. An AC source of

410 V (L-L) modelled as utility supply is connected to the ac loads. A series interlinking converter is used to interface the dc microgrid to the utility using series transformer. The dc microgrid is modelled as a dc source connected with dc loads. The dc source can be considered as solar PV output. A bypass switch is connected across the windings of the series transformer. This switch will be responsible to short circuit the series transformer winding, whenever operation of converter is not needed. A LC filter is connected in legs of windings of the transformer for power conditioning purpose. The parameters used for the simulation are specified in Table 7.1. The circuit diagram of the simulation model is shown in Figure 7.3

Table 7.1: Simulation parameters

Device	Description	Value
Supply	ACVoltage (LL rms)	410 V
	Frequency	50Hz
	Supply impedance(Zs)	0.5 Ω
AC Load(Star)	Resistance	170 Ω
Inveter	Switching Frequency	2950 Hz
	DC link Voltage	120 V
Filter	Capacitance(Cf)	70 μF
	Inductance	739 μH
Injection Transformer(per phase)	Rated Power (Star)	10 kVA
	Primary voltage(V1)(LL)	200 V
	Secondary voltage(V2)	200 V
DC Loads	Resistance	120 Ω
	Power	120 W

A dc microgrid of 120 V bus voltage is connected to the utility supply of 410 V (L-L rms) using a series interlinking converter is modelled in PSCAD/EMTDC to carryout simulation studies. The control of the converter is modelled to perform various operations such as rectification of downstream and upstream faults, power sharing between the utility and the dc microgrid etc. The state diagram of the modes of operation of the series converter is shown in Figure 7.11.

7.5.1 Mode 1:Operation during upstream faults

The upstream faults consist of balanced and unbalanced voltage sags at utility side. A CDSC filter based modified DVC algorithm is implemented for DVR control using series converter in this mode. The converter is operated whenever the source voltages experiences sag greater than 10 %. So, we can infer that the threshold limit for the

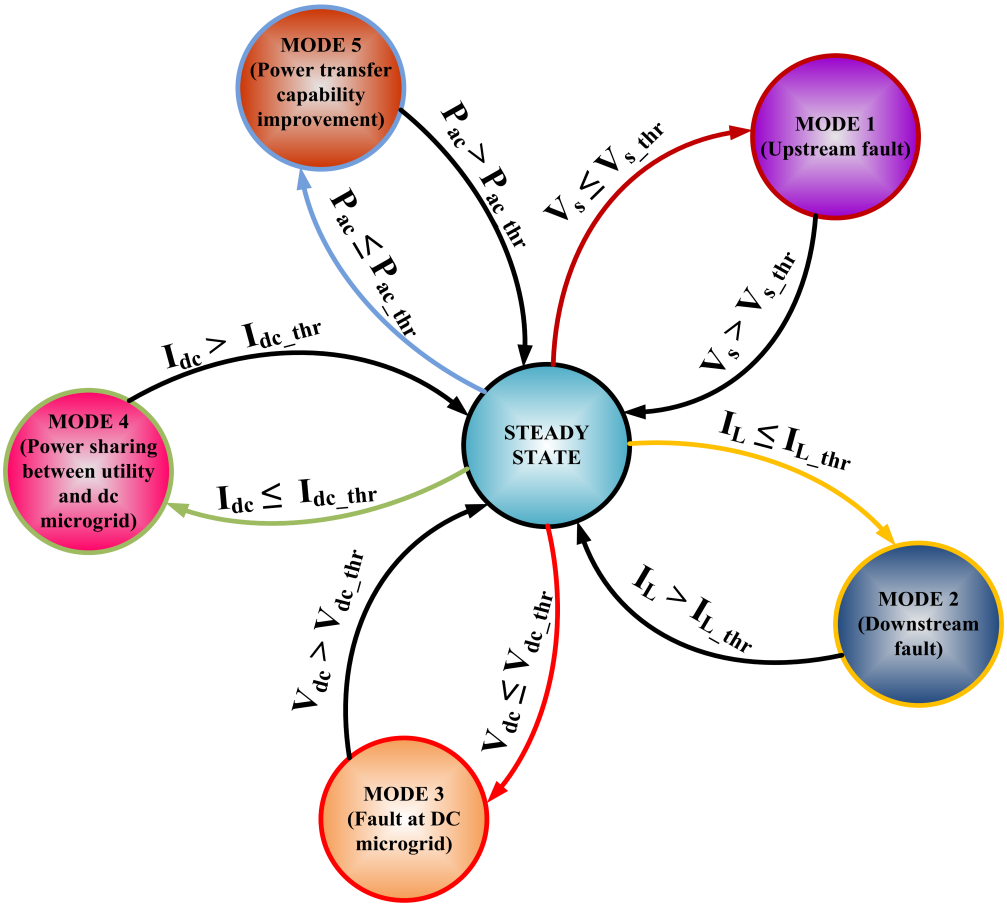


Figure 7.11: State diagram of the modes of operation of the series converter

converter to operate in this mode is 90 % of the source voltage magnitude. The cases discussed for this mode are given below:

- ***Case I***: A symmetric voltage sag of depth 15 % is generated at t=0.3s for a period of 0.5s. Once the voltage sag occurs, DVR control detects it and generates switching pulses to the VSI to compensate for the voltage dip. As it is a symmetric voltage sag, DVR injects balanced three phase voltages (positive sequence voltages) and restores the load voltage to reference value. The waveform of the source voltage and injected voltage are shown in Figure 7.12(a). The balanced three phase voltage injected by DVR can be observed in Figure 7.12(a).

- ***Case II***:A two phase to ground fault initiated at 0.3s leads to a voltage dip

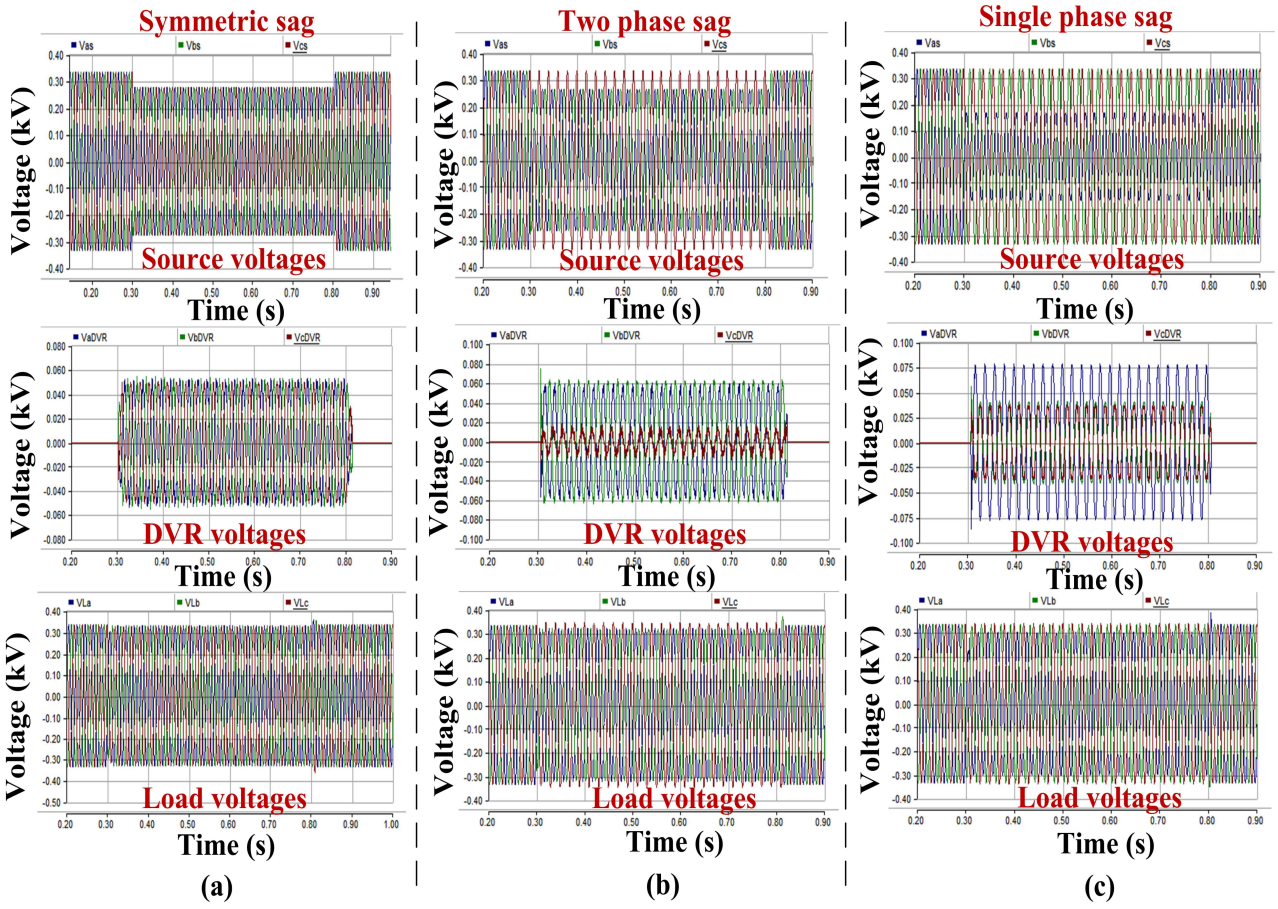


Figure 7.12: Source, DVR and load voltages under (a) symmetric sag (b) Two phase sag (c) single phase sag

of 15 % in phase-a and phase-b, which lasts for a period of 0.5s till the fault is cleared at 0.8s; whereas the voltage in phase-c remains unaffected. Figure 7.12(b) shows the performance of the control algorithm is unaffected even in the presence of unbalance voltage sags as DVR injects both positive and negative sequence voltages and restores the load voltage to its reference value.

- ***Case III***:A single phase voltage sag of 15% depth is generated at 0.3s in phase-a of source voltage for a duration of 0.5s. DVR maintains the load voltage at its reference value by injecting voltage in series with the source as shown in Figure 7.12(c).

For the balanced and unbalanced voltage sags given in cases I, II and III, it can be observed that the moment voltage sag occurs, sag detection algorithm detects

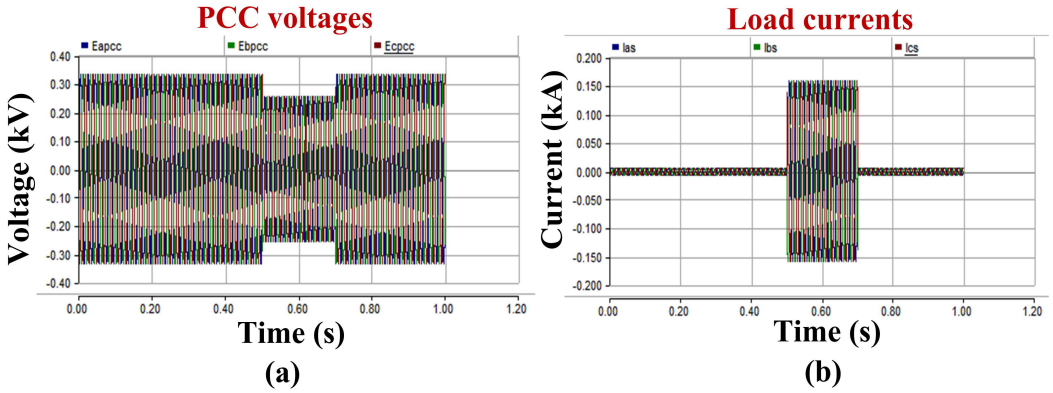


Figure 7.13: Simulation results for three-phase short circuit fault with DVR bypassed: (a) PCC voltage (b) load currents

dip in the voltage accurately. CDSC PLL extracts the symmetrical components of grid voltages, which are used to generate reference voltages to be injected. Further positive and negative sequence voltages are injected by DVR so that constant voltage is maintained across the load during balanced and unbalanced grid voltage conditions.

7.5.2 Mode 2: Operation during downstream faults

The downstream faults refers to the faults which occur at load side. The three phases of load are short circuited from 0.5s to 0.7s. The downstream fault causes extremely high currents due to very limited source and line impedance. The simulation is run for a symmetrical downstream fault. Figure 7.13 (a) & (b) shows the load current and PCC voltages, with the series converter is bypassed. These large fault currents might cause damaging effects within a few cycles. The PCC voltages shown in Figure 7.13(a) drops to 78%. It is obvious that downstream fault causes extremely high currents (150 A) as shown in Figure 7.13(b) due to the very low source and line impedance.

The threshold value for current in this mode is chosen to be 5 times the magnitude of the load current. Whenever the load current violates the limit, the converter is operated in mode-2. The system voltage and currents with DVR actively controlled by virtual impedance based FCL during fault are shown in Figure 7.14. As expected, the PCC voltages are restored which can be seen from Figure 7.14(d), by limiting the fault currents (approx. 20 A). Figure 7.14(a),(b) & (c) shows the load voltages, load currents and DVR voltages respectively. Therefore, the loads on parallel feeders connected to PCC will not be affected. The introduction of large impedance into

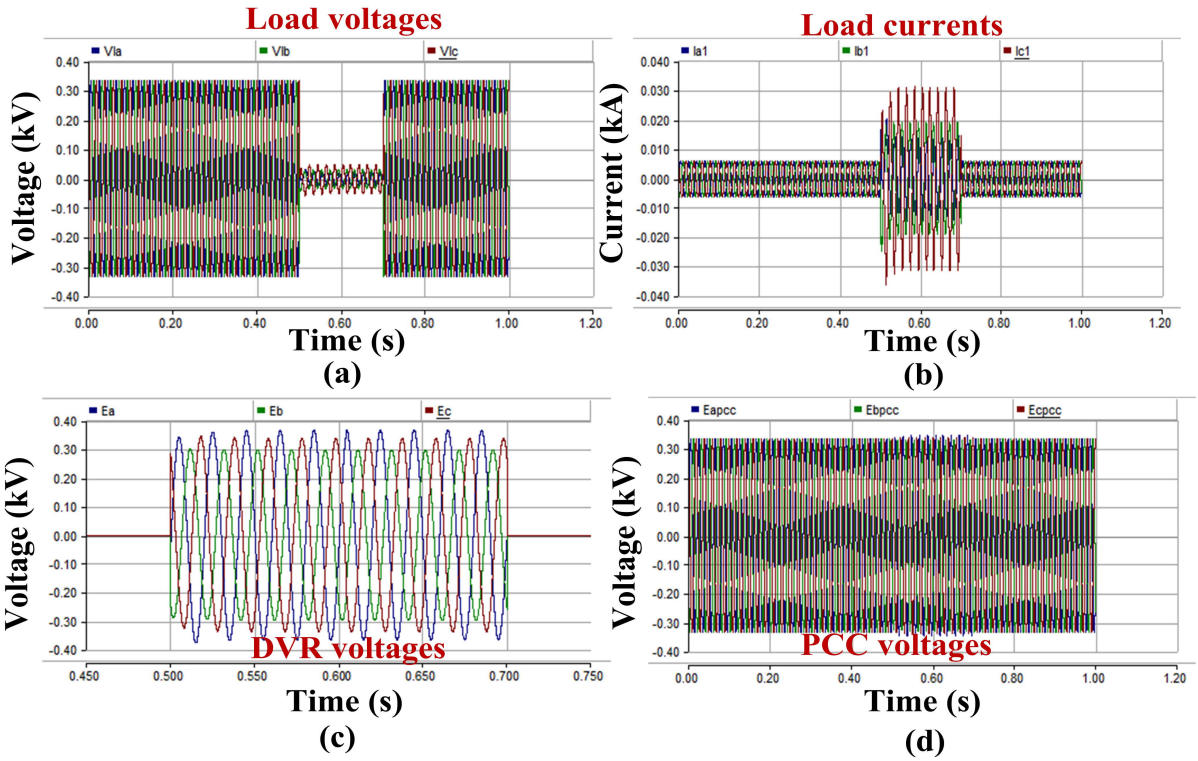


Figure 7.14: Simulation results of DVR acting as FCL during three phase short circuit fault: (a) Load voltages (b) load currents (c) DVR voltages (d) PCC voltages

the system by the series converter limits the fault current magnitude effectively. The fault current limiting control of series converter has the ability to quickly measure the system current and voltage to instantaneously take action, such as to shut down its power control systems to meet the requirement of functioning of fault current limiting algorithm.

7.5.3 Mode 3: Operation during fault at dc microgrid side

The dc microgrid is modelled as 120 V dc source with dc loads of 120 W power rating in PSCAD/EMTDC. The fault at dc microgrid side is created by opening the circuit breaker at the dc source side at t=3s for the time duration of 3s. Due to this fault at dc source side, the voltage across the dc loads starts to drop to 10 V due to the discharge of the dc link capacitor. Figure 7.15(a) shows the dc link voltage at the microgrid side. The rate of decrease of voltage across the loads during fault depends

on the time constant of the capacitor of the dc link used along with the dc loads. The threshold value for this mode is chosen to be 90 % of the magnitude of dc link capacitor voltage. Whenever the dc link voltage magnitude goes below this limit, the converter is operated in mode-3. During the interval of fault, the interlinking converter will operate in mode 3 to keep the dc link voltage to the reference value.

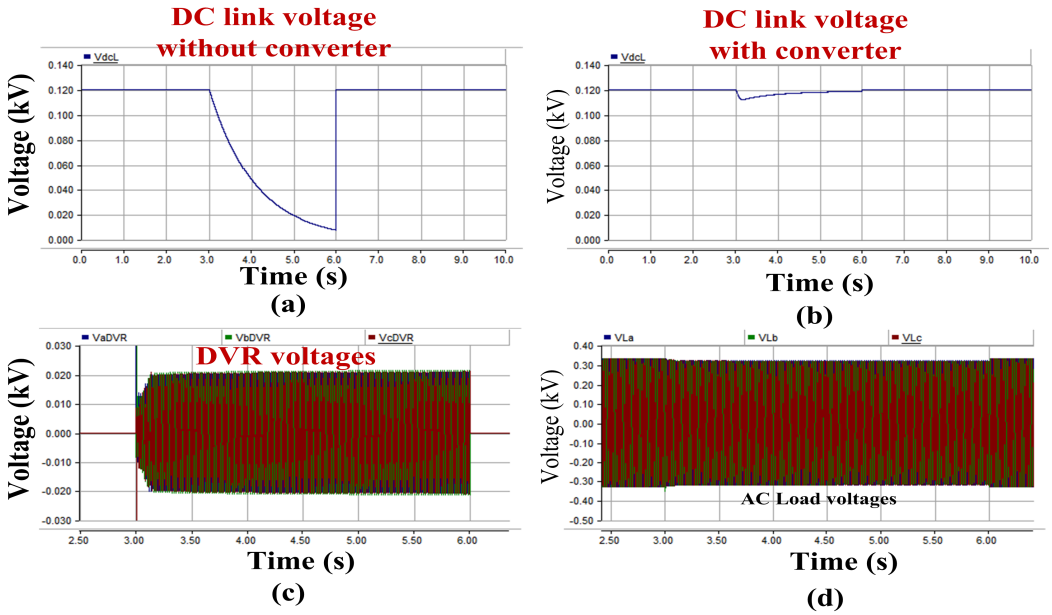


Figure 7.15: Simulation results for operation of series converter during fault at dc microgrid side: (a), (b) DC link voltage with and without converter operation (c) DVR voltage during converter operation (d) AC load voltage experiences a dip of 4 % during converter operation

Figure 7.15(b) shows the dc link voltage across the capacitor during the operation of inter linking converter in mode-3. It can be observed that the voltage is maintained close to 120 V for the duration of fault. Figure 7.15(c) shows the DVR voltage which is drawn from the utility end to supplement the voltage across the dc link capacitor via inter linking converter. Figure 7.15(d) shows a dip in voltage across ac loads (4%). This dip is caused by the converter operation during mode-3. So, for the duration of the fault, the dc loads are getting power supply from the utility via interlinking converter.

7.5.4 Mode 4: Power sharing between utility and dc microgrid

The converter is operated in mode-4 when there is deficit of power at dc microgrid and surplus power at the utility side. This surplus power can be supplied to the dc microgrid whenever there is deficit of power during operation of dc loads at peak hours. Figure 7.16(a) shows the dc link voltage maintained across the capacitor at 120 V. The dc source is supplying the power to the loads connected across dc bus. The threshold value considered for this mode is 90% of the magnitude of dc source current. Whenever the dc source current magnitude goes below this limit, the converter is operated in mode-4. Figure 7.16(b) shows the IC voltage which is drawn from the utility end to supply dc power to the microgrid. Figure 7.16(c) shows the dc source current during converter operation in mode-4. Figure 7.16(d) shows the dc current supplied from utility via converter during its operation in mode-4. From Figure 7.16(c) & (d), it can be observed that during the converter operation in mode-4, the dc source current starts to decrease from 1 A to 0.8 A and the current supplied from the utility via interlinking converter starts to increase from 0 to 0.2 A.

The dc loads are rated for 120 W at 120 V and consumes a dc current of 1 A. So, during operation of the converter in mode-4, the dc loads are supplied by 0.8 A current from dc source and 0.2 A current is provided from utility via converter.

7.5.5 Mode 5: Active power transfer capability improvement

The converter is operated in mode-5 when there is deficit of power at AC loads. Though in simulation utility grid alone is considered but in practical other AC subgrids are connected to the AC utility grid. A practical situation is emulated where there is power deficit from AC subgrids due to sudden increase in loads. This mode helps in increasing the active power which is being transferred from the utility side to the ac loads.From Figure 7.17(a), we can see that the utility is supplying 3860 W to the ac loads. Now, at t = 2s, the converter is operated to increase the power flow to the ac loads. The flow of active power is increased to 4090 W from t = 2s. So, it can be inferred that due to this operation the converter increased the active power flow capability from the source to the loads by 230 W. Figure 7.17(b) shows the injected voltage by the converter to supplement the power flow to the ac loads. Figure 7.17(c) & (d) shows the load voltages and load currents before and after the

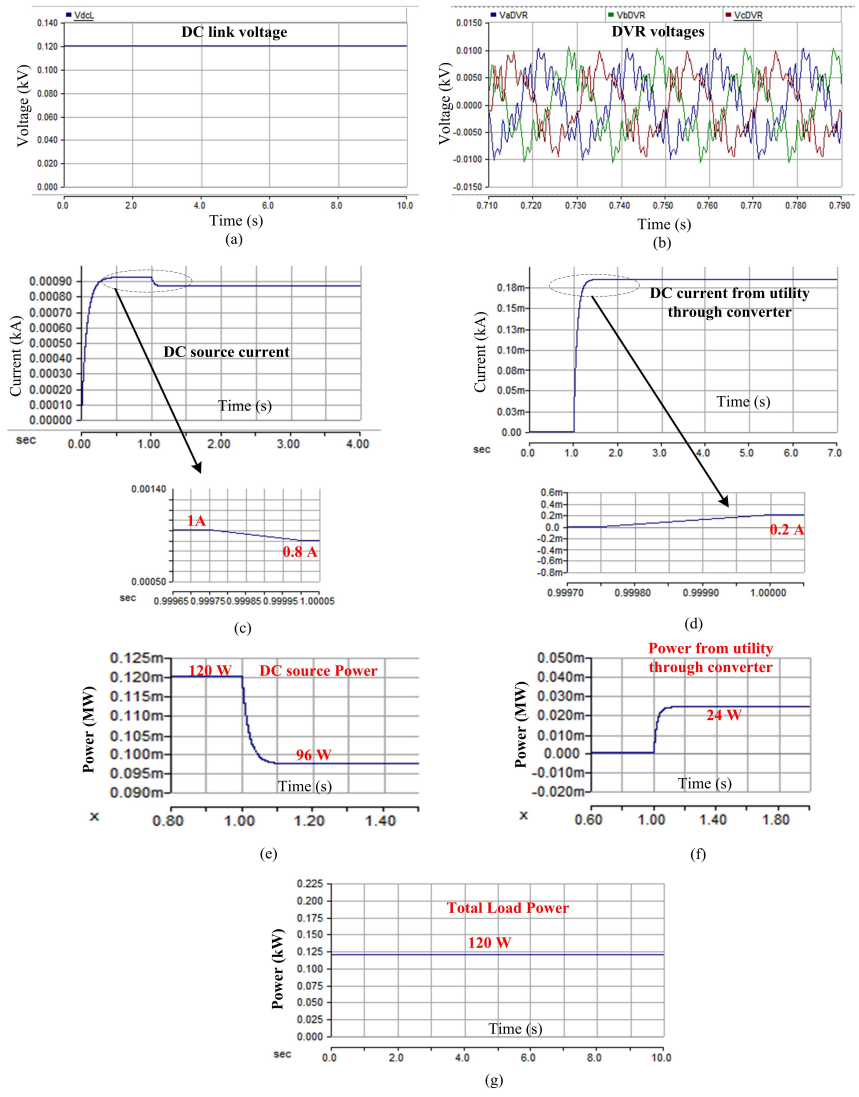


Figure 7.16: Simulation results for power sharing operation of series converter: (a) DC link voltage (b) DVR voltages during converter operation (c) Reduction in DC source current from 1 A to 0.8 A during converter operation (d) DC current supplied from utility via converter increased from 0 A to 0.2 A during its operation

operation of the converter. It can be noticed that the load voltages experiences a increase in magnitude of 4.5% when the converter is operated in this mode.

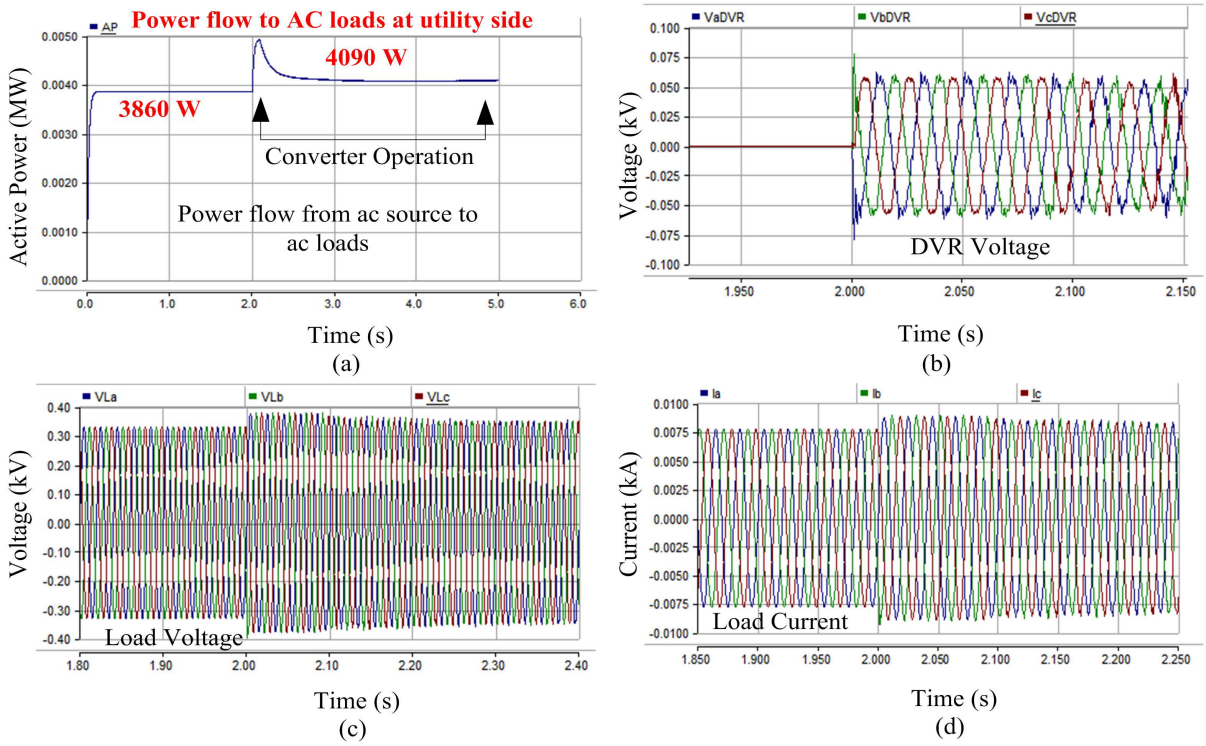


Figure 7.17: Simulation results for increasing power transfer: (a) Active power flow from utility to ac loads increased from 3860 W to 4090 W (b) DVR voltages during operation of converter (c) Load voltages (d) Load currents

7.6 Bi-directional operation of the series converter

The proposed series converter is capable of operating in bidirectional mode. This implies that the converter can transfer power from the utility to dc microgrid as well as reverse the power flow from the dc microgrid to the utility. Figure 7.18(a) shows the power flow measured from the legs of the converter which connects it to the utility through series transformer. From t =0s to t =2s, the converter is operated in mode-3, the power flow through the legs of the converter is 70 W. From t =2s to t =5s, the converter is operated in mode-5, the power flow through the leg of the converter is -70 W. The negative sign indicates the reversal of current in the leg of the converter, hence implies the bidirectional operation of the converter. Figure 7.18(b) shows the power flow from the utility to the ac loads during the two modes. During mode-3, the power flow to the ac loads is decreased to 3600 W, as the utility supply is also responsible for supplying power to the dc microgrid. During mode-5, the power

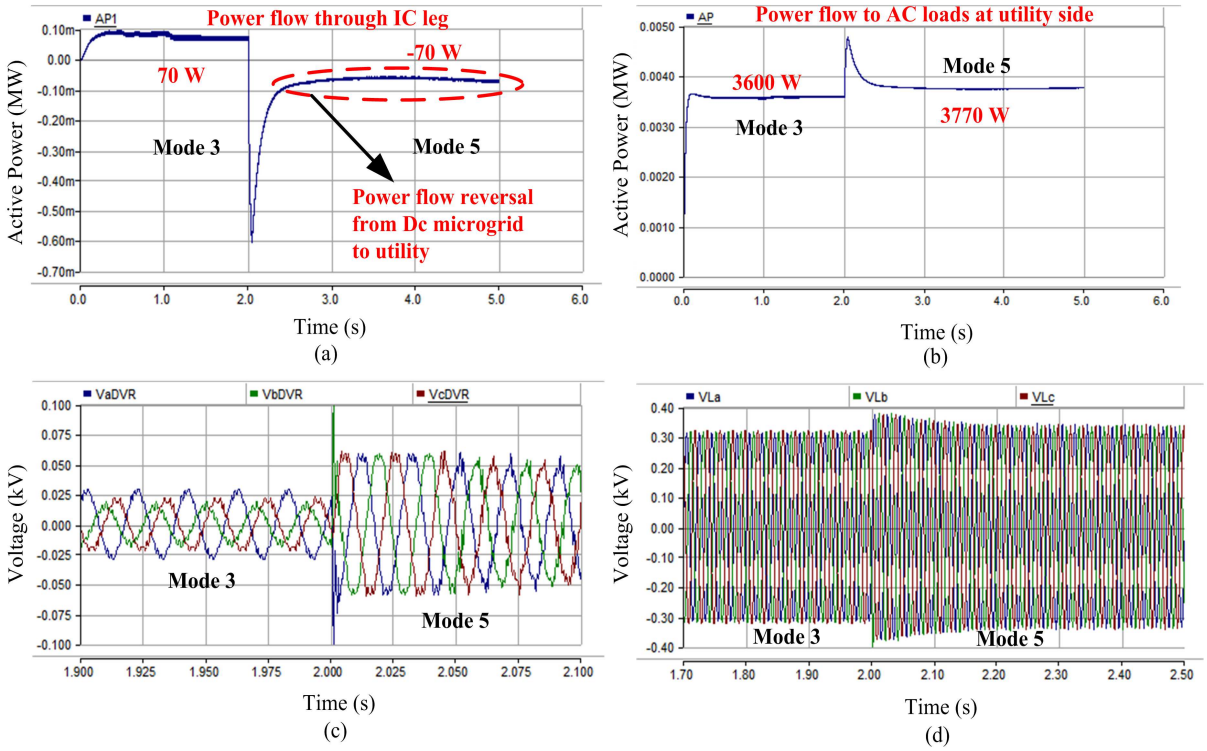


Figure 7.18: Bidirectional operation of series converter (a) Active power flow through legs of the converter during bidirectional operation of the converter (b) Active power flow from utility to the ac loads (c) DVR voltages (d) Load voltages

supplied to the ac loads is 3770 W. Figure 7.18(c) & (d) shows the DVR voltages and the load voltages during the two modes of operation. During mode-3, the load voltages experience a dip of 3%, whose cause of occurrence has been discussed before. During mode-5, the load voltages experience a swell of 1.5% which is due to increase in flow of active power to the loads.

7.7 Conclusion

Thus, in this chapter, control algorithm of series converter having a CDSC filter based modified DVC with with positive and negative sequence controllers is presented for DVR operation and control. The proposed control is robust to grid voltage harmonics and restores the grid voltages to their nominal voltages under all the test conditions. Further VI-based DFCL limits the fault current significantly to protect the system

from downstream faults. On the other hand, control algorithm for series converter based PWM rectification mode is also discussed. This scheme provides complete dc voltage regulation without risking the system to instability. The control scheme proposed for increasing power transfer capability is capable of removing interference in voltage and current between d-axis and q-axis. Finally, the simulation results of the various modes of operation of the proposed series converter are discussed. The converter is able to operate in five different modes subjected to certain conditions. The operation of bidirectional power flow can be used to transfer power from the utility to the dc microgrid and vice-versa.

Chapter 8

Conclusions and suggestions for Future work

Contents

Power Quality has become a serious concern with deregulation of energy markets and increased use of non-linear loads. Automation and process control industries such as chemical, petroleum and paper industries which are highly sensitive and affected due to power quality problems. Among all the power quality issues voltage related problems occupy a major portion and a series interfacing converter is considered to be cost effective solution to compensate the voltage related PQ isues.

In present thesis work investigation of control strategies for multimode operation of series converter is presented. The investigation ranges from operating series converter as custom power device to mitigate upstream and downstream faults in distribution system and also as interlinking converter in hybrid microgrid for power management and voltage (AC/DC) control.

8.1 Summary of the thesis

In chapter-1 a broad view of power quality scenario in the present electric system is presented which motivated to carry out the present thesis work to mitigate those issues. The description of multimode operation of series converter is presented in chapter-2. In this regard different control strategies developed in literature are discussed in chapter-2. Firstly the different control stategies for operating series converter (DVR) in distribution system to compensate voltage disturbances viz., sag, swell and harmonics is discussed. Further in the process of compensation detection of grid phase angle plays crucial role. Thus different PLL's proposed in the literature are studied then CDSC based PLL is chosen as it proves to be superior in terms of harmonic elimination ability, transient response, frequency adaptability. In addition to that control strategies for operating series converter (DVR) as FCL are discussed to reduce the magnitude of fault current and to maintain the PCC voltage at prefault level. Finally, different type's of interlinking converters which links the AC and DC microgrid are discused.

Basic representation of harmonics in different schemes are presented in chapter-3 then followed by basic operating principle of PLL and conventional SRF-PLL. The problems related to the conventional SRF-PLL operation during distorted grid conditions are discussed and to overcome these issues this chapter introduces the concept of dual role CDSC as PLL prefilter for grid phase detection and as extractor (selective harmonic elimination) for load voltage compensation. It is observed that the performance of CDSC based PLL is better compared to other contemporaries viz., DSOGI-PLL, DSC-PLL. The main feature of CDSC-PLL that outsights the other is its effectiveness in filtering out the symmetric and asymmetric harmonics. Thus in this thesis CDSC based prefilter is chosen for effective reference generation and control of DVR. Further on the other side this chapter also discuss about the design of extractor based on the modified CDSC strategy to achieve harmonic mitigation of load voltage. Thus the name dual role CDSC refers to the generation of fundamental component (from CDSC prefilter, positive and negative sequence controller) plus non-fundamental component (extractor) of the compensation voltage.

To utilise the DVR effectively the control aspect plays an important role. In open-loop control of DVR there are issues related to stability and also yields poor transient response. Further the open-loop control of DVR produces a steady state error while

tracking the DVR reference voltages. Considering aforementioned issues the chapter-4 discuss about the closed loop control of CDSC-PLL based DVR to compensate asymmetric voltage sags and harmonics. Thus in this chapter a multi-loop control based on modified DVC algorithm for DVR is presented. For this a mathematical model of DVR in dq frame is derived then dual role CDSC based DVC algorithm is explained. In the second part of the chapter performance analysis of proposed dual role CDSC based DVC control of DVR under distorted grid conditions viz., symmetrical and asymmetrical voltage sags, voltage harmonics through simulation and experimental studies are presented.

ISC of the grid voltages were obtained using a CDSC prefilter, which is customized to filter out symmetric and asymmetric voltage harmonics. In chapter-5 CDSC-based DVC algorithm with positive and negative sequence controllers in the dq frame track the DVR reference voltages. The proposed control scheme is implemented in FPGA digital controller and its performance is evaluated under symmetric and asymmetric voltage sags and harmonics. The experimental results states that load voltage THD was reduced to 3.0% (from 14.1%) in asymmetric harmonic case and to 2.1% (from 17.1%) in symmetric harmonics case by adding an extractor based on the modified CDSC strategy to the control algorithm which is designed to extract the dominant lower order harmonics from the load voltage.

In the structure of modified DVC algorithm conventional P controller is employed in the voltage control loop. In Chapter-5 a pseudo derivative feedback based voltage controller is developed for DVR to improve the compensation of voltage events. Prior to the design aspects of PDF control the chapter presents basic multiloop control schemes with conventional P and PI controller. Then the design of PDF controller is discussed. In this chapter for tuning the gains of the controller an extended root locus technique is discussed. A comparative analysis of performance parameters are carried out between PDF and existing controllers (P and PI) through simulation studies. It is found that P controller has slightly similar time response as PDF. However, the stability margin of the P controller is very less thereby any small variation on the parameter leads to the instability of the system. The relative stability of PI controller is better compared to P controller but its sluggish dynamic response increases the overall settling time and undershoot in load voltage and thereby degrades its performance. The PDF controller has better dynamic response as compared to PI with decent relative stability. Finally, the efficacy of proposed controller is verified by

adopting MV-DVR system through simulations (PSCAD) and experimental studies on low voltage laboratory prototype DVR. From the experimental results it is found that during symmetrical and asymmetrical voltage sags the proposed PDF based voltage control of DVR exhibits a less undershoot of 12.7% & 10.6 % respectively which is very less compared to other controllers (P and PI).

So far the series converter (DVR) operation during upstream faults is discussed i.e., compensation of voltage sags, swells and harmonics. In Chapter-6 the operation of series converter (DVR) during downstream faults is presented. Firstly the operation of flux-charge based fault current limiting (FCL) is discussed along with its short comings during its operation under downstream fault. It is observed that the pure integration of flux during three phase fault leads to saturated condition as the rate of integration is very less. Thus, to avoid this problem, a virtual impedance based fault current limiter is proposed for DVR to protect the PCC voltages during the downstream faults. The chapter deals with design aspects of the virtual impedance parameter is in detail. Meanwhile, the simulation studies are carried out for both symmetric and asymmetric faults to test the efficacy of the proposed VI based FCL. The results demonstrate that by using the proposed VI-DFCL the fault currents are limited to 52 A (at the secondary side of the transformer which is only 1.6 times the rated line current) compared to 1 kA when VI-DFCL based control of DVR is bypassed which proves the efficacy of the proposed VI-DFCL control algorithm for DVR.

In addition to that the Chapter-6 also deals with transformerless topology of series converter (TDVR). In conventional series converter (DVR) there are several issues namely, cost, weight, and losses related with the series injection transformer which constraints its applications to heavy area. To overcome these limitations of the conventional DVR, a transformerless series converter (TDVR) scheme with reduced cost, weight, size, and losses has been proposed in the literature. In this chapter a Uncertainty and Disturbance Estimator (UDE) control scheme is employed for TDVR to maintain load voltage at a constant value during voltage disturbance viz., sag and swells. The modelling of TDVR system is discussed and the description of proposed controller is explained. The proposed controller includes one differential feedforward term, model inversion to cancel known model dynamics and PI regulator to compensate the tracking error between the reference state vector and the actual state vector. The system is validated through simulation and experimental studies.

In Chpater-7 the operation of series converter as interlinking converter in hybrid microgrid is analysed. The interlinking converter plays important role in achieving the desired operating features of hybrid microgrid. Thus in this chapter different control schemes are discussed for operating the series converter in different modes to achieve the desired features viz., AC/DC bus voltage control, fault control and power management. All these features are segregated as five modes in this chapter. A model of series converter is developed in PSCAD/EMTDC to carry out simulation studies. A source of 410 V (L-L) modelled as utility supply is connected to the ac loads. A series interlinking converter is used to interface the dc microgrid to the utility using series transformer. The simulation results proves that the adopted control strategy can effectively manage the IC to operate bidirectionally and regulate the power exchange between dc and ac subgrids, when the operating condition changes. It was further shown that the dc subgrid voltage has been controlled in an effective manner during transients i.e., fault at dc subgird. Thus with the proposed multi-functional IC additional functions to the hybrid microgrid are achieved apart from the primary function of power flow management using single converter.

8.2 Future Scope

The future scope of the present thesis is as follows:

8.2.1 Series converter as custom power device (DVR)

- The present work can be extended with energy storage based DVR's especially from renewable sources (viz., solar and wind) with effective control strategies.

- Further investigation of DVR topologies viz., interline DVR (IDVR) for compensation of voltage sag in economic point of view is needed.

- Investigation of Artificial Neural Network (ANN) and Adaptive Neutral Fuzzy Inference System (ANFIS) based controllers for DVR to increase the dynamic performance in mitigating voltage disturbances.

8.2.2 Series converter as interlinking converter

- Exploration of differfent IC topologies viz., effective three port ICs for interfacing ac subgrid, dc subgrid, and main grid.
- IC sizing design can be investigated taking into account data related to critical loads, stochastic generation and the amount of storage available in respective subgrids.
- Newer IC control strategies should be investigated, for example, on the lines of synchronverters (Zhong and Weiss, 2011) to enhance the dynamic response of the HMG.

Appendix A

Hardware Implementation

A.1 Introduction

This chapter deals with development of low voltage laboratory prototype DVR system. The laboratory prototype is built with help of Altera cyclone-II FPGA controller using Quartus GUI. Apart from this, design and development of PCBs for voltage and scaling circuit are presented in this chapter. The laboratory prototype consists of power module and control unit. The details for development of the power module and control unit are also presented in this chapter.

A.2 Experimental setup

A scaled down 100 V low voltage DVR prototype is developed to conduct experimental studies. Hardware configuration of the three phase DVR prototype is shown in Figure A.1. The proposed control algorithm for DVR to compensate the upstream faults is implemented in Altera cyclone-II FPGA controller using Quartus GUI. The supply voltage of 100V (rms) is provided by a three-phase autotransformer which is used to generate balanced voltage sags. For generating unbalanced voltage sags three single phase transformers are employed. A semikron made VSI is used to generate voltage required for compensation. The output of the VSI is connected to a 1:1 injection transformer which is installed in series with source and resistive load. The DC link of the VSI is powered by an auxiliary supply. A 70 μF capacitor filter is placed on the secondary side of the injection transformer to filter out higher order harmonics from

DVR injected voltages. The experimental parameters are tabulated in Table A.1.

Table A.1: Experimental setup parametrs

Device	Description	Value
Source	ACVoltage (phase voltage rms)	100 V
	Frequency	50 Hz
Load(Star)	Resistance	20 Ω, 5 A
Inveter	Switching Frequency	5 kHz
	DC link Voltage	200 V
Filter	Capacitance	70 μF
	Inductance	720 μH
Injection Transformer(per phase)	Tuns ratio	1 : 1
	Primary voltage	230 V
	Secondary voltage	230 V

A.2.1 Power circuit

- **Source and load:** A three-phase autotransformer is used as voltage source to supply power to the resistive load. Balanced voltage sags are generated by reducing the voltage manually. For generating unbalanced voltage sags, three single phase auto transformers are used. Rheostats of 165 Ω, 3 A (2no.) connected in parallel per phase (which constitutes 121 W) whose voltage should be kept constant by DVR. Ratings of autotransformer are given in table A.2.

Table A.2: Three phase auto transformer parameters

Description		Rating
Voltage	Input	415 V
	Output	0-415 V
Output Current		28 A
Capacity		10 kVA
Phase		3ϕ
Frequency		50 Hz

- **Power Converter:** A semikron make VSI is used to generates the voltage and power required for compensating voltage sags. Each phase of the three phase VSI has 2 IGBTs with a parallel connected diode. The input of the VSI has a DC link powered by a 3 phase uncontrolled rectifier and the DC link is provided with a two 4700 μF connected in series to maintain constant voltage. A Skyper 32R gate drive is provided to interface control circuit with the power circuit. The gate driver requires a +15 V which is provided by a 15 V, 5 A DC supply. The gate driver circuit also provides an interlocking time of 3 s and it is capable of operating inverter at a frequency of 20 kHz. The ratings of the power converter are given Table A.3.

Figure A.1: Block diagram of experimental setup

Table A.3: VSI parameters

Description	Rating
AC input voltage	415 V
DC output voltage	600 V
AC output current	30 A
Switching frequency	20 kHz

- **Injection Transformer:** A 1:1 injection transformer is used for injecting VSI generated ac voltages in series with the source and load. The specifications of injection transformer are given in Table A.4.

Table A.4: Injection transformer parameters

Description	Rating
Voltage	300 V/300 V
Current	19.25 A/19.25 A
Capacity	10 kVA
Inductance	720 μH
Turns ratio	1:1
Phase	3
Frequency	50 Hz

- **LC Filter:** The filter is inserted to damp the switching harmonics generated by the PWM control of voltage source converter. These harmonics are usually eliminated by a passive low pass filter consisting of inductor and a capacitor. The injection transformer has an inductance of $720\mu H$. Hence no separate inductor filter is used to suppress current harmonics. The capacitor is usually placed at the inverter output to eliminate voltage harmonics from the DVR voltages. Instead the capacitors are placed at the secondary side of the injection transformer as the transformer itself carries out the inductive action. The capacitance values are fixed to give a cut-off frequency of 708 Hz (the value corresponds to harmonic order upto n=15) . Hence a standard value of $7055\mu F$ is chosen.

A.2.2 Control circuit:

The proposed algorithm to control VSI of DVR can be implemented either by analog or digital controllers. Usually analog controllers are preferred for systems with low level of complexity where the control algorithm is emulated by using OPAMPs, passive elements like resistors and capacitors. Even though analog systems are immune to noise it becomes difficult to implement control algorithms for complex systems. Hence Digital Controllers are preferred for implementation of complex control as they are

flexible and easier to implement. Digital control of power electronic devices can be achieved by using Micro controllers, Digital Signal Processors (DSP), Application Specic Integrated Circuits (ASICS), or Field Programmable Gate Arrays (FPGA). Altera Cyclone-II FPGA (EP2C70F672C8) is chosen for implementation of control algorithms.

- **FPGA controller board:** The block of the FPGA digital platform is shown in Figure A.2. The Cyclone-II FPGA is interfaced with peripherals such as a conguration device (EEPROM), physical interfacing devices such as Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), digital I/Os which are dedicated I/O pins of the FPGA device and USB device.

  a) **Power Supply:** The FPGA board requires analog and digital power supplies for its operation. It is provided with a custom-made DC supply which can generates two different voltage levels +5 V and +12 V required for operation of FPGA and its peripherals.

  b) **Clock:** FPGA is provided with a clock frequency of 20MHz

  c) **ADC:** For implementation of control algorithm the sensed voltage and current signals should be interfaced with the FPGA. Four onboard 12-bit 4-channel bipolar ADCs (AD7864) with a conversion time of 1.65 μs per channel, are used to convert analog signals to digital and the digital output of the ADC is interfaced with the FPGA.

  d) **DAC:** Four 12-bit 2-channel DACs (DAC5447) are interfaced with Cyclone-II FPGA to convert digital signals to analog for measurement and recording purpose. Output analog voltages are of the range -2.5 V to 2.5 V.

  e) **Digital I/O:** A total of 80 digital I/O pins are provided for the FPGA of which 56 pins are available for the user. These pins are useful to generate digital signals such as PWM pulses for the inverter. The output voltage of these pins is at +5 V level.

  f) **DPSRAM:** A Synchronous Dual-Port SRAM CY7C09389V with memory of 64Kx18 is interfaced with FPGA. It consists of two ports which gives access to simultaneously read and write from any location in the memory. This is useful especially for storing the data or to perform operation like signal delay which is needed in case of a CDSC filter.

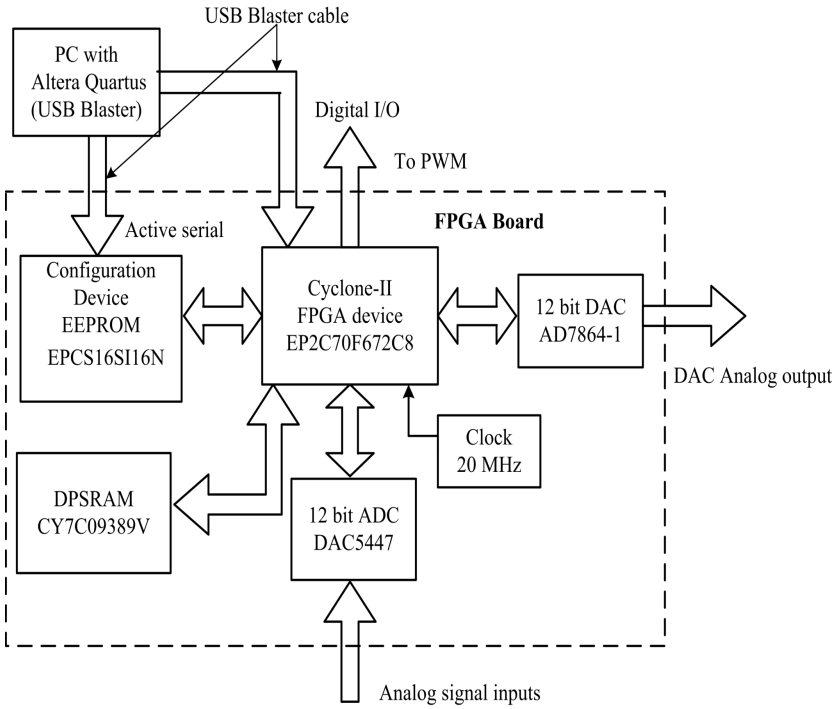


Figure A.2: FPGA control board

g) **Program flow:**Flow chart for program execution is given in Figure A.3. Photograph of the setup is shown in Figure A.4.

A.3 Voltage Sensor PCB

Three voltage sensors are mounted on three PCB boards. LV25-P/SP2 of LEM make is used. The conversion ratio for this sensor is 2.5:1 and has maximum primary current of 14 mA. The voltage sensors are used to measure the grid phase voltage and its peak value is considered for primary side resistor calculations.

As per the above constraint, the primary side resistor is chosen as 22 k and hence the primary current to the sensor is 4.54 mA. The primary side resistor arrangement consists of two parallel arms. In each arm three resistors of 66 k are connected in series. The effective resistance value of the primary side is 22 k. This arrangment is considred to avoid excess power dissipation in resistor. The corresponding secondary current is 11.27 mA. To convert the output current to voltage a 100 resistor is placed at secondrary side. Thereby, the voltage across secondary side resistor is calculated as 2.22 V. The schematic and the PCB layout of voltage sensor LV-25P/SP2 are shown

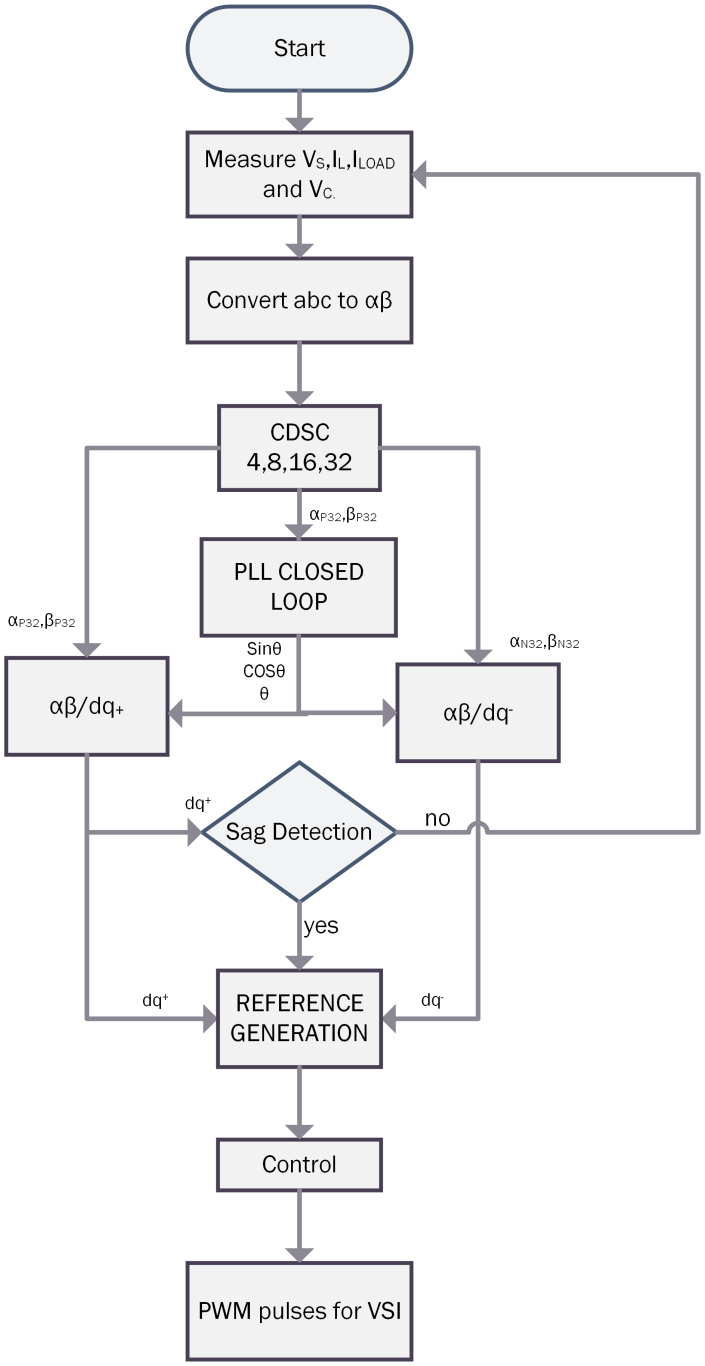


Figure A.3: Flow chart of program execution

in Figure A.5 and A.6 respectively.

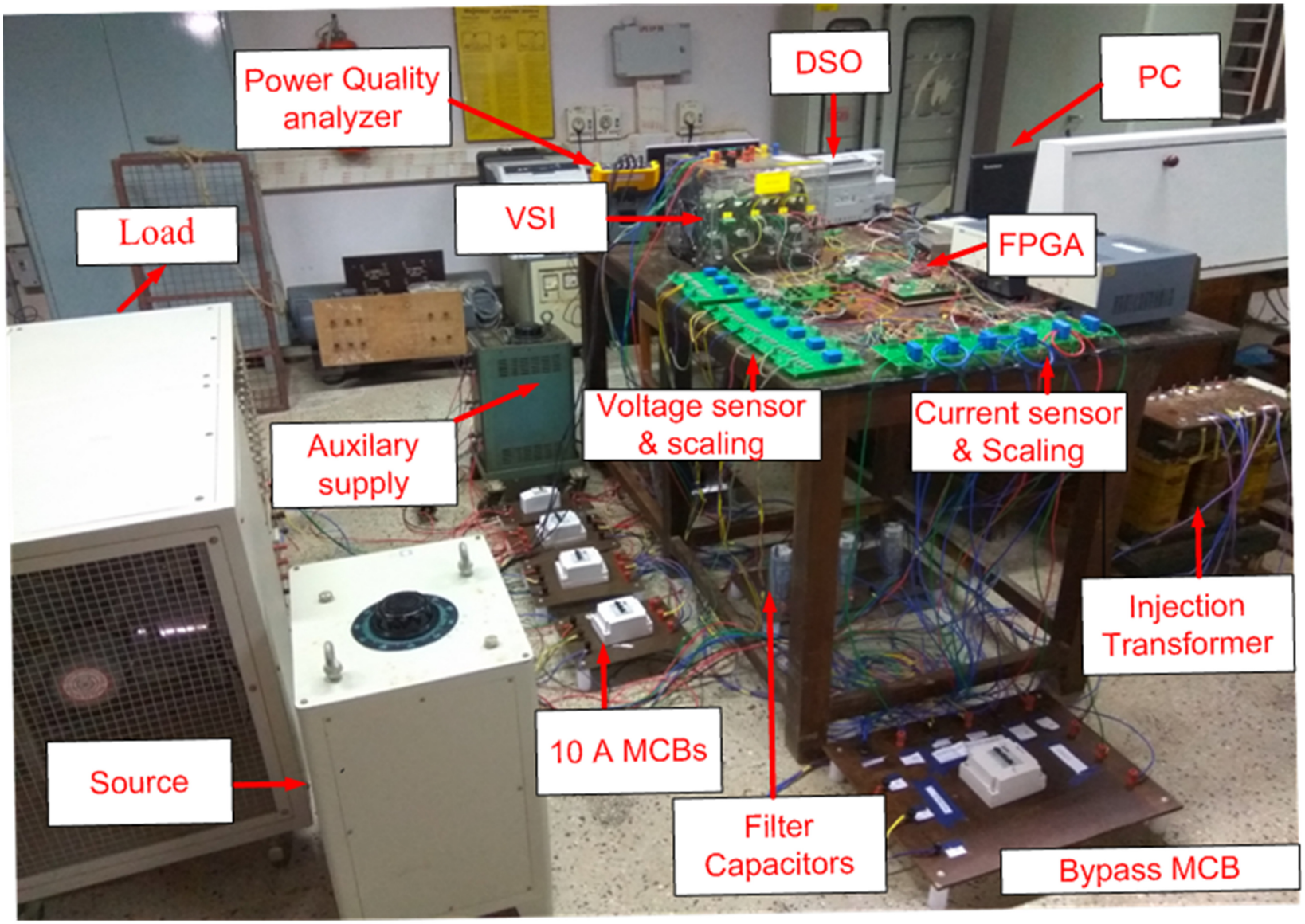


Figure A.4: Photograph of laboratory prototype setup

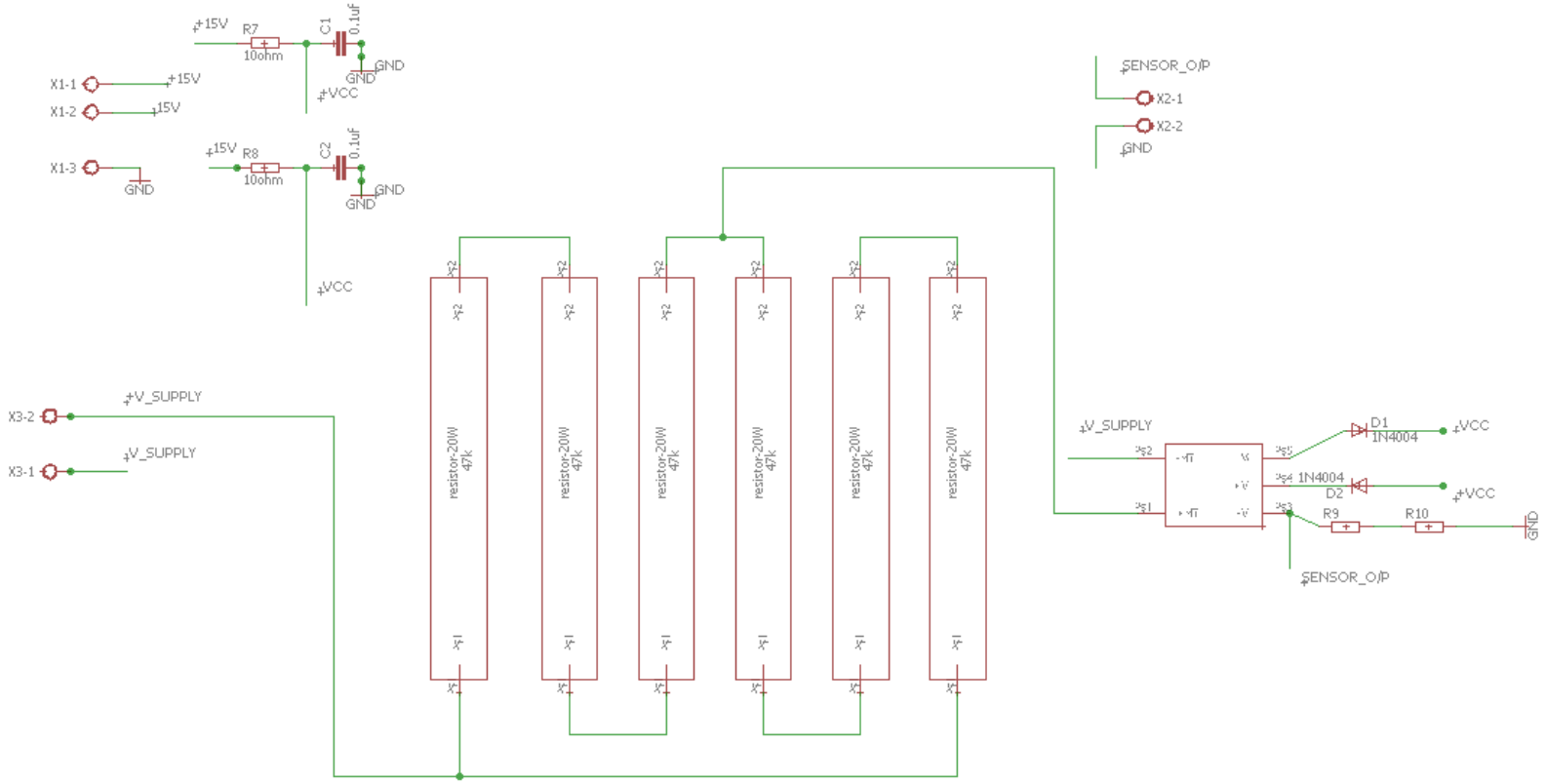


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Figure A.5: The schematic of voltage sensor LV-25P

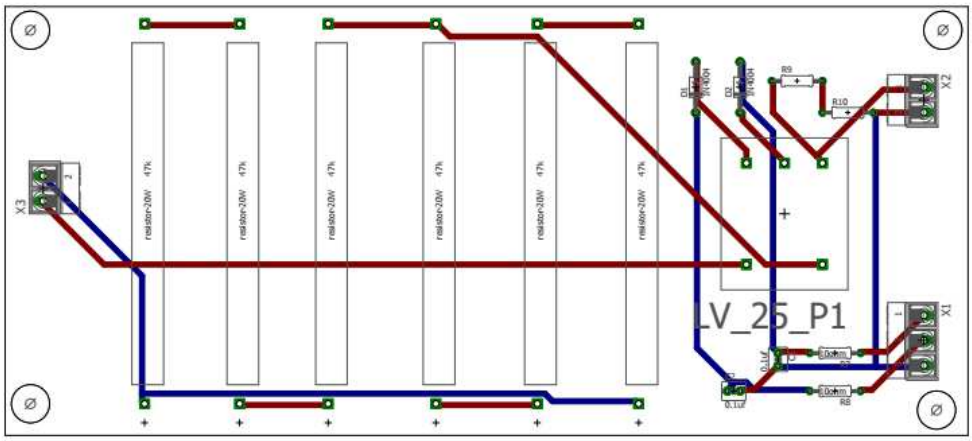

Figure A.6: PCB layout of voltage sensor LV-25P/SP2

A.4 Scaling circuit

The terminal voltage the DVR laboratory prototype is scaled down to 5 V range using sensor circuit and scaling circuit and are given as input to FPGA controller. The scaling circuit is used to amplify sensor output to 5 V range. The scaling circuit consists of op-amp's and resistors. The gain of voltage scaling circuit is chosen as 1.56 respectively because the output of voltage sensor unit is 1.52 V and 2.21 V respectively. The switching frequency of the inverter is considred as 5 kHz. In order to remove the switching noise, both the filters are designed at 3.3 kHz frequency. The PCB layout and schematic of scaling circuit are shown in Figure A.7 and A.8 respectively.

A.5 PWM Scaling

The schematic and layout of PCB for PWM amplification circuit are shown in Figure A.8 and A.9 respectively. The output signals from the FPGA board (5V) are amplified by the IC ULN2003AN before being given to the SEMIKRON DRIVER card (skyper 32 pro) (15V). It is a 16 pin IC with input impedance of 10 k and output impedance of 1 k. A High value of impedance at input side and low impedance at output side is chosen to eliminate the loading effect on the driver card and also to connect more than one device at the output. The supply is given to the 9^{th} pin of the IC and the 8^{th} pin is connected to the ground. This IC provides the inverted outputs. So, necessary precautions have to taken while connecting IC outputs to the driver card.

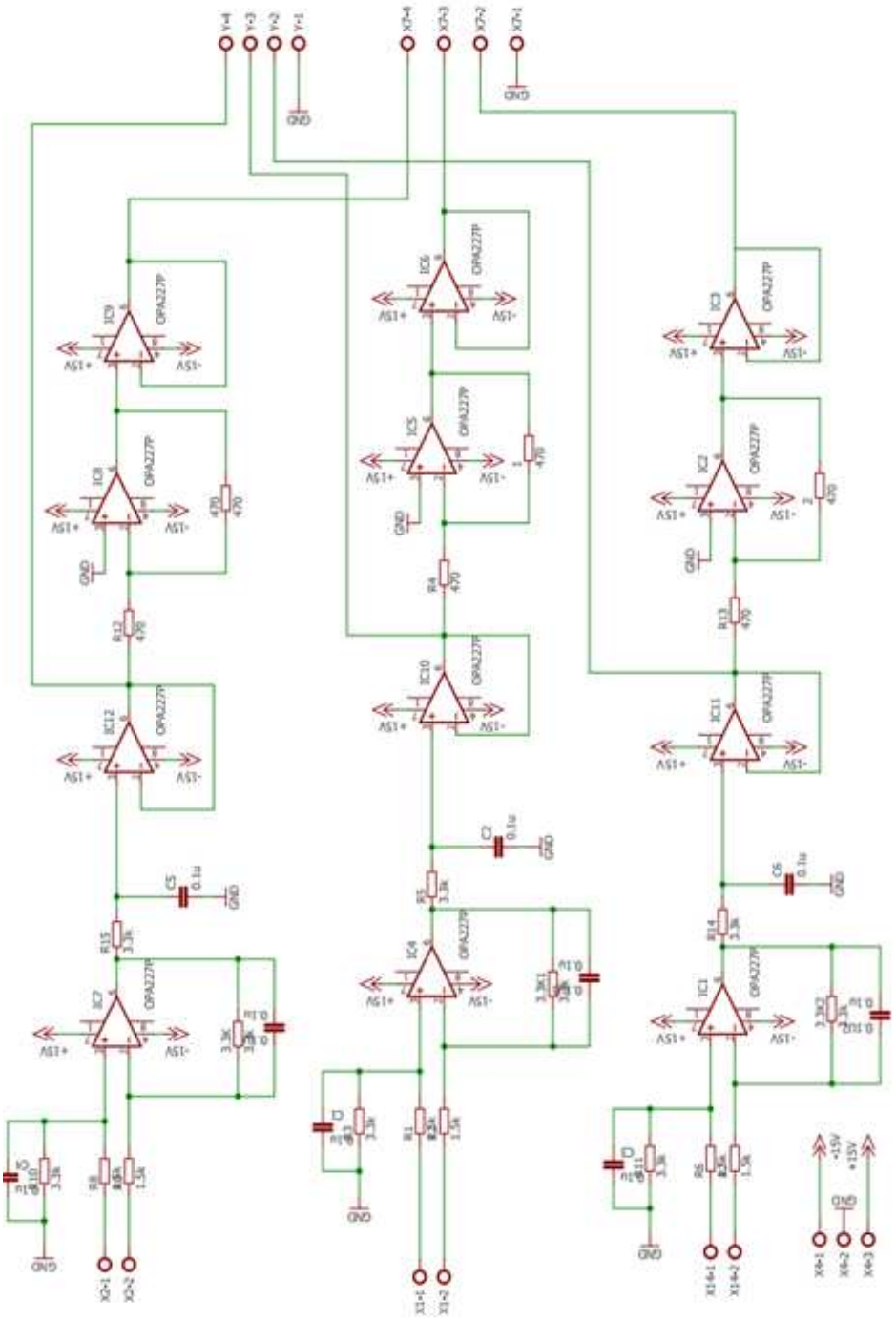

Figure A.7: The schematic of scaling circuit

A.6 Gate driver card

The PWM signals are connected to the gate and emitter terminals of the IGBT through gate driver card, which provides isolation and sufficient current drive ability

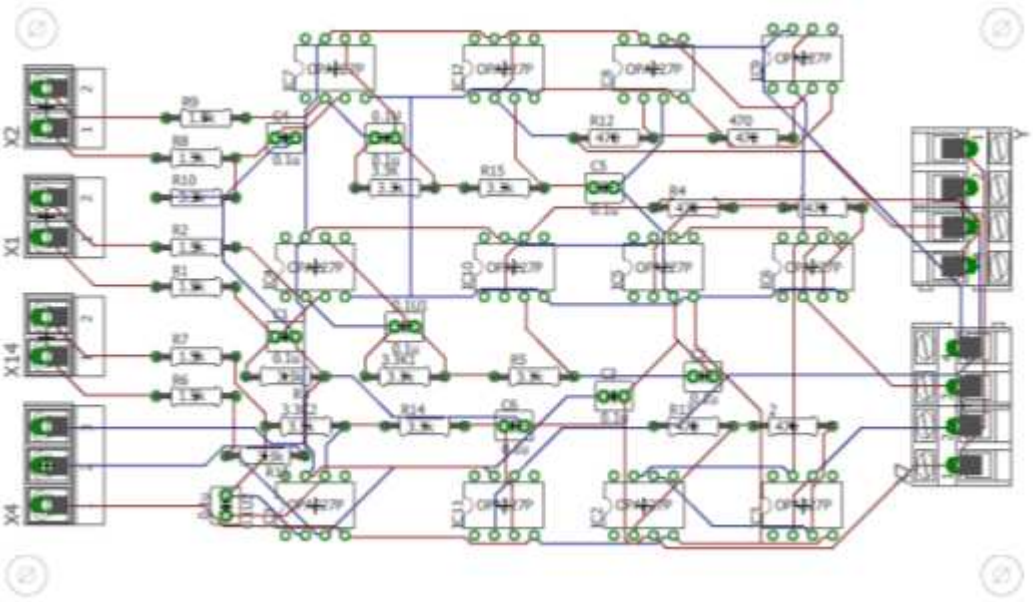

Figure A.8: PCB layout of scaling circuit

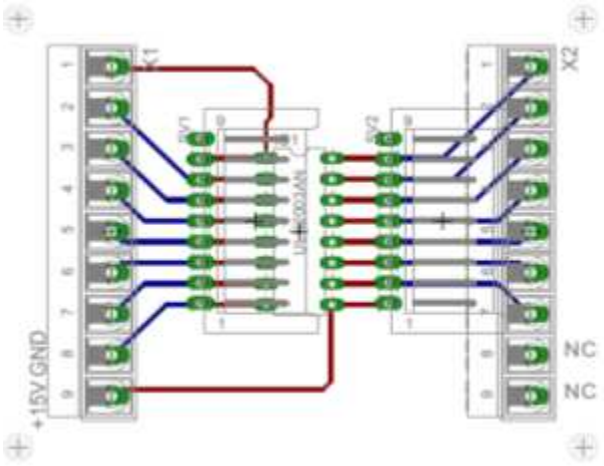

Figure A.9: PCB layout of PWM amplification

for the operation of the IGBT. The gate driver also incorporates the short-circuit protection by sensing the collector-to-emitter (i.e. VCE) voltage of the switch. The SEMIKRON made gate driver (SKYPER 32 Pro) is used for this application. The connection diagram of SKYPER 32 Pro is shown in Figure A.10. DC power supply of 15 V with current rating of 1 Amp is used for powering of driver card. Further, grounds are common for 15 V power supply and switching pulse. During normal/healthy condition of driver card, the error status is low (LED status is OFF) and the driver current should be around 120 mA.

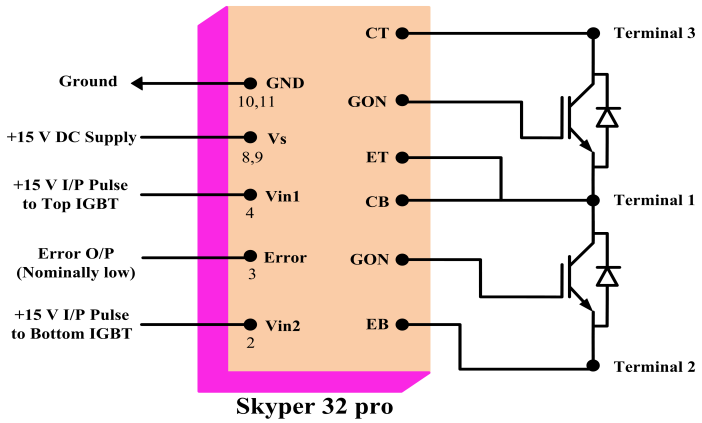

Figure A.10: Skyper32Pro driver card

A.7 TDVR Experimental setup

The papameters involved in TDVR experimental are almost similar to the aformentioned setup except for the custom made-VSI which is as shown in Figure.

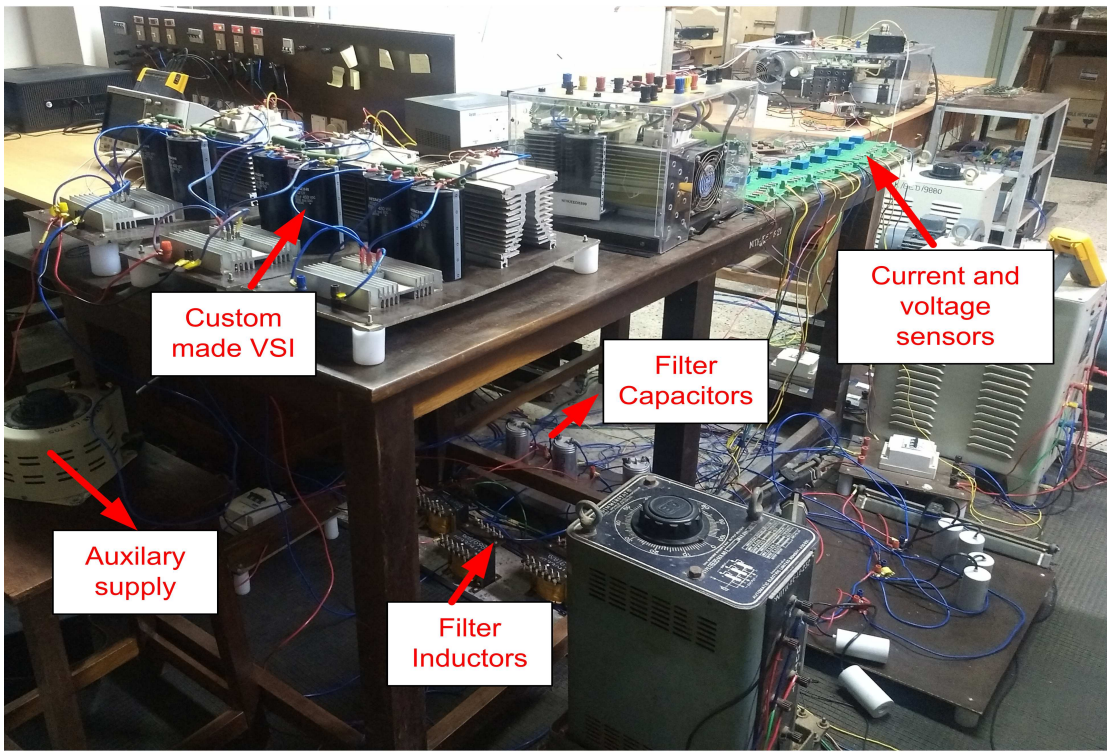

Figure A.11: TDVR Experimental setup

A.8 Conclusion

This chapter has provided a detailed description of laborotory prototype for the FPGA based closed loop control of low voltage series converter (DVR). Various PCBs are designed for current and voltage sensing, scaling circuit and PWM amplification. The schematic, layout of PCBs designed are provided.

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PUBLICATIONS BASED ON THE THESIS

Patents

a) A.Karthikeyan, B.Venkatesa Perumal, D.G.Abhilash Krishna, K.K.Prabhakaran, "A dynamic voltage restoration system for weak ac grids and a method thereof", Indian patent application no. 201741004197 filed on 16/03/2017.

Papers in refereed journals

a) D.G.Abhilash Krishna, A. Karthikeyan, K. K. Prabhakaran, Sushant Kumar, "An Efficient Pseudo-Derivative-Feedback-Based Voltage Controller for DVR Under Distorted Grid Conditions.", *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*,vol. 2, no. 1, pp. 71-81, Jan. 2021.

a) A. Karthikeyan, D.G.Abhilash Krishna, Sushant Kumar, B.Venkatesa Perumal, S. Mishra, "Dual Role CDSC based Dual Vector Control for Effective Operation of DVR with Harmonic Mitigation.", *IEEE Transactions on Industrial Electronics*,vol. 66, no. 1, pp. 4-13, Jan. 2019.

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a) D. G. Abhilash Krishna and A. Karthikeyan, "Design and analysis of frequency adaptive CDSC-PLL for Dynamic Voltage Restorer during adverse grid conditions" in Proc. *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, Cochin, India, 2020

b) A. Karthikeyan, D. G. Abhilash Krishna and C. Nagamani, "Virtual Impedance based DFCL for DVR during Downstream Faults" in Proc. *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Chennai, India, 2018, pp. 1-6

c) A. Karthikeyan, D. G. Abhilash Krishna, S. Kurra and K. K. Prabhakaran, "Uncertainity and Disturbance Estimator based Control of Transformerless DVR.", *018 IEEE International Telecommunications Energy Conference (INTELEC)*, Turin, 2018, pp. 1-6

d) A. Karthikeyan, D. G. Abhilash Krishna, S. Kumar and C. Nagamani, "Design and Analysis of Multi-Loop Feed Forward Control Schemes for DVR under Distorted Grid Conditions.", *2017 14th IEEE India Council International Conference (INDICON)*, Roorkee, 2017, pp. 1-6

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