DESIGN AND ANALYSIS OF SWITCHED CAPACITOR CONVERTER TOPOLOGIES FOR LOW POWER APPLICATIONS

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

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To God Almighty, my strength
To My father Subburaj R and mother Selvi O, my inspiration
To Shivani M and Monish N, my love
To My family members and all the friends, my sincere thanks

DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled **"Design and Analysis of Switched Capacitor Converter Topologies for Low Power Applications"** which is being submitted to the **National Institute of Technology Karnataka, Surathkal** in partial fulfillment of the requirement for the award of the Degree of **Doctor of Philosophy** in **Department of Electrical and Electronics Engineering** is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

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Place: NITK-Surathkal

Date:

CERTIFICATE

This is to *certify* that the Research Thesis entitled **"Design and Analysis of Switched Capacitor Converter Topologies for Low Power Applications"** submitted by **Vivekanandan S** (Register Number: 148038EE14F11) as the record of the research work carried out by him, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of **Doctor of Philosophy**.

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Abstract

DC - DC converter can be regarded as the heart of any electrical or electronic circuit for buck, boost, inverting or conditioning the target voltage from the available source voltage. Switched Mode Power Supplies (SMPS) are the widely used converters in this segment. Any modern SMPS comprises an energy storage element that transfers the energy from source to load. Inductors are the widely accepted storage element in most of the present day SMPS. They are capable of carrying larger currents by virtue of their construction in large power converters. However, when it comes to small converters, bulky and heavy inductors often restrict the application in an on chip miniaturization circuit. Capacitor, which is another energy storage element, because of its high energy density and low equivalent series resistance compared to inductors, is promising for efficient on chip application. Switched capacitor converters (SCC) that are using only switches and capacitors popularly known as flying or charge pump capacitors are gaining popularity in on die power management boards.

In this thesis, the concept of generalized Fibonacci single input single output (SISO) SCC is discussed and it has more efficiency and less equivalent resistance value. Generalized Fibonacci SCCs are technologically advanced and operate on fixed conversion ratio. Different target ratios of Fibonacci series have already been carried out by researchers to step-up and step-down configuration. But, 1/6 and 5/6 voltage ratios of Fibonacci SCC have not been proposed in the literature. To solve the unsolved voltage ratios two possible cases are considered: 1) Fourteen switches and four flying capacitors using $F_i = F_{i-1} + F_{i-3}$ series. 2) Generalized Fibonacci SCC network is used and a new series is developed to solve the voltage ratios 1/6 and 5/6 with 12 switches and 3 flying capacitors. Theoretical results and simulation results are validated. To overcome limited voltage ratios, reconfigured dual input and single output (DISO) SCC is developed. A reconfigurable SCC topology with nine/ten CMOS switches and two flying capacitors is developed. It is capable of accepting two input sources simultaneously with an input voltage in the range of 1-2.5 V and delivers the output for 15 conversion ratios. The proposed SCC

can drive a load current ranging from 10 μA to 10 mA at an open loop efficiency of >90%. One of the important applications of the proposed converter is the utilisation of photovoltaic (PV) or the combination of PV and other direct current sources. The regulation of the output voltage can be achieved either by changing the voltage ratios or using variable switching frequency. DISO requires more space and more capacitors to develop more voltage ratios. To overcome such issues, the dual input dual output (DIDO) converter is developed.

A new dual-input and dual-output SCC is designed to operate with two independent voltage sources that provide two different output voltages and generate 56 voltage ratios. The converter is portable to operate with one or two input sources alternatively and have the ability to vary 56 voltage ratios. An efficient low power SCC is designed for input voltage of 1.5 V to 5 V that gives dual output voltages of 1 V to 10 V. The designed converter can operate in both buck and boost modes. SCC has high drive capability of load current from 10 μA to 25 μA that is adjusted by operating frequency. The algorithm is discussed to solve the coupled case of dual input and dual output converter. Another major contribution in this research is the introduction of R- parameters calculation for the coupled case and is deliberated in detail since it includes all conduction and ohmic losses accounting for coupling effects. To validate the performance of designed SCC, modeling and mathematical analysis has been carried out. Finally, an extended version of reconfigurable SISO SCC is designed for driving the white light emitting diodes (WLEDs).

The various voltage ratios are selected to control the WLEDs blacklights using the inverted SCC (ISCC), which helps to save the battery life of electronic devices. The major contribution is developing maximum voltage ratios for power converter driver ICs and equivalent resistance (R_{eq}) accurate calculation where it includes all conduction and ohmic losses. Furthermore, ISCC experimental results are obtained from prototype model. Accurate R_{eq} analyses validate the accuracy of the proposed topology. It is designed for low voltage of 10 mV to 0.1 V and it provides the output voltage of -100 mV to -0.5 V. Finally, the accurate R_{eq} calculation and the results are verified experimentally, particularly, at the transition re-

gion (between slow switching limit (SSL) and fast switching limit (FSL)). Theoretical calculation from the model derived concurs well with simulation and experimental findings. Accurate equivalent resistance calculation and average current calculation are compared with existing R_{eq} analysis available in the literature.

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[1] All the values in the table are rounded to nearest points

List of Abbreviations

CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DISO	Dual input dual output
DISO	Dual input single output
ESR	Equivalent series resistance
FC	Full charge
FSL	Fast switching limit
IC	Integrated circuit
IDC	Indirect Charging
ISCC	Inverted SCC
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCD	Liquid crystal display
PCB	Printed circuit board
RC	Resistor - capacitor
SCC	Switched capacitor converter
SGF	Signed generalized Fibonacci
SGT	Signed generalized Tribonacci
SIDO	Single input dual output
SISO	Single input single output
SMPS	Switched-mode power supply
SPST	Single pole single throw
SSL	Slow switching limit
VCR	Voltage conversion ratio
VLSI	Very-large-scale integration
WLB	White LED blacklight
WLEDs	White light-emitting diode
ZC	Zero Charge

List of Symbols

V_r, M_n	Voltage ratio
V_{in}, V_s, V_{s1}, V_{s2}, V_{in1}, V_{in2}	Input voltage
C_{in}	Input capacitor
V_o, V_0, V_{o1}, V_{o2}	Output voltage
i_o	Discontinuous current
N_c	No connection
V_{r+1}	Pairs of voltage ratio
R_{eq}	Equivalent resistance
N	Integer
n	Number of capacitors
Φ	Phase
N_S	Number of capacitor stages
C_o, C_{out}	Output capacitor
M_u	Pair of conversion ratio
N_c	No connection
i_o	Discontinuous current
R_{on}, r_{on}	On resistance
V_c	Capacitor voltage
C_1-C_4, C_{fly}	Flying capacitors
V_1-V_4	Flying capacitor voltages
T_i	Tribonacci sequence
F_i	Fibonacci sequence
I_i	Average topology current
i	Topology number
I_o	Average output current
$A_{i,m}$	SGF coefficients
$S_{b1} - S_{b9}$, $S_1 - S_{11}$	Bidirectional switches
Φ_c	Charging phase
Φ_t	Discharging phase
V_{bat}	Input battery voltage
P_{equi}	Power equivalent
T_{Φ_c}	Time period for charging phase

T_{Φ_t}	Time period for discharging phase
f_{switch}, f_s	Switching frequency
R_1, R_2	Load resistance
I_{L1}, I_{L2}	Load current
R_{12}, R_{21}	Transresistance, Coupling resistance
T_1 - T_4	Time constant for different phase
Q	Net charge

Chapter 1

INTRODUCTION

This chapter discusses a detailed overview of the switched capacitor converter (SCC). SCC is a subset of DC-DC power electronics converters without inductors that convert one range of voltage to the other. As there are no inductors, it is preferably used for on chip integration. Before proceeding to more advanced topics, this chapter presents the fundamental principles behind SCC. The first part of this Chapter deals with the basics of SCC. Next, an overview of the SCC model and the different types of SCC topologies. Finally, a brief discussion about the dissertation outline is introduced which will be discussed at length in the later Chapters of this work.

1.1 Background

In recent days, portable electronic equipment such as digital devices, tablets, mobile phones, digital cameras have been technologically improving very fast. Due to their popularity, the electronic device power module requires some features of light weight, small volume, high efficiency and good regulation capability. Besides these, flexible controller design, and multiple output ratios become more and more essential for designing power modules. More emphasis is laid on developing power converters in literature for low power applications. One of the main applications of SCC is the design of VLSI circuits, which operate from a single input voltage source and supply different voltages to various part of the circuit. For energy limited VLSI applications, DC/DC converters such as battery charger and power management for signal processors and flash memory systems are utilized (Tanzawa et al., 2002, Baek et al., 2010, Derhacobian et al., 2010). Many switched capacitors converters are proposed in the

literature (Wong et al., 2014) and the switched capacitor converters (SCCs) contain only capacitors and power switches. Unlike conventional power converters, SCCs do not require any energy storage in the form of magnetic field. SCCs have large number of topologies, allowing both step/up and step/down functions. SCCs are used for LCD drivers where input voltage is higher than the supply voltage (Wu and Chen, 2008, Su and Ki, 2008) and also in voltage regulators, charge pump application, wireless sensor network circuits, biomedical implant devices and energy harvesting system (Zhao et al., 2012, Salter et al., 2009, Eguchi et al., 2009, Kim et al., 2012, Zhang et al., 2012, Sarker et al., 2011).

1.2 SCC Commercial Integrated Products

SCCs are mainly used for many applications such as chip level management, inverters, converters and surge generators in high voltage engineering. SCC has more advantage because, energy is transferred solely using capacitors. SCC commercial products are available in the market for different voltage ranges with usage of multiple SCC. These commercial parts are basics, providing fixed voltage ratios such as doubling and inverting (Wu and Chang, 1998). Some commercial products related to the SCC are developed by MAXIM integrated circuits, implemented single input dual output SCC (Pumps, 2014). Similarly Texas Instruments developed single input single output SCC (management IC-TPS65913, 2015) and power management IC with 20 regulated outputs (Converter, 2014). The National semiconductors (Dickson, 1976a) developed a buck/boost DC-DC converter supporting multiple outputs but needed to be used with flying capacitors externally (Makowski and Maksimovic, 1995). The above commercial SCCs are likely to generate less voltage ratios and more chip space. This research aims at designing a new topology of SCC that will be capable if developing maximum voltage ratios.

1.3 Various SCC Topologies Structures

A SCC is a power electronic converter that has only two components, namely switches and capacitors. In general, SCC can have a large number of ports. Each of the ports can be connected to different types of circuits. A SCC can be developed in many stages or sub circuits to expand the voltage ratios. A single stage/multi stage SCC

can be implemented using different SCC configurations which are

1. Single input single output converter (SISO).
2. Single input dual output converter (SIDO).
3. Dual input single output converter (DISO).
4. Dual input dual output converter (DIDO).

All the above mentioned SCC configurations are charged using different switching sequence to generate different voltage ratios, i.e, it can be configured by changing the charging direction of the capacitors or changing the clock sequence of each switches. The voltage ratios are realized when the capacitors are charged and discharged using load, to another capacitor or the ground terminal in the circuit. Three operating states of capacitors (Zou and Wang, 2012) are: (a) Charging state (b) Discharging state (c) Idle State. By the concept of energy transfer, SCC topologies are classified as following:

1. Direct charging Converter.
2. Indirect Charging Converter.

1.4 Direct Charging Converters (DCC)

The output capacitor is charged directly through voltage source and therefore no intermediate circuits and capacitors are connected. In DCC, the conduction loss is minimum and the ideal time is zero because the output capacitor is charged directly using voltage sources. Direct charging converter is further classified into two different schemes:

1. Parallel-series converter scheme.
2. Time sharing converter scheme.

1.4.1 Parallel-Series Converter Scheme

It is a basic scheme for SCC; for step-down configuration. Direct charging is done for capacitor by connecting in parallel and discharging is done by connecting the load

in series. Similarly for step-up configuration, charging of the capacitors is performed in series and discharge in parallel with respect to the load. As an example, step-up parallel series converter is considered and it is shown in Fig 1.1 where, V_{in} is the input voltage, C_{in} is input filter capacitor, $C_1 - C_3$ are the flying capacitors and V_o is the output voltage. The switching pattern is performed using series-parallel operation where all $n-1$ capacitors are connected in phase 1 (ϕ_1) parallely and remaining capacitors are connected in phase 2 (ϕ_2) in series.

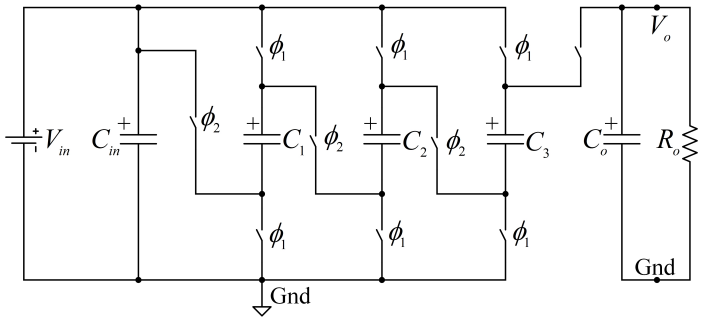


Figure 1.1: Generalized parallel-series topology

1.4.2 Time Sharing Converter Scheme

Each output capacitor is charged in the means of time sharing (time taken to charge a capacitor). Time sharing concept based on voltage triple circuit is shown in Figure 1.2, where $S_1 - S_6$ are the bidirectional switches, V_{in} is the input voltage, C_{in} is input filter capacitor and R_o is the load resistance. For 3 flying capacitors ($C_1 - C_3$) to be charged, each of the capacitor is charged for 1/3 times of the switching cycle. As a direct-charging topology, there are no intermediate stages between the source and the load, which can help to reduce the conduction loss. However, this time-sharing scheme is not efficient for generating more voltage ratios. As the voltage transfer ratio increases, both the voltage stress on the switches and the peak charging current increase, resulting in larger conduction losses and converter cost.

1.5 Indirect Charging Converters (IDC)

Most advanced SCC topologies belong to this category. In this converter category, energy flows through intermediate capacitors and get delivered to the load, where

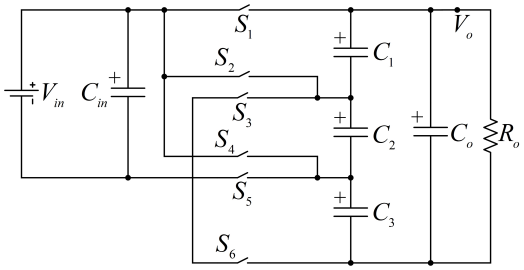


Figure 1.2: Generalized 3X timing sharing converter topology

intermediate capacitors are mainly used for transferring the energy from source to load through step by step charging level. Here the main advantages of these categories of converters are less number of switches and limited peak charging current. Some of the developed SCCs of IDC based converters are classified as,

- Dickson charge pump.
- Fibonacci converters.
- Exponential converters.

The different topologies of IDC SCC are constructed for step-up and step-down configurations. Voltage ratios for different topologies are achieved by cascading number of stages, N_s. The three topologies mentioned in this section are the most commonly used topologies for DC-DC conversion (Dickson, 1976b, Ueno et al., 1991, Starzyk et al., 2001).

- **Dickson charge pump**[1] of n stages, is shown in Figure 1.3 where $S_{11} - S_{n1}$ and $S_{21} - S_{n2}$ are bidirectional switches, $C_1 - C_n$ are the flying capacitors and all the switches and capacitors are considered as ideal values. The capacitors are charged from supply voltage V_{in}, and then transferring capacitor voltage to next flying capacitors during clock pulse, ϕ_1 and ϕ_2 respectively. For n, number of flying capacitors output voltage is equal to $(n+1)V_{in}$, i.e., Generation of maximum voltage ratios is with respect to number of flying capacitor stages.
- **Fibonacci converters**[2] of n stages are shown in Figure 1.4 where $S_{11} - S_{n1}$ and $S_{21} - S_{n2}$ are bidirectional switches, $C_1 - C_n$ are the flying capacitors and all

[1]For, simplicity step-up operation is considered.
[2]For, simplicity step-down operation is considered.

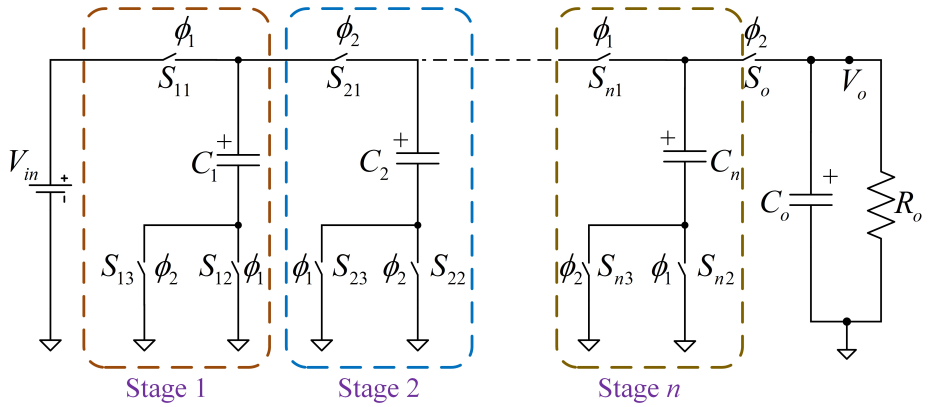


Figure 1.3: Topology of Dickson charge pump for step-up

the switches and capacitors are considered as ideal values. Normally Fibonacci series is defined as, $F_n = F_{n-1} + F_{n-2}$, where all the capacitors are charged according to $F(N_s + 1)V_{in}$ in phase 1 ϕ_1, (even Fibonacci values) and phase 2 ϕ_2, for odd Fibonacci values. N_s is the stages of converter and V_{in} is the input voltage of the converter.

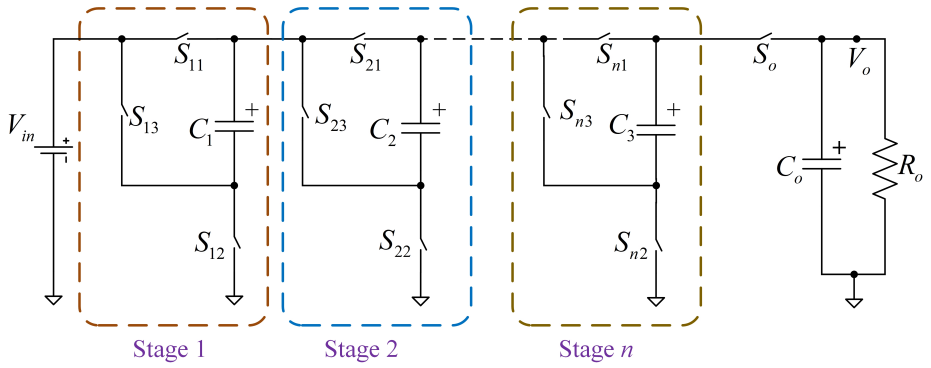


Figure 1.4: Generalized topology of Fibonacci charge pump

- **Exponential converters**[2] of n stages are shown in Figure 1.5 where $S_{11} - S_{n4}$ and $S_{21} - S_{n4}$ are bidirectional switches, $C_{11} - C_{n1}/C_{12} - C_{n2}$, are the flying capacitors and all the switches and capacitors are considered as ideal values. In this topology, output voltage of each stage will become the input voltage of next stage. For n^{th} stage conversion ratio exponential method is given by $2^n V_s$. The main disadvantage of these topologies is that in each stage two capacitors are used.

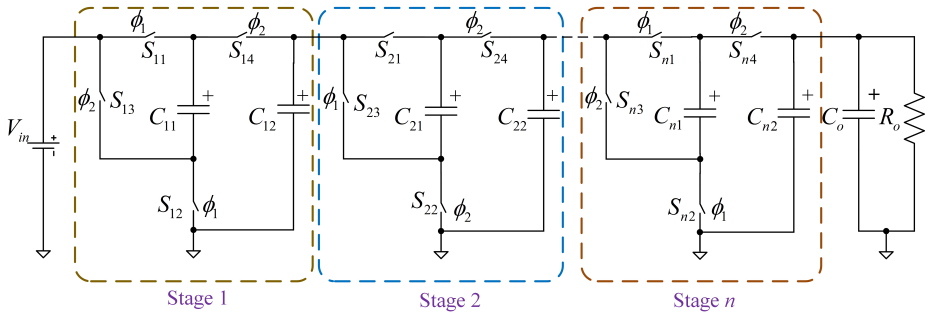


Figure 1.5: Generalized topology of exponential charge pump

Among all the topologies, Fibonacci has more advantages over all the other topologies because, higher voltage ratios (Kushnerov, 2014b) can be achieved. Also, the Fibonacci SCC requires less number of switches, capacitors and topologies stages. Whereas other topologies generates less conversion ratios and more voltage stress across switches.

1.6 Classification of Various Configurations of SCC

Referring to Section 1.3 the different classifications of the various SCC topologies are explained in detail.

1.6.1 Single Input Single Output Converter

SISO converters are the basic converters which are used for low voltage circuits and preferably used for designing voltage regulators. Different types of SISO were discussed in the previous Section 1.5.

1.6.2 Single Input Dual Output Converter

Dual output converter is mainly designed to increase the resolution (Kushnerov, 2014a) for obtaining different voltage ratios (V_r). Here, V_r is spaced as $1 + V_r$. For a conversion ratio formal synthesis is derived for obtaining dual step-up Fibonacci SCC. It gives different pairs of conversion ratio V_{r+1}. For dual output, switching is performed between load and conversion ratio (Han et al., 2007, Jeon and Kim, 2012, Kumar and Proefrock, 2012, De Clercq et al., 2012, Rao et al., 2005). The main problem occurs when switching is done continuously such that transients will

be more. For controlling the transients each output of SCC is operated in burst mode (Kushnerov, 2014a). To overcome discontinuous current, i_0, a topology is proposed

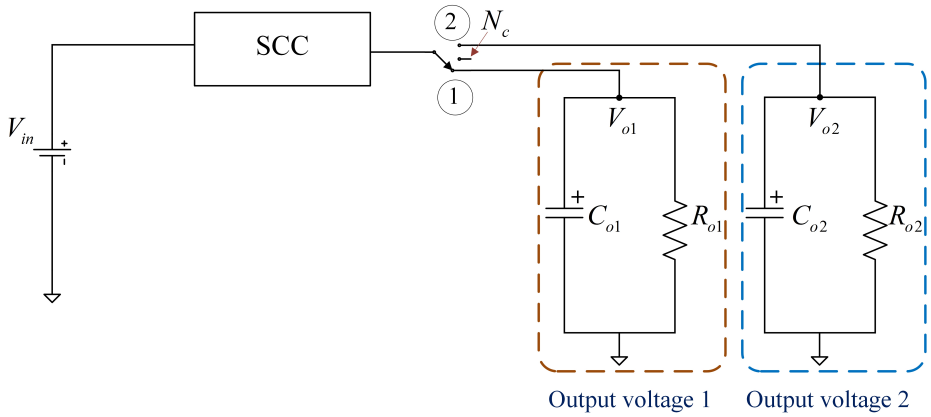


Figure 1.6: Dual output topology using sub interleaved mode

by changing the output from ①, ②, and N_c, where N_c denotes no connections which is shown in Figure 1.6. When switching is done between load and conversion ratio for single period it is known as sub-period interleaved mode (Kushnerov, 2014a). The main disadvantage of this method is that only non unity gain voltage ratios can be achieved.

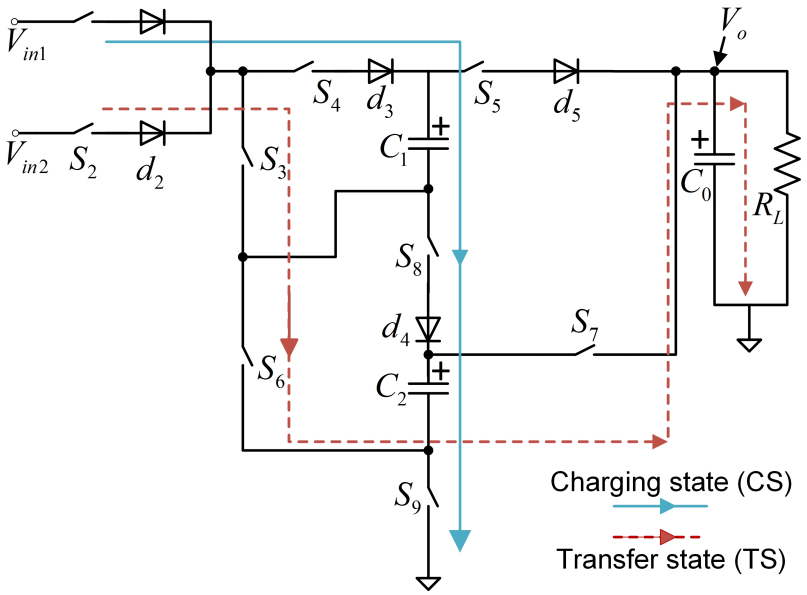


Figure 1.7: Generalised DISO topology

1.6.3 Dual Input Single Output Converter

Dual input single output (Abraham et al., 2017) SCC is designed for developing standby inputs and is shown in Figure 1.7. The different target voltage ratios are generated to operate with low input/output voltages where maximum of 11 voltage ratios are possible to develop. DISO switching phases (ϕ_1 and ϕ_2) are used for charging (CS) and discharging (TS) the capacitors. The DISO is easy to implement in on chip due to its small size and light weight and more efficiency. The main disadvantage of this topology is that only non unity gain voltage ratios can be developed using 9 switches ($S_1 - S_9$), 5 diodes ($d_1 - d_5$) and 2 flying capacitors ($C_1 - C_2$). The detailed explanation is discussed in Chapter 3.

1.6.4 Dual Input Dual Output Converter

DIDO converter is an advanced converter and it is developed using new topology where two outputs in single converter, generates coupled outputs and decoupled outputs. DIDO SCC is developed for maximum voltage ratios which generates two different output voltages. The first output terminal is used to generate step-up or step-down voltages. Similarly, the second output terminal is used to generate another voltage ratios. A brief explanation is given in Chapter 4.

1.7 Research Gaps and The Pre-Existing SCC Analysis

Many researchers worked on different topologies of SCCs such as Fibonacci, series-parallel, Inversion, charge pump that are used for developing the trendy electronics gadgets and supportive electronic equipment such as bio-medical instruments and mobile phones. The converters which are discussed in Sections 1.4 - 1.5 are eligible to develop minimum number of voltage conversion ratios (VCRs). The major disadvantages of all the categories of SCC topologies are more chip size, requires more number of capacitors and switches (i.e), based on number of stages of the converters, less efficiency and generates less voltage ratios. Among those categories of converters Fibonacci SCC can generate more voltage ratios. Kushnerov et al. (Kushnerov, 2014b) completely discussed Fibonacci voltage ratios in which two voltage ratios are

not possible to solve using generalized Fibonacci series. Herein, Tribonacci sequence is developed to solve the unsolved voltage ratios of generalized Fibonacci series using 2^3 Farey sequence. To develop the maximum voltage ratios with minimum equivalent resistance (R_{eq}), three advanced topologies of SCC are designed, which are capable of providing high efficiency, less voltage ripple and high performance. The advanced topologies will be discussed in Chapters 2 - 6.

Many researchers worked on analyses of R_{eq} SCC and they preferred to use diode-based implementation analysis which is specific for selected networks (Dickson, 1976a). Further, the analysis (Brugler, 1971, Ngo and Webster, 1994, Seeman, 2009) are performed using non general steps to solve their SCC problems. Long back, Maksiomovic et al (Makowski and Maksimovic, 1995) worked to develop a basic and fundamental concept for solving the problems in SCC and developed the concept of slow switching limit (SSL) (Seeman, 2009) but not the Fast switching limit (FSL) (Seeman, 2009). Further, they extended to solve R_{eq} analysis using network theory but, it was complex to solve the analysis even in ideal conditions. Seeman et al. (Seeman and Sanders, 2008) had solved both the SSL and FSL output conditions for single input single output topologies. All the topologies mentioned in Section 1.5 are solvable as mentioned in (Seeman, 2009). Recently, due to trendy of on-chip circuits and electronic products dual input/dual output topologies are improving a lot and the analysis for that topologies is very complex to solve which is due to two different cases, i.e., coupled and decoupled case (Zhaikhan et al., 2017). The decoupled case can be solvable as discussed in (Seeman and Sanders, 2008) or other methodologies, but for coupled case it is complex and lengthy. For solving the coupled case a new methodology is developed using the R-parameters two-port system.

1.8 Advancements in this thesis

The aim of this work is to present a complete design of SCC where it covers the unsolved fraction of Fibonacci topologies, improvement of voltage ratios in dual input converter topologies, design and analysis of dual input/dual output (DIDO) converter topologies and designing a reconfigured inversion SCC topologies used for low power applications. The overview of the thesis is depicted in Figure 1.8. Chapter 2 explains the single input single output SCC fundamentals and unsolved voltage ratios in Fibonacci SCC. These voltage ratios are solvable using two different series,

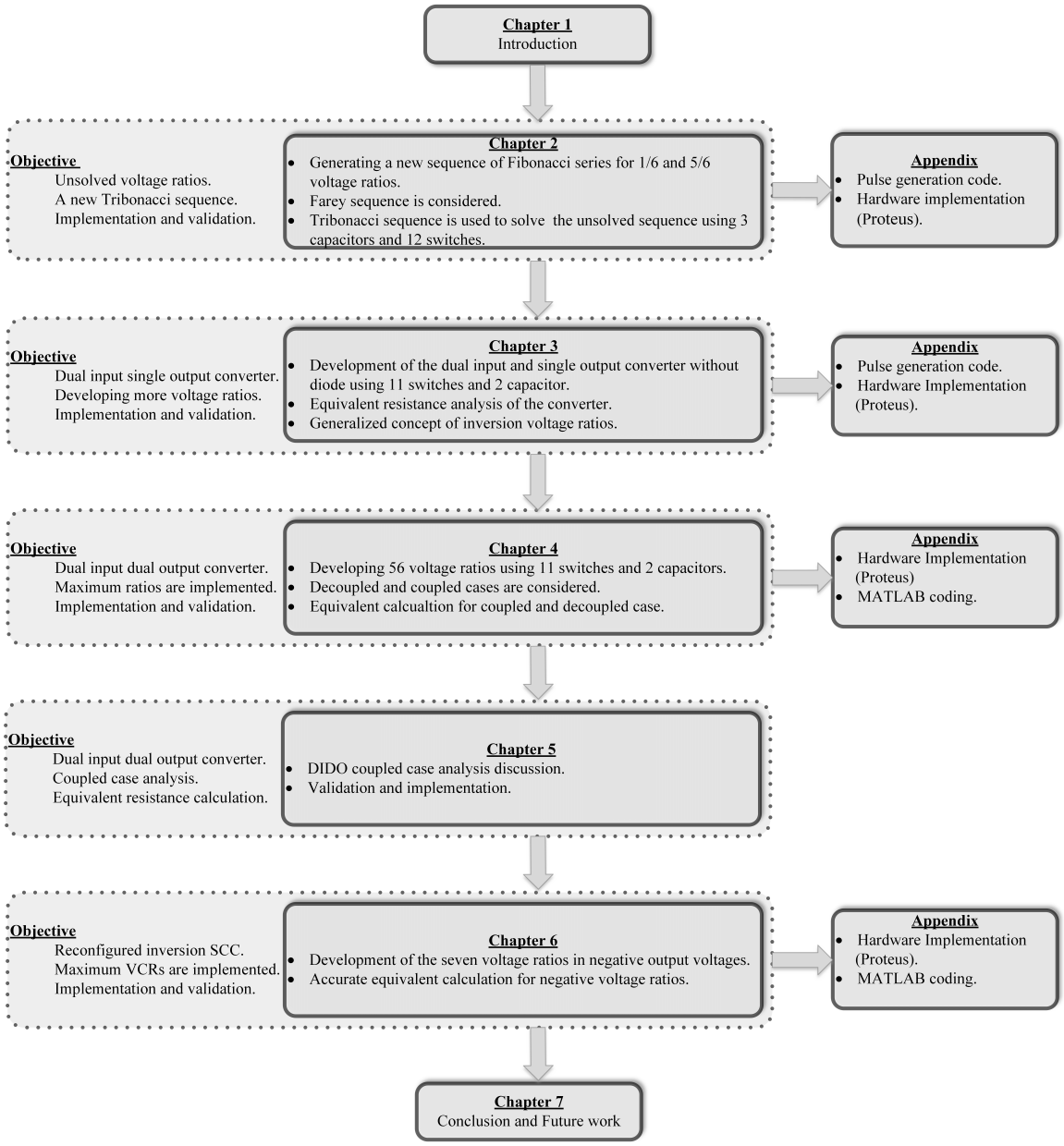


Figure 1.8: Thesis overview

namely Fibonacci and Tribonacci sequence. Finally, it explains the advantage of the developed sequences.

Chapter 3 explains the concept of 11 voltage ratios using reconfigurable DISO SCC topology with nine/ten CMOS switches and two flying capacitors. It is capable of accepting two input sources simultaneously with an input voltage and delivers the output for 15 voltage ratios. This chapter also discusses inversion topologies of SCC

for driving the white led driving circuits.

A new DIDO SCC topology has been developed and discussed in Chapter 4, which operates with two independent voltage sources that provide two different output voltages and generate 56 voltage ratios. The converter is portable to operate with one or two input sources alternatively and have the ability to vary 56 voltage ratios. An efficient low power SCC is designed for input voltage of 1.5 V to 5 V that gives dual output voltages of 1 V to 10 V. The designed converter can operate in both buck and boost modes. Challenges of DIDO coupled case is discussed in Chapter 5

The last chapters of the SCC topologies are extended version of Chapter 2 inversion mode. Chapter 6 discusses the inversion SCC (ISCC), that is capable of achieving seven negative voltage ratios using only three flying capacitors and minimum number of switches which is used to drive white-LED[3] backlight (WLB) in cellular phones for various backlight conditions. It has the advantage of choosing buck/boost voltages to drive the WLBs for various blacklight conditions. Finally, conclusion and future scope are discussed in Chapter 7

This work aims to present a complete and straightforward design methodology for SCC. The different topologies will benefit designers greatly in the use of SCC for both integrated and non-integrated applications. The designed SCC topology is the model for designing the on-chip[4] IC design. From the SCC model, chip designing will be easy to carry out back end IC fabrication.

[3]The prototype is designed using mV input voltage source for validating the ISCC converter.

[4]All the designed SCC topologies in this Thesis are considered as a model/ideology for developing ICs. All the prototype are designed for validation with the help of off-chip components.

Chapter 2

SINGLE INPUT SINGLE OUTPUT SCC

As discussed in Chapter 1, the voltage ratios of SISO Fibonacci SCC are unsolved using the generalised topology. The unsolved voltage ratios (1/6 and 5/6) of 2^3 Farey sequence order are solved by two possible cases that is discussed in this Chapter.

1. Generalized Fibonacci sequence with 5 capacitors and 16 switches.
2. Tribonacci sequence with 4 capacitors and 12 switches.

Comparative study of 12 switches/3 flying capacitors and 16 switches/4 flying capacitors is discussed with equivalent resistance calculation (R_{eq}).

Parts of this chapter were previously presented at the 1st IEEE International Conference on Power Electronics Intelligent Control and Energy Systems (ICPEICES), 2016 in Delhi, India (Subburaj et al., 2016).

2.1 Generalized Fibonacci Sequence With 5 Capacitors and 16 Switches.

The reconfigured proposed switching network for SCC to solve the unsolved voltage ratios (Kushnerov and Ben-Yaakov, 2013) is shown in Figure 2.1 where the bidirectional switches are S_1 to S_{16} with inbuilt switch on resistance $R_{on} = 0.4\Omega$ and the flying capacitors are C_1 to C_4. To solve the unsolved fractions a generalized series

has to be synthesized using a generalized equation that is given in (2.1). The possible generalized series is shown in Table 2.1. For simplicity and easy understanding a simple sequence, (i.e) $n \geq 2$ and $h \leq k \leq h+1$ is considered. The generalized Fibonacci numbers are normally defined as $F_i = F_{i-1} + F_{i-k} + (k-h)$, where starting value is $F_{2-k} = F_{3-k}$=. . .=$F_0 = (h-k+1)$ and F_1=1 (Kushnerov and Ben-Yaakov, 2013). Any Positive number N in the range of $(F_i \leq N_n \leq F_{i+1})$ can be expressed uniquely as a sum of distinct $(h,k)^{th}$ Fibonacci numbers using Daykin's theorem (Zeckendorf, 1972). Daykin expansion is also known as EZ-code (BROWN JR, 1964). In the range

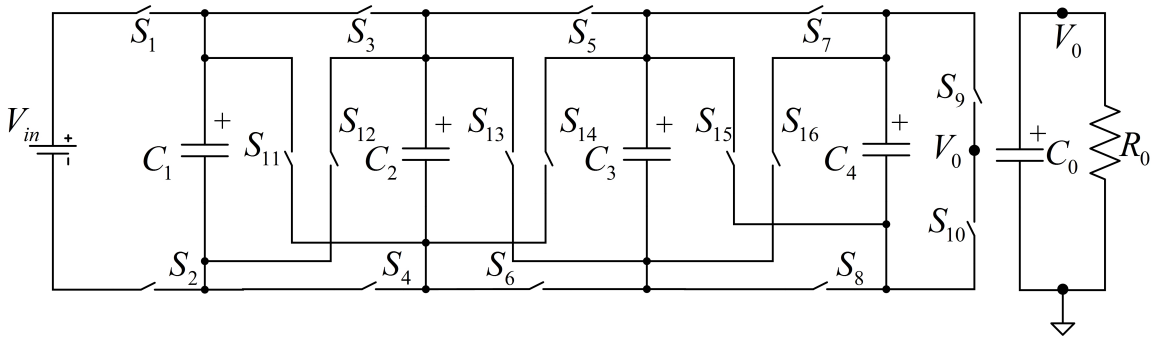


Figure 2.1: Reconfigured SCC network

of $(h,k)^{th}$ generalized signed Fibonacci number are expressed in (2.1).

$$N_n = \sum_{m=0}^{n} A_m \cdot F_{n-m+1} \tag{2.1}$$

where, A_m can be 0 or 1; n, is the maximum number of capacitors which sets the resolution value by incrementing the index m. From Table 2.2, largest $(h,k)^{th}$ Fibonacci

Table 2.1: $(3, 3)^{th}$ Fibonacci weights for n=6.

j	0	1	2	3	4	5	6
F_{n-m+1}	13	9	6	4	3	2	1

number F_{n+1} is shown in the leftmost position for h=3, k=3 and n=6. Signed Fibonacci representation (SGF) is defined for the fractions M_n= N_n/F_{n+1} of the range (0, 1) as follows. Largest $(h,k)^{th}$ Fibonacci number, F_{n+1} can be carried out using (2.1) and the coefficients A_m, $m \geq 1$ should have a three values 0, 1, and -1. From Table 2.2, resolution for any fraction is selected according to less number of capacitors and switches. For example, a resolution of 13 is chosen, that can be achieved

Table 2.2: Generalized Fibonacci numbers

h	k	Expression	1	2	3	4	5	6	7	8
1	1	F_i=$2F_{i-1}$	1	2	4	8	16	32	64	128
1	2	F_i=F_{i-1}+F_{i-2}+1	1	2	4	7	12	20	33	54
2	2	F_i=F_{i-1}+F_{i-2}	1	2	3	5	8	13	21	34
2	3	F_i=F_{i-1}+F_{i-3}+1	1	2	3	5	8	12	18	27
3	3	F_i=F_{i-1}+F_{i-3}	1	2	3	4	6	9	13	19

by either using $(2, 2)^{th}$ series or $(3, 3)^{th}$ series, with m=6 and m=7 respectively but $(2, 2)^{th}$ series is opted because only 5 capacitors need to be used rather than 6 capacitors in $(3,3)^{th}$ series. The SGF can also be represented by a leading coefficient, A_0 as shown in (2.2), where A_0 has a value 0 or 1 (Kushnerov, 2014b).

$$M_n = A_0 + n \sum_{m=1} A_m \cdot \frac{F_{n-m+1}}{F_{n+1}} \tag{2.2}$$

Different SGF codes are derived using same the fraction using (2.2). The M_n parameters are varied for different SGF codes, for example,

$$\left(\frac{5}{6}\right) = 0 \cdot 1 + 0 \cdot \left(\frac{4}{6}\right) + 1 \cdot \left(\frac{3}{6}\right) + 1 \cdot \left(\frac{2}{6}\right) + 0 \cdot \left(\frac{1}{6}\right) = \{0 \quad 0 \quad 1 \quad 1 \quad 0\} \tag{2.3}$$

$$\left(\frac{5}{6}\right) = 0 \cdot 1 + 1 \cdot \left(\frac{4}{6}\right) + 0 \cdot \left(\frac{3}{6}\right) + 0 \cdot \left(\frac{2}{6}\right) + 1 \cdot \left(\frac{1}{6}\right) = \{0 \quad 0 \quad 1 \quad 1 \quad 0\} \tag{2.4}$$

$$\left(\frac{5}{6}\right) = 0 \cdot 1 + 1 \cdot \left(\frac{4}{6}\right) + 0 \cdot \left(\frac{3}{6}\right) + 1 \cdot \left(\frac{2}{6}\right) - 1 \cdot \left(\frac{1}{6}\right) = \{0 \quad 1 \quad 0 \quad 1 \quad -1\} \tag{2.5}$$

$$\left(\frac{5}{6}\right) = 0 \cdot 1 + 1 \cdot \left(\frac{4}{6}\right) + 1 \cdot \left(\frac{3}{6}\right) - 1 \cdot \left(\frac{2}{6}\right) + 0 \cdot \left(\frac{1}{6}\right) = \{0 \quad 1 \quad 1 \quad -1 \quad 0\} \tag{2.6}$$

$$\left(\frac{5}{6}\right) = 1 \cdot 1 + 0 \cdot \left(\frac{4}{6}\right) + 0 \cdot \left(\frac{3}{6}\right) - 1 \cdot \left(\frac{2}{6}\right) + 1 \cdot \left(\frac{1}{6}\right) = \{1 \quad 0 \quad 0 \quad -1 \quad 1\} \tag{2.7}$$

$$\left(\frac{5}{6}\right) = 1 \cdot 1 + 0 \cdot \left(\frac{4}{6}\right) + 0 \cdot \left(\frac{3}{6}\right) + 0 \cdot \left(\frac{2}{6}\right) - 1 \cdot \left(\frac{1}{6}\right) = \{1 \quad 0 \quad 0 \quad 0 \quad -1\} \tag{2.8}$$

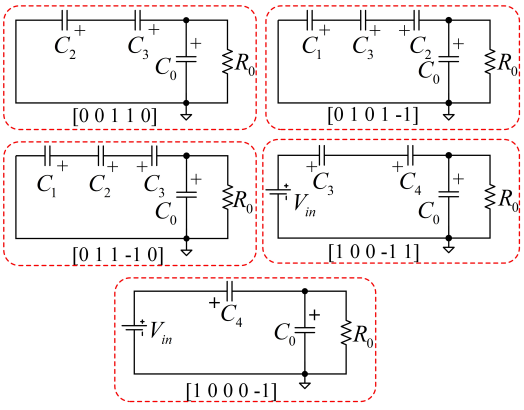
The codes ((2.3)–(2.8)) are validated using spawning rule, based on conditions $h = 3$ and $k = 3$ of series F_i=F_{i-1}+F_{i-3}, which generates $2F_i = F_{i+1} + F_{i-1} + F_{i-3} - F_{i-2}$. Here two 1's are added in SGF code and it provides four carries. In general case, the carry of 1st one moves to 1 bit left, the second moves to one bit right, third moves two bits right and fourth moves three bit right (Kushnerov and Ben-Yaakov, 2013).

2.1.1 Spawning Rule for SGF Code

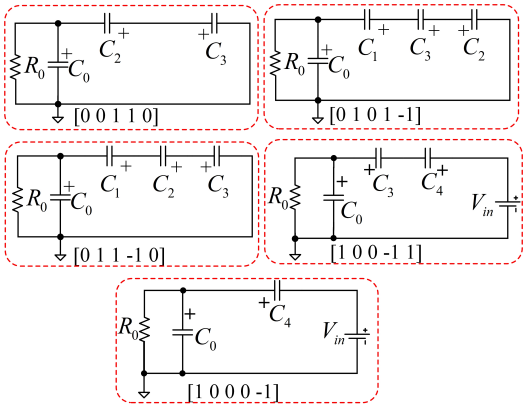
This is an iterative process that begins with EZ- code of M_n. By neglecting the zeros from the left side a "1" is to be added to any element of A_m=1 (Ben-Yaakov and Kushnerov, 2009). The addition of "1" leads to $A_m = 0$ and generates carries. Finally, a "-1" is to be added to $A_m = 0$ for retaining the original value. This procedure creates a new SGF code, which is to be repeated. In the next step this new SGF code becomes the original code and process is repeated for all $A_m = 1$. Furthermore, few corollaries are used for new SGF code generation (Kushnerov and Ben-Yaakov, 2013) and the spawning of SGF code are shown in Table 2.3.

Table 2.3: SGF codes for different fractions of M_n, h=3, k=3

*M*4=1/6					*M*4=5/6					*M*3=1/4				*M*3=3/4			
A_0	A_1	A_2	A_3	A_4	A_0	A_1	A_2	A_3	A_4	A_0	A_1	A_2	A_3	A_0	A_1	A_2	A_3
0	0	0	0	1	0	0	1	1	0	0	0	0	1	0	1	0	0
0	0	0	1	-1	0	1	0	1	-1	0	0	1	1	1	-1	1	0
0	0	1	-1	0	0	1	1	-1	0	0	1	-1	0	1	0	-1	1
0	1	-1	0	0	1	0	0	-1	1	1	-1	0	0	1	0	0	-1
1	-1	0	0	-1	1	0	0	0	-1	–	–	–	–	–	–	–	–



(a) Step-down topology for switched capacitor converter of fraction 5/6



(b) Step-up topology for Switched capacitor converter of fraction 5/6

Figure 2.2: Topology for switched capacitor converter of step-down/step-up configuration.

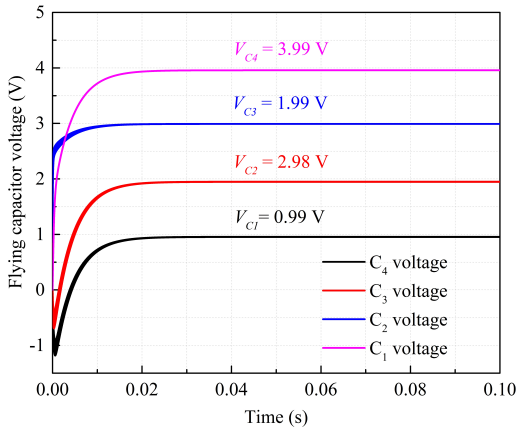
2.1.2 Transforming Multiphase SFN TO SCC Topologies

The rules for transforming multiphase (Ben-Yaakov and Evzelman, 2009, Kushnerov, 2014b) SGF to SCC topologies (step up and step down configuration) are discussed in this Section. The step down and step up topology are shown in Figure 2.2(a) and Figure 2.2(b), respectively where V_{in} is the input voltage, C_1, C_2, C_3, C_4 are the flying capacitors and C_0 is the output capacitor, which is connected parallel to the load R_0. The procedure for transformation is as follows with respect to (2.2),

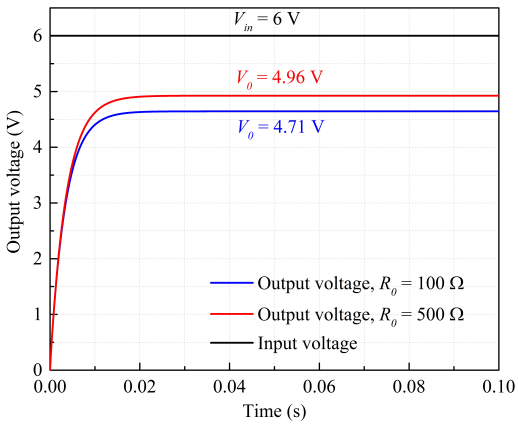
- If A_0 takes the value 1, then V_{in} charges the output with same polarity.
- If A_0 takes the value 0, then V_{in} gets disconnected from the output.
- If A_m takes the value -1, then flying capacitors are connected in charging mode.
- If A_m takes the value 1, then flying capacitors are connected in discharging mode.
- If A_m takes the value 0, then no flying capacitors are connected.

Mathematically, unknown voltages and output voltages of the 5/6 and 1/6 voltage ratios can be derived using KVL. Let us assume that all the flying capacitors depicted in Figure 2.2(a) and Figure 2.2(b) are charged to constant unknown voltages V_1, V_2 , V_3, V_4 and the output capacitor voltage as V_0 which is also unknown. The unknown voltages V_1, V_2 , V_3, V_4, and V_0 are solved using matrix method by applying KVL to each topology in Figure 2.2(a) and Figure 2.2(b) for both step up and step down topologies. The flying capacitors and output voltages are derived using (2.9) and (2.10).

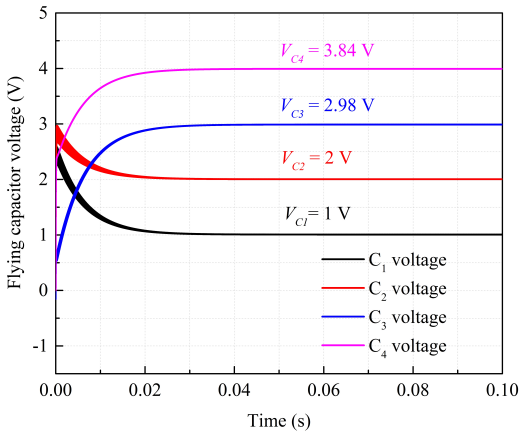
$$\begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1 \\ 1 \end{pmatrix} \cdot V_0 + \begin{pmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & -1 \\ 1 & 1 & -1 & 0 \\ 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & -1 \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} = \begin{pmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{pmatrix} \cdot V_{in} \tag{2.9}$$



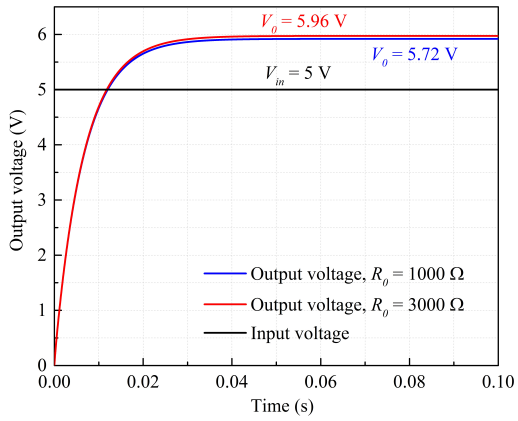
(a) Step down flying capacitor voltages of V_{C1}, V_{C2}, V_{C3}, V_{C4}



(b) Step down output voltage of fraction 5/6



(c) Step up flying capacitor voltages of V_{C1}, V_{C2}, V_{C3}, V_{C4}



(d) Step up output voltage of fraction 5/6

Figure 2.3: Simulation results for 5/6 fraction SCC configuration

$$\begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1 \\ 1 \end{pmatrix} \cdot V_{in} + \begin{pmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & -1 \\ 1 & 1 & -1 & 0 \\ 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & -1 \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} = \begin{pmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{pmatrix} \cdot V_0 \tag{2.10}$$

By solving (2.9) the voltage across the flying capacitors and the output capacitor are given as $V_1 = 4 \cdot V_{in}/6, V_2 = 3 \cdot V_{in}/6, V_3 = 2 \cdot V_{in}/6, V_4 = V_{in}/6$ and $V_0 = 5 \cdot V_{in}/6$. Similarly, by applying KVL to the step-up topologies shown in Fig 2.2(b), it gives

another 4 equations as given in (2.10). By solving (2.10) the voltage across the flying capacitors and the output capacitor are given as $V_1 = 4 \cdot V_0/5, V_2 = 3 \cdot V_0/5, V_3 = 2 \cdot V_{in}/5, V_4 = V_{in}/5$ and $V_0 = 6 \cdot V_{in}/5$. From this it is clear that interchanging the input and output voltages of V_{in} and V_0, results in changing from step-down SCC to step-up SCC (Ben-Yaakov and Kushnerov, 2009).

2.1.3 Simulations

The simulation is performed in PSIM simulation tool. The input voltage is selected as 6V DC and 5V DC source for SCC design. Figure 2.3 shows the simulation results of unsolved fraction, 5/6 SCC. The flying capacitor voltages for step up/step down configuration are depicted in Figure 2.3(a) and Figure 2.3(c) respectively. The output voltages for both step up/step down configuration are depicted in Figure 2.3(b) and Figure 2.3(d) respectively. From (2.9) and (2.10) it is clear that, both theoretical

Table 2.4: Different load conditions of 5/6 voltage ratios

Step-down configuration M_4=5/6			Step-up configuration M_4=5/6		
R_0	V_0	R_{eq}	R_0	V_0	R_{eq}
100	4.57	9.40	1000	5.97	15.7
200	4.78	9.20	1500	5.96	16.7
300	4.85	9.27	2000	5.95	16.8
400	4.89	8.99	2500	5.94	15.1
500	4.908	8.54	3000	5.91	15.2

analysis and simulation are almost the same for a flying capacitor voltage and output voltage of SCC for step-up/step-down configuration. For step down configurations V_{in}= 6 V, V_1=4.89 V, V_2=3.89 V, V_3=2.97 V, V_4=1.98 V and V_0=4.92 V. For step up configurations, V_{in}= 5 V, V_1=1.98 V, V_2=2.98 V, V_3=3.99 V, V_4=4.86 V and V_0=5.982 V. Different load conditions are shown in Table 2.4. The main disadvantage of the 16 switches and 5 capacitors methodology is that it requires more switches and capacitors and the initial charges at the capacitor terminals are in negative directions. It affects SCC topology and the switching losses increases drastically with reduced converter efficiency. To overcome the above problem, the reconfigured Tribonacci sequences are developed with less number of switches and capacitors. Detailed explanation of Tribonacci sequence is explained in the following Section 2.2.

2.2 Tribonacci Sequence with 3 Capacitors and 12 Switches.

The reconfigured proposed switching network for Tribonacci sequence SCC to solve the unsolved voltage ratios is shown in Figure 2.4 where the bidirectional switches are S_1 to S_{12} with inbuilt switch on resistance $R_{on} = 0.4\ \Omega$ and the flying capacitors are C_1 to C_3. The similar steps are followed for solving the missing voltage ratios using the same procedure as discussed in Section 2.1-2.1.2 by changing the spawning rule. The

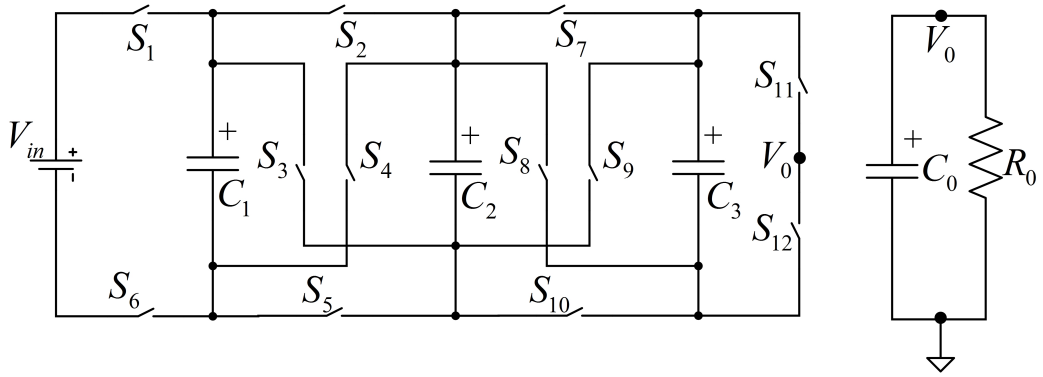


Figure 2.4: 12 switch and 3 capacitor network

new spawning technique, i.e., $F_i = F_{x+1} + F_{x-3} - F_x$ (Makowski and Kushnerov, 2017) has been developed to solve the unsolved fractions with less number of switches and capacitors. Tribonacci sequence is developed for solving missing Fibonacci voltage ratios. Fibonacci numbers are defined as $F_x = F_{x-1} + F_{x-2}$ where arbitrary values are (0, 1) and the sequence is 0, 1, 1, 2, 3, 5, 8, . . . , x^n where x is the integer and n is the number of capacitors. In this sequence the denominator number 6 is not present.

$$T_i = \begin{cases} 1 \quad for \quad x \quad \epsilon \quad \{0, 0, 1\} \\ T_{x-1} + T_{x-2} + T_{x-3} \quad for \quad x \geq 3 \end{cases} \tag{2.11}$$

Tribonacci numbers are defined as, $T_x = T_{x-1} + T_{x-2} + T_{x-3}$, where starting values of the Tribonacci numbers are (0, 0, 1) and the sequence is 0, 1, 1, 1, 2, 4, 7, 13, 24, . . . , x^n. Similarly in this sequence the denominator 6 is not present. The missing fractions are solved using 3 capacitors and 12 switches using (2.11) where the arbitrary values are (0, 1, 0). The different signed generalised Tribonacci (SGT) codes can be derived

for the same fraction of voltage ratio M_n and it is given in (2.12)–(2.15).

$$\frac{5}{6} = 0 + 1 \cdot \frac{3}{6} + 1 \cdot \frac{2}{6} + 0 \cdot \frac{1}{6} \Longrightarrow \{0 \quad 1 \quad 1 \quad 0\} \tag{2.12}$$

$$\frac{5}{6} = 1 + 0 \cdot \frac{3}{6} - 1 \cdot \frac{2}{6} + 1 \cdot \frac{1}{6} \Longrightarrow \{1 \quad 0 \quad -1 \quad 1\} \tag{2.13}$$

$$\frac{5}{6} = 1 + 0 \cdot \frac{3}{6} + 0 \cdot \frac{2}{6} - 1 \cdot \frac{1}{6} \Longrightarrow \{1 \quad 0 \quad 0 \quad -1\} \tag{2.14}$$

$$\frac{5}{6} = 1 - 1 \cdot \frac{3}{6} + 1 \cdot \frac{2}{6} + 0 \cdot \frac{1}{6} \Longrightarrow \{1 \quad -1 \quad 1 \quad 0\} \tag{2.15}$$

The generalized sequence of Tribonacci number with different arbitrary values is

Table 2.5: Different arbitrary values of Tribonacci sequence

a	**b**	**c**	**Sequence**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0	0	1		1	2	4	7	13	24	44	81
0	1	0	$T_n = T_{n-1} + T_{n-2} + T_{n-3}$	1	2	3	6	11	20	37	68
1	1	1		3	5	9	17	31	57	105	193

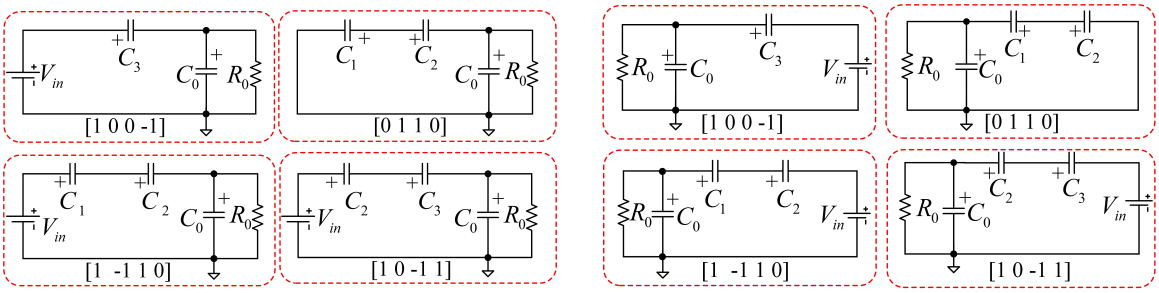
shown in Table 2.5. From Table 2.5 all missing conversion ratios which come under Farey sequence of 2^n, are solved where "n" denotes the number of capacitors ($n = 3$). By spawning rule (Makowski and Kushnerov, 2017) the SGT code is generated and it is discussed in Table 2.6. Assume steady state condition for all the capacitors (C_1,

Table 2.6: Spawning of SGT codes

6/6	3/6	2/6	1/6	0/6	1/6	0/6
0	**1**	**1**	**0**	0		
	+1					
1	0	1	0	1	0	0
	-1					
1	**-1**	**1**	**0**			
		+1				
1	0	0	0	0	0	1
		-1				
1	**0**	**-1**	**1**	0	0	
			+1			
1	0	0	0	0	0	0
			-1			
1	**0**	**0**	**-1**	0		

C_2 and C_3, are charged to fixed voltage), but the capacitor voltages (V_1, V_2, V_3, and

V_0) are unknown.By applying KVL to each topology in Figure 2.5(a), V_1, V_2, V_3, and V_0, of SCC are given by $1/2 \cdot V_{in}$, $1/3 \cdot V_{in}$, $1/6 \cdot V_{in}$, and the output voltage is $5/6 \cdot V_{in}$. Similarly for step up configuration by applying KVL to Figure 2.5(b),



(a) Topology of Step-down SCC

(b) Topology of step-up SCC

Figure 2.5: Topology of Switched capacitor converter, M_3=5/6.

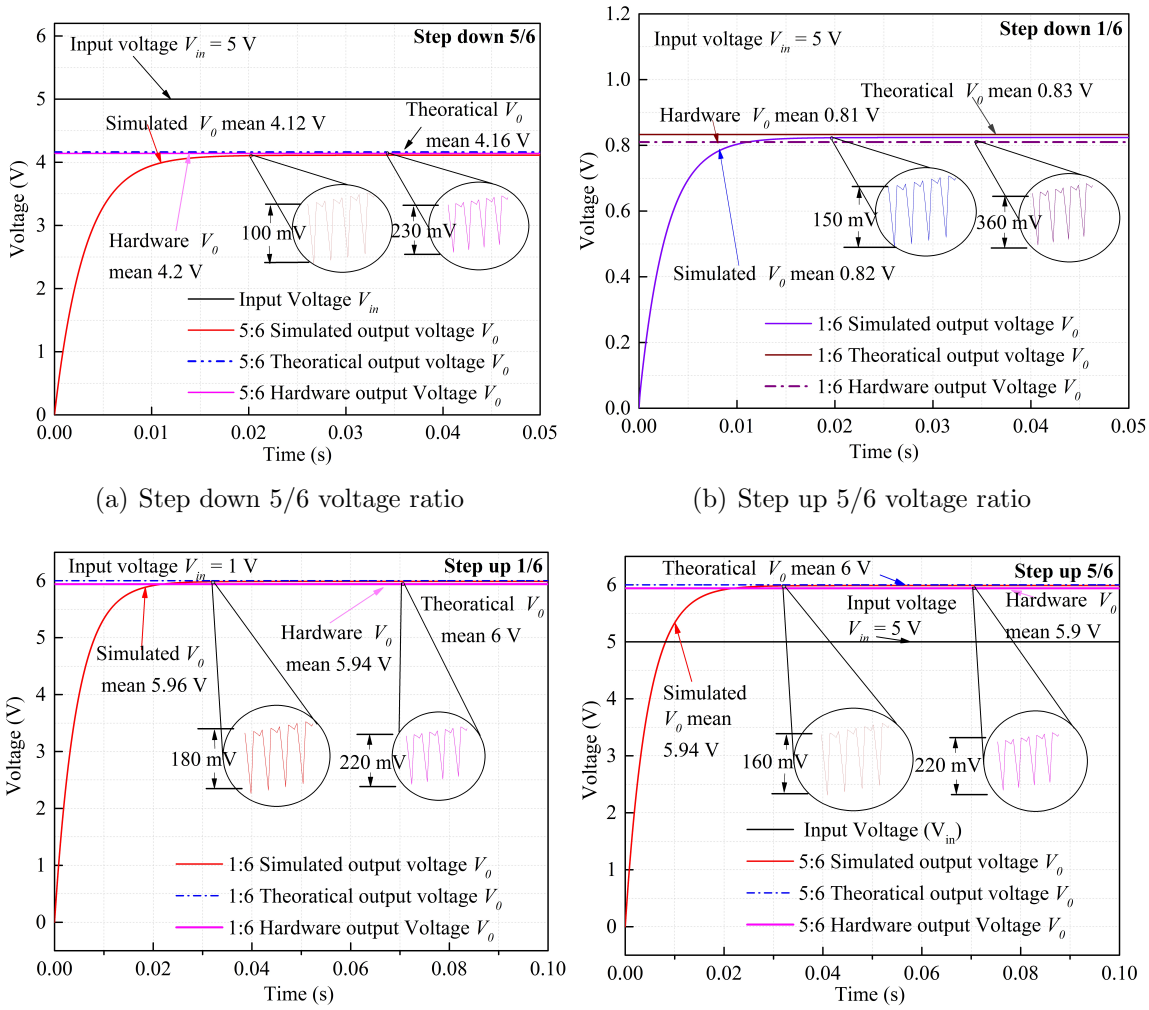
unknown voltages are given by, $1/2 \cdot V_{in}$, $1/3 \cdot V_{in}$, $1/6 \cdot V_{in}$, and the output voltage is $V_0 = 6/5 \cdot V_{in}$.

2.2.1 Simulation Results, Experimental Results and Discussion:

Figure 2.6(a) and Figure 2.6(b) illustrate the simulation, theoretical and experimental results of step down 5/6 and 1/6 voltage levels of frequency 100 kHz. Similarly Figure 2.6(c) and Figure 2.6(d) illustrate the simulation, theoretical and experimental results of step up 1/6 and 5/6 voltage levels of frequency 100 kHz. From Table 2.7 it is clear that modelled and simulated results are in good agreement to verify the proposed converter fraction. Switching Frequency (f_s) is varied accordingly to verify the proposed converter efficiency. PIC controller is used for generating pulse pattern for bidirectional switches, which is discussed in APPENDIX A. Figure 2.7(a) shows the SCC prototype[1]. Figures 2.7(b)-2.7(f) show the output voltage of V_0 for an voltage levels of ($V_0 = 5/6V_{in}$ and $V_0 = 1/6V_{in}$). Figures 2.6 and 2.7(b), 2.7(c) show good agreement for hardware and simulation output. For hardware[2] input (V_{in}) is treated as ≅5.1 V for step-down configuration and ≅1.2 V for step-up configuration because MAX4678 switch has the maximum voltage rating of 10 V (Abraham et al., 2018).

[1]Proteous model of Fibonacci SCC is shown in FigureA.1

[2]PCB Fibonacci SCC circuit is shown in Figure A.2



(a) Step down 5/6 voltage ratio

(b) Step up 5/6 voltage ratio

(c) Step down 1/6 voltage ratio

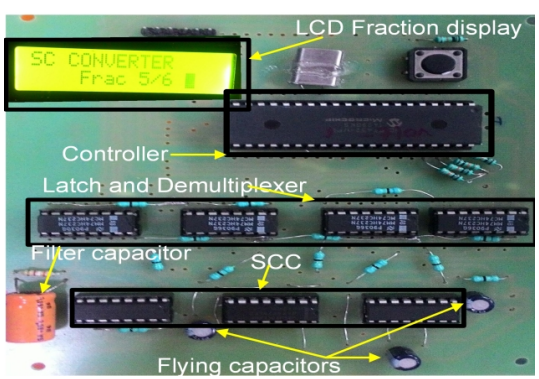
(d) Step up 5/6 voltage ratio

Figure 2.6: Simulation, Theoretical, experimental results of 5/6 and 1/6 voltage ratios.

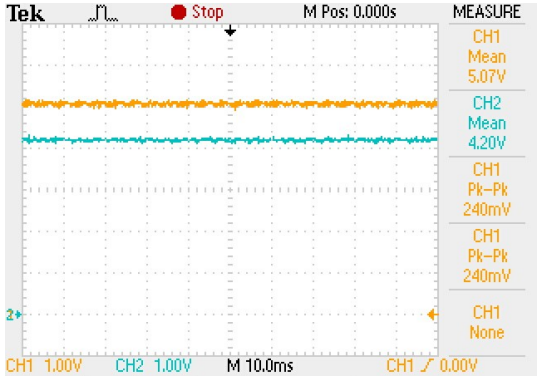
Figure 2.8 shows the family of Fibonacci SCC voltage levels.

Table 2.7: Modelled, simulated and experimental comparison of ($V_o = 5/6V_s$)

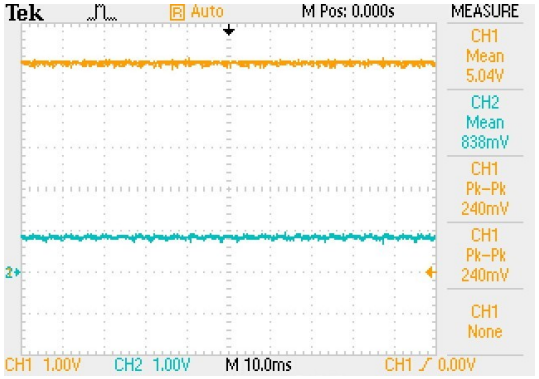
Frequency [kHz]	$V_o = 5/6V_s$			η %
	Model [V]	Simulated [V]	Hardware [V]	
5	4.12	4.9	4.9	83.2
10	4.15	4.11	4.10	98.5
25	4.16	4.11	4.10	98.5
50	4.16	4.12	4.13	99.2
100	4.16	4.12	4.13	99.2



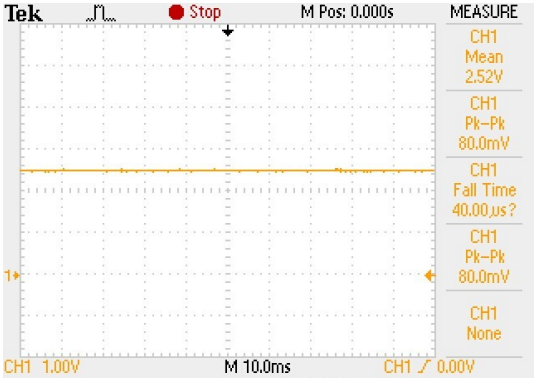
(a) Prototype[a] setup of Fibonacci SCC



(b) Output voltage of fraction 5:6



(c) Output voltage of fraction 1:6



(d) Flying capacitor[b] voltage C_3

(e) Flying capacitor voltage C_2

(f) Flying capacitor voltage C_1

Figure 2.7: Experimental results[c] of unsolved voltage ratios (1/6 and 5/6) step down Fibonacci SCC.

[a]Board size is shown in Appendix E.1(a)
[b]The flying capacitor (C_1 - C_3) voltage is approximately same for both the unsolved voltage ratios.
[c]Input voltage used for experimental setup is $\approx$ 5.00 - 5.09 V.

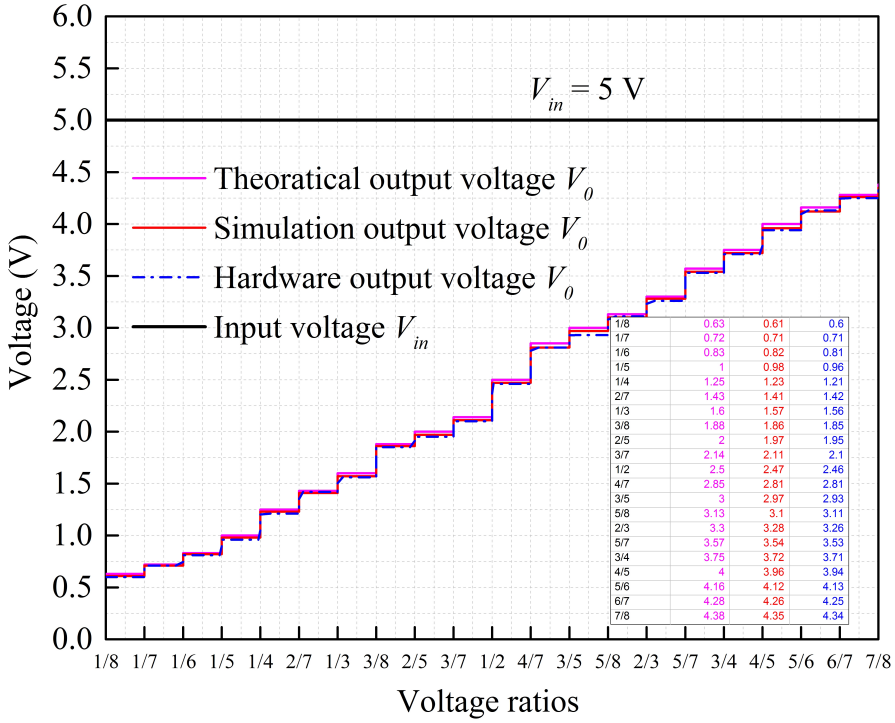


Figure 2.8: Family of Fibonacci switched capacitor target ratios (Ben-Yaakov and Kushnerov, 2009, Kushnerov, 2014b)

2.3 Analysis of Equivalent Resistance for Unsolved Voltage Ratios

In this section, using charge balance equation, total equivalent resistance of SCC is derived, where the flying capacitors are always connected in series (Evzelman and Ben-Yaakov, 2013). The R_{eq} calculation follows the same procedure as discussed in (Kushnerov, 2014b).

2.3.1 16 Switches and 5 Capacitors

The equivalent resistance of SCC, R_{eq} (Kushnerov, 2014b) is given in (2.16),

$$R_{eq} = \frac{1}{2f_s} \sum_{i=1}^{n+1} \frac{k_i^2}{c_i} \coth \frac{\beta_i}{2} \tag{2.16}$$

where, i, is the topology number which increases in the ascending order upto $n+1$, $k_i = I_i/I_o$ where, I_i is average topology current, I_o is average output current and $\beta_i = t_i/\tau_i$ is the ratio of time allotted to topology where time constant is given by $\tau_i = R_i C_i$. For expressing the k_i value all flying capacitor receiving charges must be equal to output charge and equal time duration is set to configure all SCC topologies, which can be derived using linear equation given in (2.17).

Table 2.8: Unknown currents for 1/6 and 5/6 voltage ratios

M_4=1/6				M_4=5/6			
C_1	C_2	C_3	C_4	C_1	C_2	C_3	C_4
0	0	0	I_1	0	I_1	I_1	0
0	0	I_2	$-I_2$	I_2	0	0	I_2
0	I_3	$-I_3$	0	I_3	0	I_3	$-I_3$
I_4	$-I_4$	0	0	I_4	I_4	I_4	0
$-I_5$	0	$-I_5$	I_5	0	0	$-I_5$	I_5
$-I_6$	0	0	$-I_6$	0	0	0	$-I_5$

$$\sum_{i=1}^{n+1} A_{i,m} I_i = 0 \sum_{i=1}^{n+1} A_{i,n+1} I_i = I_0 \tag{2.17}$$

where m is SCC topology count and $A_{i,m}$ is SGF coefficients. From (2.17), a fixed value of m , can be obtained as a product of transposed m^{th} column and column of unknown currents, I_i. For example, M=5/6 is considered for solving the unknown currents which are derived using Table 2.8. From (2.18) – (2.22), we derived the values of unknown currents I_1, I_2, I_3, I_4, I_5, I_6 in terms of I_0 shown in (2.23). We considered the particular solution of (2.23), when unknown current is equal to zero,

$$I_2 + I_3 + I_4 = 0 \tag{2.18}$$

$$I_1 + I_4 = 0 \tag{2.19}$$

$$I_1 + I_3 - I_4 - I_5 = 0 \tag{2.20}$$

$$I_2 - I_3 + I_5 - I_6 = 0 \tag{2.21}$$

$$I_1 + I_2 + I_3 + I_4 + I_5 + I_6 = I_0 \tag{2.22}$$

the particular row is eliminated. Here second row in 5/6 Table 2.3 is eliminated because unknown current $I_2 = 0$. Hence second topology is not configured.

Table 2.9: Coefficients required for calculation of R_{eq} for $n = 1, 2..4$.

i	M_4=1/6		M_4=5/6		M_3=1/4		M_3=3/4	
	I_i/I_o	C_i/C	I_i/I_o	C_i/C	$I_i/_o$	C_i/C	I_i/I_o	C_i/C
1	2/5	1	1/6	1/2	1/4	1	1/4	1
2	1/5	1/2	1/6	1/3	1/4	1/4	1/4	1/2
3	1/5	1/2	1/6	1/3	1/4	1/2	1/4	1/2
4	1/5	1/2	3/6	1/2	1/4	1	1/4	1
5	1/5	1/2	2/6	1	–	–	–	–

$$I_1 = I_3 = -I_4 = \frac{I_0}{6}; I_5 = \frac{3I_0}{6}; I_6 = \frac{2I_0}{6}; I_2 = 0 \tag{2.23}$$

The coefficients required for R_{eq} solution for M_n, n=1, ..., 4. are provided in Table 2.9. For obtaining the R_{eq}, substitute the value of β_i, β and Table 2.9 coefficients in (2.16) where $\beta = \frac{t}{RC}$. Equivalent resistance for different fraction is shown in Table 2.10.

$$R_{eq} = \frac{1}{36}\frac{T_s}{C}\left[10\beta\coth(\beta) + 3\coth(\frac{3\beta}{2}) + 2\coth(\frac{\beta}{2})\right] \tag{2.24}$$

$$R_{eq} = \frac{5}{36}R\left[10\beta\coth(\beta) + 3\coth(\frac{3\beta}{2}) + 2\coth(\frac{\beta}{2})\right] \tag{2.25}$$

Table 2.10: Equivalent Resistance

M_n	Equivalent Resistor Expression	$\beta \underrightarrow{lim} 0 R_{eq}$	R_{eq} Ω
M_4=1/6	$\frac{5}{25}R\beta\left[2\coth\left(\frac{\beta}{2}\right) + 2\coth(\beta)\right]$	$\frac{9}{5}$ R	8.64
M_4=5/6	$\frac{5}{36}R\beta\left[10\coth(\beta) + 3\coth\left(\frac{3\beta}{2}\right) + 2\coth\left(\frac{\beta}{2}\right)\right]$	$\frac{20}{9}$ R	10.6
M_4=3/4	$\frac{4}{16}R\beta\left[2\coth(\beta) + \coth\left(\frac{\beta}{2}\right)\right]$	R	4.8
M_4=1/4	$\frac{1}{4}R\beta\left[2\coth(\beta) + \coth\left(\frac{\beta}{2}\right)\right]$	R	4.8
M_4=2/3	$\frac{1}{6}R\beta\left[4\coth(2\beta) + \coth\left(\frac{\beta}{2}\right) + 3\coth\left(\frac{3\beta}{2}\right)\right]$	R	4.8

2.3.2 12 Switches and 4 Capacitors

Similarly, the equivalent resistance for Tribonacci sequence can be solved using the same procedure as discussed in the previous Section.

A = (Maksimovic and Dhar, 1999)

B = (Favrat et al., 1998)

Table 2.11: Comparison of voltage ratios

Parameters	A*	B*	C*	D*	E*	Fibonacci SCC
Voltage ratio	1	1	1	3	5	21
Input voltage	2 or 3	1.5	1.2	2	1.2	2.5 or 3
Flying capacitor	4	2	—	2	12	3
Frequency, Hz	10 M	100 k-10 M	70 -19 M	10 M- 800 M	15 M	10 k-100 k
Peak Efficiency	68%	75%	75%	79.76%	74%	82%

C = (Jung et al., 2014)

D = (Le et al., 2011)

E = (Ramadass and Chandrakasan, 2007)

2.4 Conclusion

The unsolved voltage ratios of series 1, 2, 3, 4, 6, 9, 13, 19.... were derived using generalized Fibonacci series for both step up/step down configuration and were simulated and verified theoretically. Comparison between previous SCC in the literature and in this work was done and presented in Table 2.11. Finally, theoretical results and simulation results of equivalent resistance were verified by varying load conditions.

Chapter 3

DUAL INPUT SINGLE OUTPUT SCC

In Chapter 1 it was pointed out that several SCC topology families had been developed for generating maximum voltage ratios using reduced component counts. The first topology, Single input single output (SISO) SCC was discussed in Chapter 2, using the concept of Fibonacci voltage ratios. In that, maximum voltage ratios were generated but all the voltage ratios were related to Fibonacci series and it was not possible to generate addition of two voltage ratios. Finally, to develop summation, multiplication and divison, DISO was designed. In this chapter, DISO is designed for developing standby inputs. 15 output voltage ratios are developed by reconfiguring the switches and flying capacitor connections. Different targeted output voltages are generated to operate with low input/output voltages. In this DISO only two switching phases (ϕ_c and ϕ_t) are used for charging and discharging the capacitors. The DISO is easy to implement in on-chip due to its small size and light weight and more efficiency.

Parts of this Chapter were previously published at the Electronics letter, IET, 2018 (Abraham, Subburaj et al., 2018).

3.1 Proposed DISO SCC Architecture

The DISO SCC is shown in Figure 3.1. It works for 13 voltage ratios using 9 CMOS switches ($S_{b1} - S_{b9}$), 2 flying capacitors (C_{fly1} and C_{fly2}) and one filter capacitor C_{out}. Additional 2 inversion voltage ratios are discussed in Section 3.5 and brief explanation

is offered in the following Chapter 5. The pulse pattern of all voltage ratios is given in Table 3.1. For each voltage ratio, a predetermined pulse sequence is generated for controlling the switches. Two phases (ϕ_c and ϕ_t) are used to charge and discharge

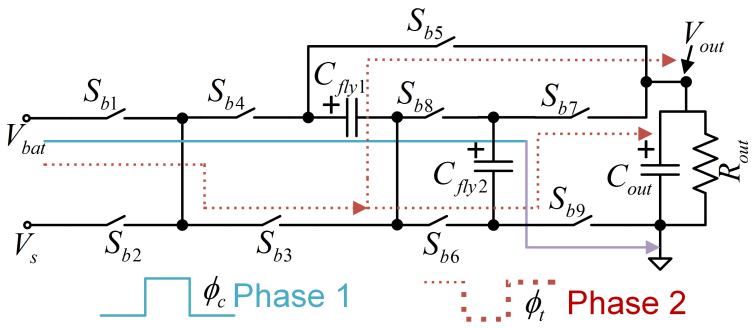


Figure 3.1: Proposed Buck - Boost SCC

the capacitors as shown in Figure 3.1. Yet another feature of this converter is that all the 15 voltage ratios are achievable with two phase operation against multi phase gating in Fibonacci type of SCC. The work presented in (Abraham et al., 2017) has 14 switches which includes 4 diodes that can considerably lower the efficiency due the forward diode voltage drop. Therefore the attempt in this work is to generate 15 against 11 voltage ratios in (Abraham et al., 2017), using only 9/10 CMOS switches and no diodes. This reduces the component count which increases efficiency at the same time requires less chip space.

3.2 Working Principle of the DISO SCC

From Table 3.1 for state 6, $S_{b1}, S_{b4}, S_{b8}, S_{b9}$ are connected in phase 1 (ϕ_c) the charging phase and $S_{b2}, S_{b3}, S_{b5}, S_{b6}, S_{b7}$ are connected in phase 2 (ϕ_t) the discharging phase. In phase 1 the capacitors (C_{fly1} and C_{fly2}) are connected through the switches in series and share half the input voltage V_{bat} from battery. In phase 2 the capacitors (C_{fly1} and C_{fly2}) connect in parallel and together with the second source V_s. The second voltage source can be fed from solar if desired, and the generated voltage is delivers to the load. To model the equivalent resistance R_{eq} in Figure 3.2 which represents the complete model of SCC to predict the output voltage, the reduced equivalent circuit of the converter for state 6 is developed in Figure 3.3. The CMOS switch resistance is taken as r_{on} and the capacitor ESR is $resr_1$ and $resr_2$.

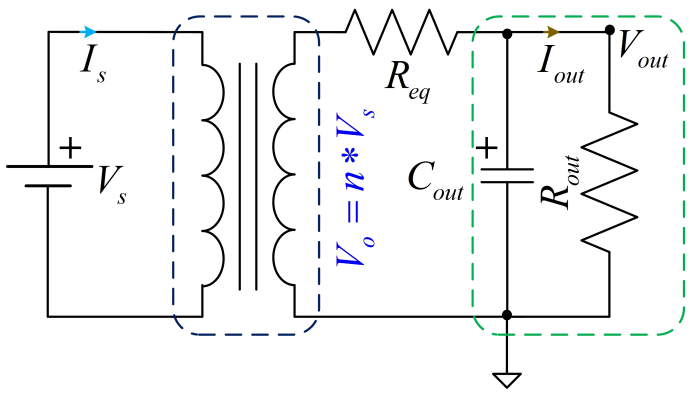


Figure 3.2: Model of proposed circuit (Abraham et al., 2017)

3.3 Theoretical Framework of DISO SCC

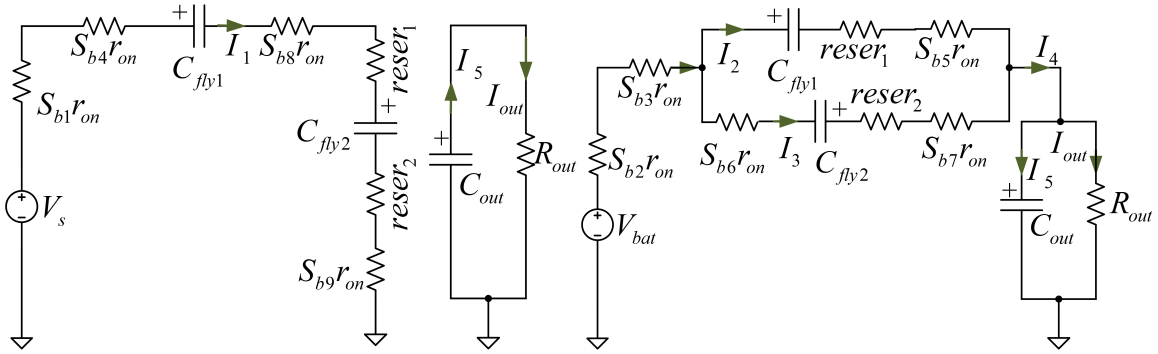
Theoretical analysis is performed on SCC for the 6^{th} state ($V_s + (V_{bat} * 0.5)$) of Table 3.1 by utilizing two different independent sources. The charging and discharging phase path is as shown by solid and dotted lines in Figure 3.1. Similar analysis can be considered for other voltage ratios mentioned in Table 3.1. The authors in (Evzelman and Ben-Yaakov, 2013) have proposed an average current based conduction losses model to develop R_{eq}. This analysis is derived from the basic circuit theory con-

Table 3.1: 13 States and voltage ratios of the Proposed Converter

States	voltage ratios	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	S_{b7}	S_{b8}	S_{b9}
1	$V_{bat} * 2$	1	-	ϕ_t	ϕ_c	ϕ_t	ϕ_c	-	-	ϕ_c
2	$V_s * 2$	-	1	ϕ_t	ϕ_c	ϕ_t	ϕ_c	-	-	ϕ_c
3	$V_s + V_{bat}$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	ϕ_c	-	-	ϕ_c
4	$V_{bat} * 1.5$	-	1	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
5	$V_s * 1.5$	1	-	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
6	$V_s + (0.5 * V_{bat})$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
7	$V_{bat} + (0.5 * V_s)$	ϕ_t	ϕ_c	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c
8	$V_{bat} * 0.5$	ϕ_c	-	-	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	1
9	$V_s * 0.5$	-	ϕ_c	-	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	1
10	V_{bat}	ϕ_c	-	-	ϕ_c	ϕ_t	1	-	-	1
11	V_s	-	ϕ_c	-	ϕ_c	ϕ_t	1	-	-	1
12	$(V_{bat} + V_s) * 0.5$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	-	ϕ_t	ϕ_c	1
13	$(V_{bat} + V_s) * 0.75$	ϕ_c	ϕ_t	ϕ_t	ϕ_c	ϕ_t	ϕ_t	ϕ_t	ϕ_c	ϕ_c

cept of approximating the SCC circuit in any operating phase to a First order RC network. During a time period corresponding to a switching frequency, if charging

and discharging processes in C_{fly1} and C_{fly2} are completed, then the transition state is fully charged (FC) or slow switching limit (SSL). When the switching frequency is small or time period is large then the SSL and FC occurs in the circuit. On the contrary, if switching frequency is large, then time period is small and the flying capacitors cannot completely charge and is said to be in the zero charge (ZC) or fast swicthing limit (FSL) mode where the current is constant in C_{fly1} and C_{fly2} (Abraham et al., 2017, Evzelman and Ben-Yaakov, 2013). The average capacitor current



(a) ϕ_c state (b) ϕ_t state

Figure 3.3: Equivalent circuit of series-parallel SC Converter (Abraham et al., 2017)

in ϕ_c and ϕ_t is mapped to the I_{out}, given by (Evzelman and Ben-Yaakov, 2013) and (Abraham et al., 2018), where R_{eq} referred in Figure 3.2 is sum of the equivalent resistance defined by both the charge and discharge phases. Figure 3.3 shows the equivalent circuit of SC converter.

$$P_{equi} = I_{out}^2 R_{equi} \tag{3.1}$$

If $T_{\phi c}$ and $T_{\phi t}$ are the time periods during the ϕ_c and ϕ_t , then

$$\lambda_{\phi c} = \left[\left(T_{\phi c}/\left(4s_{b\phi c} * r_{d(on)} + 2esr_{\phi c}\right)(C_{fly}/2)\right)\right]/2 \tag{3.2}$$

$$\begin{aligned} \lambda_{\phi t} \quad = \quad & [(T_{\phi t}/(3s_{b\phi t} * r_{d(on)} + esr_{\phi t}/2) * \\ & (2C_{fly} * C_{out}/2C_{fly} + C_{out}))]/2 \end{aligned} \tag{3.3}$$

During ϕ_c and ϕ_t to get R_{equ} the corresponding equivalent resistances are given in (3.4) and (3.5),

$$R_{equ\phi c} = \frac{0.125 * \coth \lambda_{\phi c}}{f_{switch} * 0.5 * C_{fly}} \tag{3.4}$$

$$R_{equ\phi t} = \frac{0.5 * \coth \lambda_{\phi t}}{f_{switch} * ((2 * C_{fly} * C_{out})/(2C_{fly} + C_{out}))} \tag{3.5}$$

By combining and approximating equations (3.4) and (3.5), R_{eq} of converter is

$$R_{equ} = \frac{1}{4 f_{switch} * C_{fly}} \left[\coth\left(\lambda_{\phi c}\right) + \coth\left(\lambda_{\phi t}\right)\right] \tag{3.6}$$

Once R_{eq} is known V_{out} referred in Figure 3.2(b) can be calculated since V_o, I_{out} and

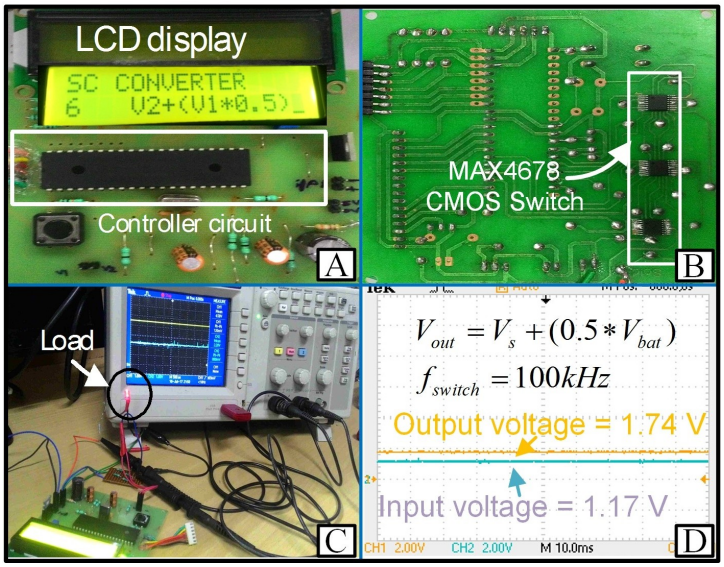


Figure 3.4: Hardware Prototype

R_{out} are also known. The model derived R_{eq} [1] and the calculated V_{out} for different frequencies are shown in Table 3.2. Both the source voltages are assumed to be the same and is taken as 1.17 and 2 for 100 kHz and 5 kHz respectively.

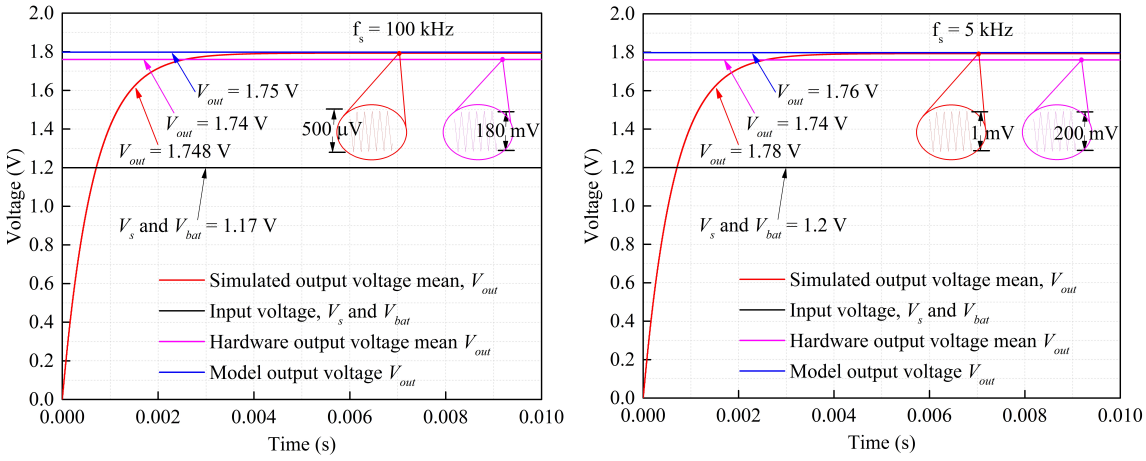
[1] General MATLAB code for R_{eq} calculation is appended in APPENDIX B.1

Table 3.2: Modelling, Simulation and Hardware Comparison for 6^{th} State

f_{switch} kHz	$\lambda_{\phi c}$	$\lambda_{\phi t}$	R_{eq}	V_{out} Model	V_{out} Simulation	V_{out} Hardware	η Hardware
100 (Source = 1.17 V)	3.24	1.43	0.25	1.75	1.75	1.74	99 %
5 (Source = 1.2 V)	1.62	7.17	5	1.76	1.78	1.74	96.5 %

3.4 Implementation and Key Results

For validation of the converter the protoype developed is shown in Figure 3.4. The switches $S_{b1} - S_{b9}$ used are of bi-directional SPST analog switch manufactured by MAXIM INTEGRATED circuits MAX4678. The flying capacitor and filter capacitor are manufactured by SANYOUNG 22 μF, 50 V with an ESR of 100 mΩ. The load current ranges between 10 μA and 10 mA at an output voltage level of 0.55 V to 2.5 V. Figure 3.4A shows a prototype[2] of PIC16F controller which is used to generate



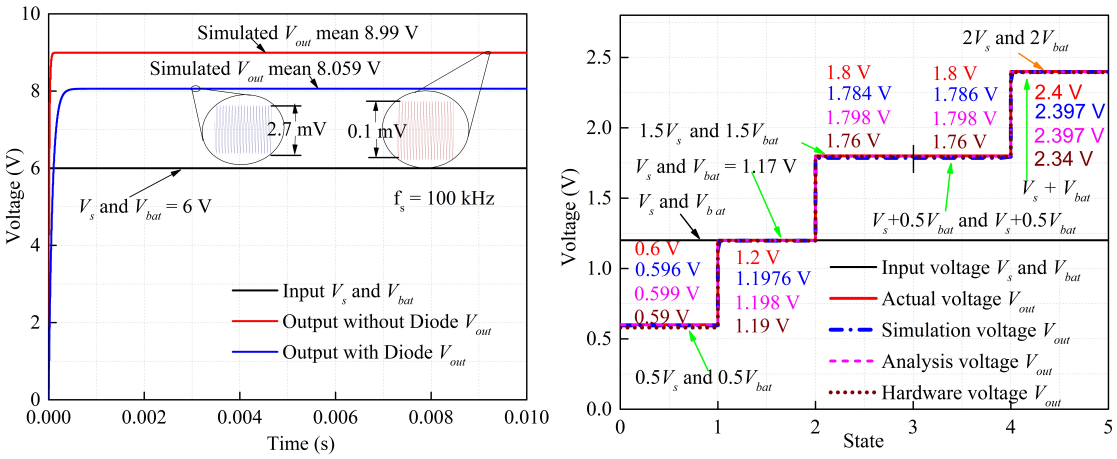
(a) 100 kHz (b) 5 kHz

Figure 3.5: Simulation, Analysis and Experimental Results for State 6 Frequencies.

switching sequence for CMOS switch and LCD are used to display the particular state of the proposed converter. The dead time is 10 ns. Figure 3.4B shows the MAX4678 SMD bidirectional switch and the prototype[3] size is 5 cm x 5 cm including

[2]Board size of front view and rear view is shown in Figure E.1(b) and Figure E.1(c)
[3]PCB drawing board is shown in Figure B.1

all components. Figure 3.4C shows the test bench of the proposed prototype where LED is used as a load which is highlighted in the circle. Experimental result[4] shown in Figure 3.4D corresponds to an input voltage of 1.17 V and the output voltage is 1.76 V which is in good agreement of state 6. Two frequencies 100 kHz (Figure 3.5(a)) and 5 kHz (Figure 3.5(b))with a duty cycle of 50% are implemented and shown in Figure 3.5. We can conclude from Figure 3.5 that for those frequencies, simulation, modeling and experimental results are in good agreement with each other as shown in Table 3.2. Figure 3.6(a) shows the comparison of work in (Abraham et al., 2017)



(a) With and without diode (Input Voltage = 6 V)

(b) Voltage ratio of all 13 States of the DISO

Figure 3.6: Comparison results of output voltage of DISO SCC.

with diode and the proposed topology in this Chapter without diode. The efficiency increases considerably and is greater than (92%). The size of the prototype is very much smaller than the size of existing converter discussed in (Abraham et al., 2017), with two more additional voltage ratios, is an additional feature of the proposed converter. Figure 3.6(b) shows comparison of the first 11 voltage ratios derived by the switching sequence referred in Table 3.1 for modelling, simulation and hardware results of the proposed circuit. For regulation first method is to change the voltage ratios by proper gating to get the corresponding voltage and second method is to adopt a variable switching frequency to vary R_{eq} which in turn gives desired output variable V_{out}. This can be verified in Table 3.3 as it is 1.74 V for 1.17 V input with

[4]Proteous circuit is shown in Figure B.2

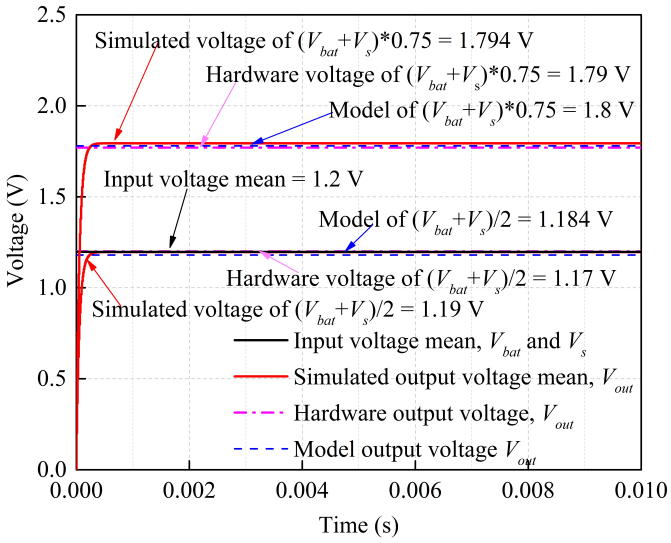


Figure 3.7: Simulation, analysis and experimental results of state 12 & 13

frequency 100 kHz against 1.74 V for 1.2 V at 5 kHz. Figure 3.7 shows the simulation, analysis and experimental results of State 12 & 13.

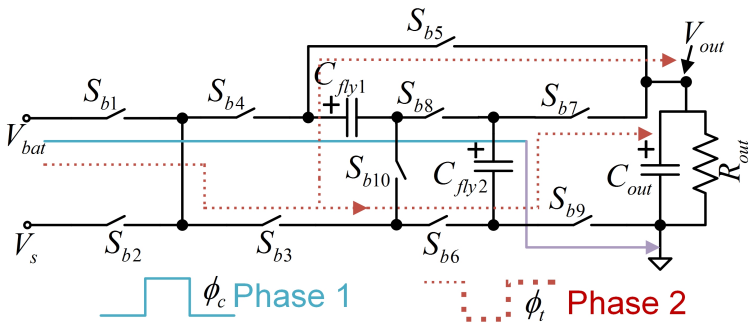


Figure 3.8: Proposed SCC in Inversion Mode (Abraham et al., 2018)

3.5 Modified Circuit

With the addition of one more switch S_{b10}, two more voltage ratios in the inversion mode (Abraham et al., 2018) can be realised. The circuit diagram for inversion mode is shown in Figure 3.8 and the switching states are explained in Table 3.3. The complete results are shown in Figure 3.9.

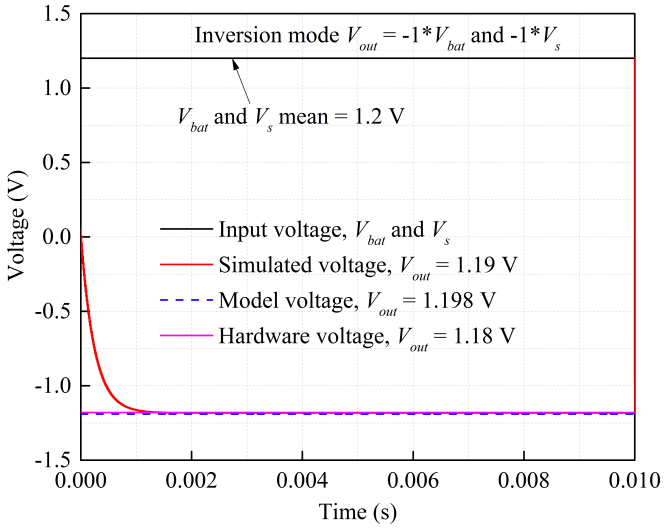


Figure 3.9: Simulation, analysis and experimental results of state 14 & 15

Table 3.3: Inversion States

States	Voltage ratios	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{b5}	S_{b6}	S_{b7}	S_{b8}	S_{b9}	S_{b10}
14	$V_{bat} * -1$	ϕ_c	-	ϕ_c	-	1	1	ϕ_t	ϕ_c	ϕ_t	ϕ_t
15	$V_s * -1$	-	ϕ_c	ϕ_c	-	1	1	ϕ_t	ϕ_c	ϕ_t	ϕ_t

Table 3.4: Comparsion of existing SCC

Parameter	A*	B*	C*	D*	This Work
Voltage ratios	2	1	2	11	15
No of switches	15	4	7	14	11
No of capacitors	4	1	2	2	2
No of diodes	-	-	-	5	-
Output voltage	1 V	36 V	5.4 V	9 V	10 V
Output current	250 mA	120 mA	120 mA	120 mA	100 mA
Efficiency	-	-	-	>85%	>95%
No of inputs	1	2	1	2	2

A* = (Le et al., 2011)

B* = (Yuanmao and Cheng, 2012, Yuan-mao and Cheng, 2013)

C* = (1.5x/2x High-Efficiency White LED Charge Pumps, 2014)

D* = (Abraham et al., 2017)

3.6 Conclusion

A reconfigurable highly efficient CMOS based dual input variable output buck boost switched capacitor converter for low power applications is discussed and verified in this chapter. Compared to other topologies in SCC, DISO is capable of generating 15 voltage ratios with less number of switches and capacitors which is discussed in Table 3.4. The converter delivers high efficiency in open loop conditions.

Chapter 4

DUAL INPUT DUAL OUTPUT SCC

In Chapter 3 DISO SCC was discussed which is similar to DIDO, but the non unity gain voltage ratios are not possible to develop in DISO and maximum 15 voltage ratios can be possible. The main contribution of this Chapter is developing two outputs in single converter, which generates coupled outputs and decoupled outputs. DIDO SCC is developed for 56 voltage ratios which generates dual output voltages. One of the output port will generate different voltages, and the second port will generate different voltage ratios based on switching sequence. DIDO is easy to fabricate in single ICs due to its small size and higher output voltages with less number of components.

Parts of this chapter was presented at the TENCON 2017, in Penang, Malaysia (Zhaikhan et al., 2017) and published in the IET Circuits, Devices & Systems, in December 2018 (Subburaj et al., 2018b).

4.1 Circuit Description

The DIDO SCC configuration is illustrated in Figure 4.1 and it consists of 2 capacitor series-parallel operation with 11 bidirectional switches. The main advantage of the circuit is that both loads can appear in the same topology so the DIDO SCC generates 56 voltage ratios with charging and discharging of the flying capacitors. It is possible to configure one of the outputs to certain voltage, and use this value to generate different voltage ratios in the second output. All the 56 voltage ratios are shown in

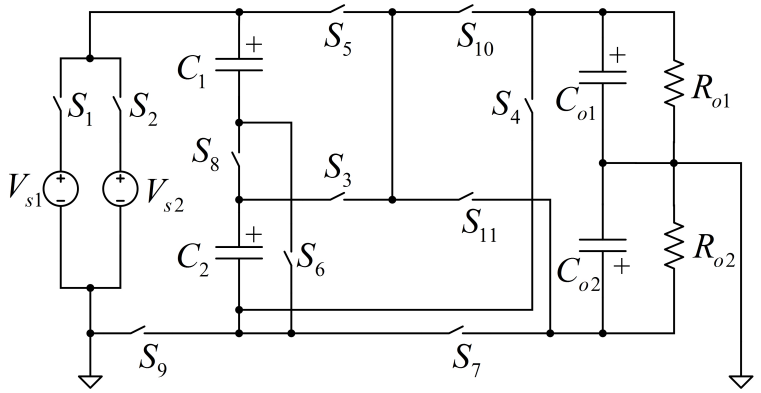


Figure 4.1: DIDO SCC

Table 4.1. DIDO SCC could implement summation of inputs similar voltage ratios as

Table 4.1: 56 voltage ratios

*Voltage ratios	No. of voltage ratios	Remarks
$V_{ok} = V_{si}$ and $V_{on} = 0.5 * V_{sj}$.	8	-
$V_{o1} = 1/3 * V_{si}$ and $V_{o2} = 1/3 * V_{sj}$.	2	$i \neq j$
$V_{o1} = 2/3 * V_{si}$ and $V_{o2} = 2/3 * V_{sj}$.	2	$i \neq j$
$V_{ok} = 1/3 * V_{si}$ and $V_{on} = 2/3 * V_{sj}$.	8	-
$V_{ok} = V_{si}$ and $V_{on} = 1/3 * V_{sj}$.	8	-
$V_{ok} = V_{si}$ and $V_{on} = 2/3 * V_{sj}$.	8	-
$V_{ok} = V_{si}$; $V_{on} = (0.5 * V_{s1}) + (0.5 * V_{s2})$.	4	-
$V_{ok} = 2 * V_{si}$; $V_{on} = (2 * V_{s1}) + (2 * V_{s2})$.	4	-
$V_{ok} = 2 * V_{si}$ and $V_{on} = 1.5 * V_{sj}$.	4	-
$V_{ok} = 2 * V_{si}$ and $V_{on} = V_{sj}$.	4	-
*V_{ok}/V_{on} = output voltage; V_{si}/V_{sj} = input voltage; where, $i, j, n, k = 1, 2$; $n \neq k$		

discussed in Abraham et al. (2017), where the SCC is implemented as 11 voltage ratios using 2 capacitors, 9 switches and 5 diodes. The limitation is that only one of the inputs can have non-unity gain. To overcome those issues DIDO SCC is implemented by (Zhaikhan et al., 2017) and the detailed working principle is explained using two different output[1] cases.

[1]Decoupled and Coupled

4.1.1 Operation of Decoupled Case

For simplicity the voltage ratio, $V_{o1} = V_{s1}$ and $V_{o2} = (0.5 * V_{s1})$ is considered for demonstration. To configure the considered voltage ratio, multiphase switching is used to generate four phases $(\phi_1, \phi_2, \phi_3, \phi_4)$ as shown in Figure 4.2. In phase 1 ϕ_1 flying capacitors are charged in series and in ϕ_2, flying capacitors are discharged in parallel which generates the output voltage $(V_{o2} = 0.5 * V_{s1})$. In the ϕ_3 capacitors are charged again, capacitor voltage level becomes $(0.5 * V_{s1})$. Similarly for ϕ_4 newly charged parallelly connected capacitors get the voltage level of $(0.5 * V_{s1})$. Hence results in $(0.5 * V_{s1}) + (0.5 * V_{s1})$ voltage across R_{o1}. Switching pattern is given in Table 4.2. For both outputs charging and discharging are performed individually so that equivalent resistance can be obtained for each of the outputs independently which is discussed in Section 4.3.1.

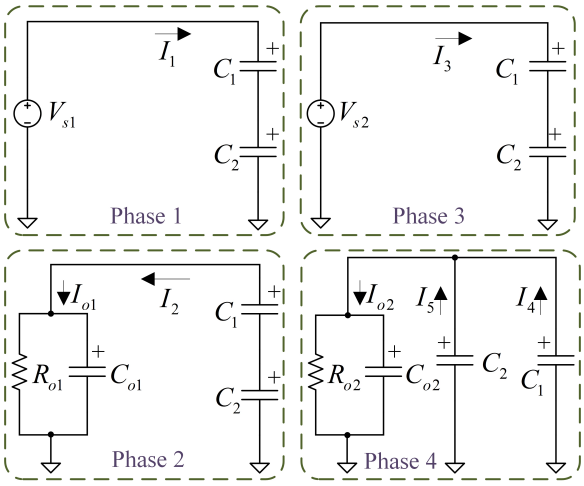


Figure 4.2: Different phases of proposed converter $V_{o1} = V_{s1}$ and $V_{o2} = 0.5 * V_{s2}$

Table 4.2: Pulse pattern of decoupled voltage ratio

Voltage ratio	ϕ	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
$V_{o1} = V_{s1}$ and $V_{o1} = 0.5 * V_{s2}$	ϕ_1	1	0	0	0	0	0	0	1	1	0	0
	ϕ_2	0	0	0	0	1	0	0	1	1	1	0
	ϕ_3	0	1	0	0	0	0	0	1	1	0	0
	ϕ_4	0	0	1	0	1	1	0	0	1	0	1

4.1.2 Operation of Coupled Case

Consider the voltage ratio ($V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ and $V_{o2} = 0.5 * V_{s1}$). To configure the given SCC voltage ratio, 4 phases ($\phi_1, \phi_2, \phi_3, \phi_4$) are required as shown in Figure 4.3. The switching pulse for the coupled case is shown in Table 4.3. For ϕ_1

Table 4.3: Pulse pattern of coupled voltage ratio

Voltage ratio	ϕ	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
	ϕ_1	1	0	0	0	0	0	0	1	1	0	0
$V_{o1} = 0.5 * V_{s1} + 0.5 * V_{s2}$	ϕ_2	0	0	1	0	1	1	0	0	1	1	0
$V_{o2} = 0.5 * V_{s1}$	ϕ_3	0	1	0	0	0	0	0	1	1	0	0
	ϕ_4	0	0	1	1	1	1	0	0	0	0	1

and ϕ_2, series charging and parallel discharging of flying capacitors are required which results in $V_{o2} = 0.5 * V_{s1}$. In ϕ_3 capacitors are charged again, capacitor voltage level

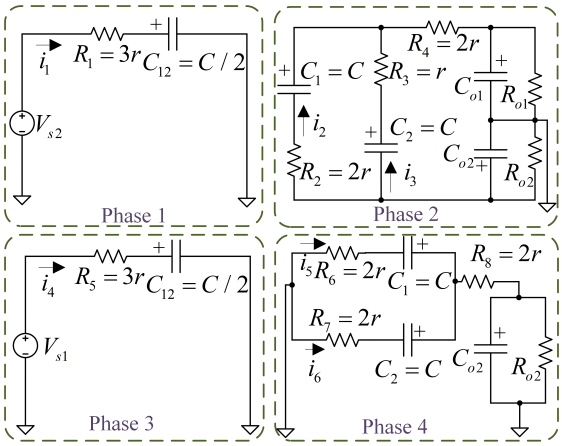


Figure 4.3: Different phases of proposed converter $V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ and $V_{s2} = 0.5 * V_{s1}$

becomes $(0.5 * V_{s2})$. Similarly for ϕ_4 newly charged parallelly connected capacitors get in to series with R_{o2} which has already gained the voltage level of $(0.5 * V_{s1})$. Hence the output voltage becomes $(0.5 * V_{s1}) + (0.5 * V_{s2})$ across R_{o1}.

4.2 Analysis and Modelling of DIDO SCC

Equivalent resistance (R_{eq}) of the circuit is another important parameter of DIDO SCC. Two possible cases are considered in terms of DIDO outputs, i.e., decoupled

output and cross coupled outputs. Dual output converters provide two outputs in which the output will be generated based on flying and output capacitors. If implementations of outputs are independent from each other, then two outputs can be assumed as *decoupled*. With reference to Figure 4.1, if there are changes in output 1 (V_{o1}), that affects the second output (V_{o2}) (Zhaikhan et al., 2016b) then it is said to be *cross coupling*. DIDO systems commonly face with the issue known as a cross coupling, i.e., coupled outputs. Such kind of phenomenon can be detected by simulations or by analysis of switching pattern. Two possible cases are discussed to solve the coupled problems with analysis and experimental setup. R_{eq} analysis of DIDO SCC can be solved using various procedures as discussed in the literature (Seeman, 2009, Seeman and Sanders, 2008, Abraham et al., 2017, Evzelman and Ben-Yaakov, 2013, Ben-Yaakov and Evzelman, 2009). In this thesis, two solutions are considered. 1) Charge balance and nodal KCL analysis. 2) Accurate calculation using partial KVL. The details of the discussion are as follows in the upcoming Sections.

4.3 Charge Balance and Nodal KCL Analysis

Decoupled output can be analysed separately using the following output analysis (Evzelman and Ben-Yaakov, 2013, Ben-Yaakov, 2012) by considering two[2] different voltage ratios.

4.3.1 Decoupled Case

The design proposed in this work claims general advantages of dual output system. DIDO SCC can also resolve voltage ratios which are impossible[3] with single output. Following the procedure described in (Evzelman and Ben-Yaakov, 2013) charge balance and nodal KCL analysis for ϕ_1 and ϕ_2 yields the following system of equations:

$$I_1 - I_2 = 0; \tag{4.1}$$

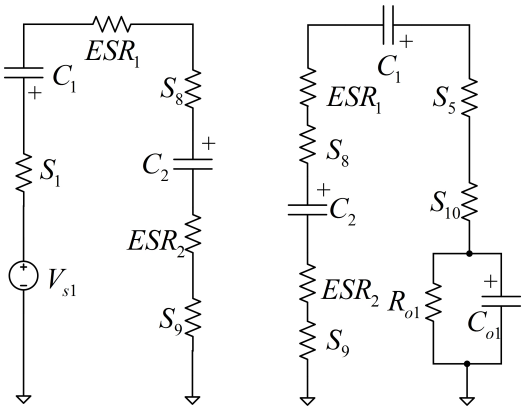
$$I_1 = I_0; \tag{4.2}$$

$$I_1 = I_2 = I_0. \tag{4.3}$$

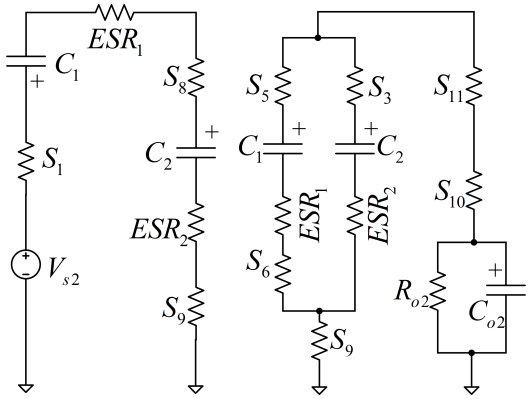
[2]Two voltage ratios are selected using Table 4.1 for simplicity and brief understanding only two voltage ratios are chosen.

[3]Circuit can be reconfigured for $V_{s1} + (0.5 * V_{s2})$ (Abraham et al., 2017) or $V_{s2} + (0.5 * V_{s2})$ (Abraham et al., 2017), but not $(0.5 * V_{s1}) + (0.5 * V_{s2})$.

Using the (4.1) - (4.3) equivalent resistance 1 (R_{eq1}) (Ben-Yaakov, 2012, Zhaikhan et al., 2016b, Pumps, 2014) is given by:



(a) Equivalent resistance of charging state and discharging state of V_{o1}



(b) Equivalent resistance of charging and discharging state of V_{o2}

Figure 4.4: Equivalent resistance of state $V_{o1} = V_{s1}$ and $V_{o1} = 0.5 * V_{s2}$

$$R_{eq1} = \frac{1}{2f_s * C_{eq1}} \coth\left(\frac{1}{8f_s * C_{eq1} * r_{eq1}}\right) + \frac{1}{2f_s * C_{eq2}} \coth\left(\frac{1}{8f_s * C_{eq2} * r_{eq2}}\right). \tag{4.4}$$

Using Figure 4.4(a) R_{eq1} is derived and the simplified form is given in (4.4) and the parameters of (4.4) are given in (4.5), where ESR is equivalent series resistance of capacitors.

$$r_{eq1} = 3 * r_{on} + 2ESR; \tag{4.5}$$

$$r_{eq2} = 4 * ron + 2ESR; \tag{4.6}$$

$$C_{eq1} = \frac{C}{2} = C_{eq2}. \tag{4.7}$$

Similarly for R_{eq2}, the equations are given by,

$$R_{eq2} = \frac{1}{8f_s * C_{eq1}} \coth\left(\frac{1}{8f_{c1} * C_{eq1} * r_{eq1}}\right) + \frac{1}{2f_s * C_{eq2}} \coth\left(\frac{1}{8f_s * C_{eq2} * r_{eq2}}\right). \tag{4.8}$$

Using Figure 4.4(b), R_{eq2} is derived and the simplified form is given in (4.8). The parameters of (4.8) are given in (4.9).

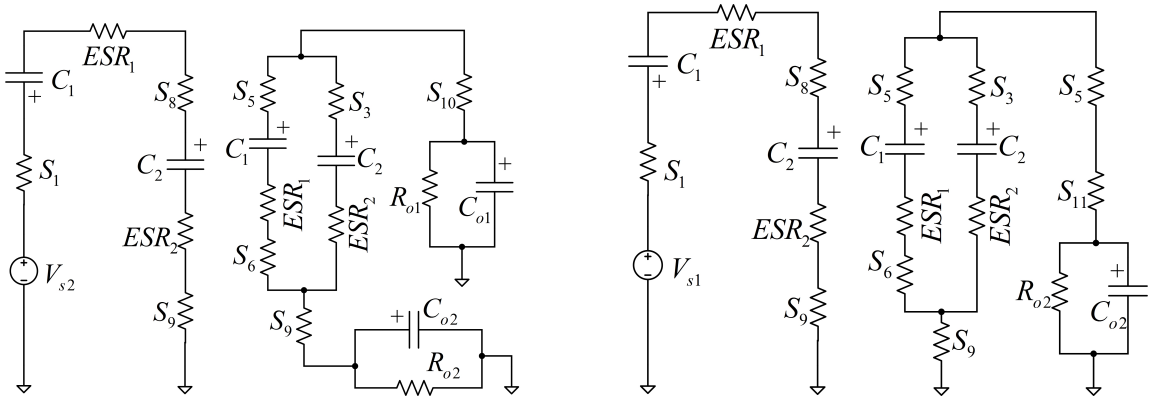
$$r_{eq1} = 3 * r_{on} + 2ESR; \tag{4.9}$$

$$r_{eq2} = \frac{8}{3} r_{on} + \frac{ESR}{2}; \tag{4.10}$$

$$C_{eq1} = \frac{C}{2}; \tag{4.11}$$

$$C_{eq1} = 2C. \tag{4.12}$$

From Figure 4.1 assume, all the switches on resistance, r_{on} are identical, capacitance and parasitic effects (ESR) are the same for both flying capacitors, and filter capacitance (C_{o1} and C_{o2}) is large compared to flying capacitance (C_1 and C_2) value. The equivalent resistance of the proposed converter output is given in (4.4) and (4.8). For all other voltage ratios given in Table 4.1 similar steps are followed to find the R_{o1} and R_{o2} of the proposed SCC assuming no coupling effects.



(a) R_{eq} of charging state and discharging state of V_{o1}

(b) R_{eq} of charging and discharging state of V_{o2}

Figure 4.5: Equivalent resistance of state $V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ and $V_{o1} = 0.5 * V_{s1}$

4.3.2 Coupled Case

Implementation of coupled voltage ratio requires two outputs being in the same phase as shown in Figure 4.5. Referring to Figure 4.5(a), coupled operation clearly point that the output voltage V_{o1} and V_{o2} are used in the same operations which makes it difficult to avoid cross coupling phenomenon. Modeling of the circuit based on two

separate equivalent resistances may result in highly inaccurate results. Modelling and equivalent resistance of coupled dual output systems is the major area of DIDO SCC. The detailed coupled outputs are discussed in Chapter 5. In this Chapter, verification of coupled voltage ratios are limited to simulations.

4.3.3 Simulation Results and Discussion

Simulation and modelling parameters of the proposed converter is discussed in this Section. To verify the design, PSIM simulation tool was used. Real time parameters were considered for simulation and modeling the converter. The details are as follows: MAX4678 CMOS analog bidirectional switch parameters are used for switches $S_1 - S_{11}$ referring to the Figure 4.1 with $r_{on} = 0.4\ \Omega$, flying capacitor is 22 μF with ESR of 100 mΩ, output capacitor is 220 μF and the load resistance of 200 Ω. The load current ranges from 25 mA to 100 mA at voltage range of 5 V – 10 V. **Decoupled:**

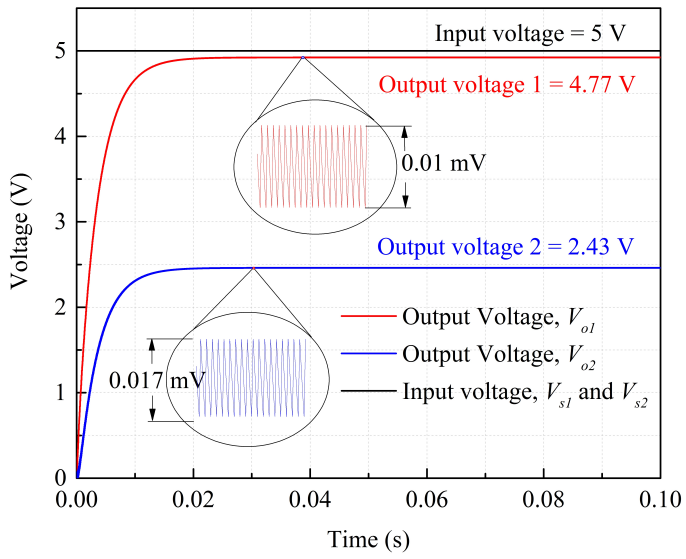


Figure 4.6: Simulation result voltage ratio of $V_{o1} = V_{s1}$ and $V_{o2} = 0.5 * V_{s2}$

Figure 4.6 illustrates the output voltages and voltage ripples of voltage ratio ($V_{o1} = V_{s1}$ and $V_{o2} = 0.5 * V_{s2}$). **Coupled:** Similarly Figure 4.7 illustrates the output voltages and voltage ripples of the proposed voltage ratio ($V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ and $V_{o2} = 0.5 * V_{s1}$). Switching Frequency (f_s) is varied accordingly to verify the proposed converter efficiency. For modelling the converter, equivalent resistance needs to be calculated and it is verified by applying different frequencies that are discussed in

Table 4.4: Modelled and simulated value comparison of V_{o1} and V_{o2}

Frequency	V_{o1}, $I_{o1} = 25$ mA		V_{o2}, $I_{o2} = 12.5$ mA		η [%]		η [%]	
kHz	Model [V]	Simulated [V]	Model [V]	Simulated [V]	Model	Simulated	Model	Simulated
100	4.68	4.77	2.43	2.41	93.6	95.4	97.2	96.4
50	4.68	4.77	2.43	2.41	93.6	95.4	97.2	96.4
25	4.68	4.75	2.43	2.41	93.6	95.0	97.2	96.4

Table 4.5: Different voltage ratios simulated output

voltage ratios	V_{s1}	V_{s2}	V_{o1}	V_{o2}
$V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ $V_{o2} = 0.5 * V_{s1}$	4	6	4.985	1.991
$V_{o1} = (0.5 * V_{s1}) + (V_{s2})$ $V_{o2} = V_{s2}$	6	4	6.999	2.999
$V_{o1} = 2 * V_{s2}$ $V_{o2} = 1.5 * V_{s2}$	4	-	7.997	5.997

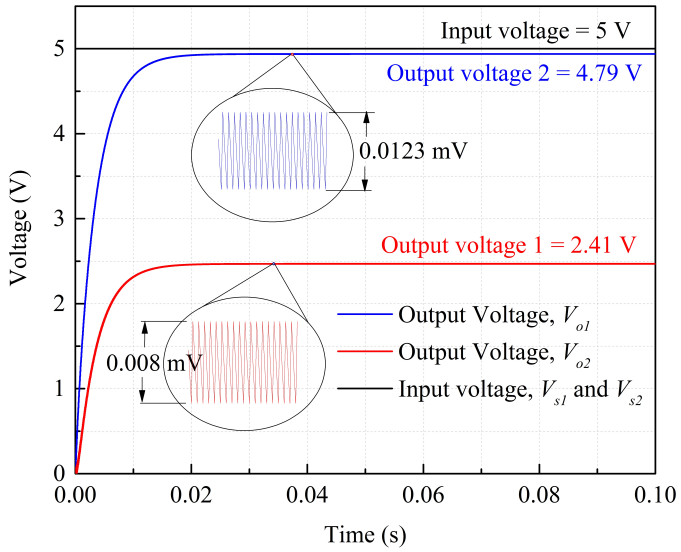


Figure 4.7: Simulation result voltage ratio of $V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2}$ and $V_{o2} = 0.5 * V_{s1}$

Table 4.4. From Table 4.4 it is clear that modelled and simulated results are in good agreement to verify the proposed converter topology. In addition, the results are verified for different voltage ratio states as presented in Table 4.5.

4.4 Two Port System

Single output modelling methods are preferred for decoupled case, such as phase average-current methodology (Evzelman and Ben-Yaakov, 2013), (Seeman, 2009), can be applied separately for each of outputs. The modeling includes losses of capacitor and on switch resistance. Average current methodology (Evzelman and Ben-Yaakov, 2013), (Ben-Yaakov, 2012) was quite accurate for predicting the behavior of dual output decoupled SCC described in (Zhaikhan et al., 2017). On the other hand, for **coupled case** a new methodology is implemented for solving the equivalent resistance. Approach in (Zhaikhan et al., 2016a) proposes to treat dual output ternary SCC as a two-port system (Mustafa et al., 2018a) shown in Figure 4.8(a) and Figure 4.8(b). According to the two-port system analysis, output voltages for load resistances R_1 and R_2 are described as in (4.13), (4.14).

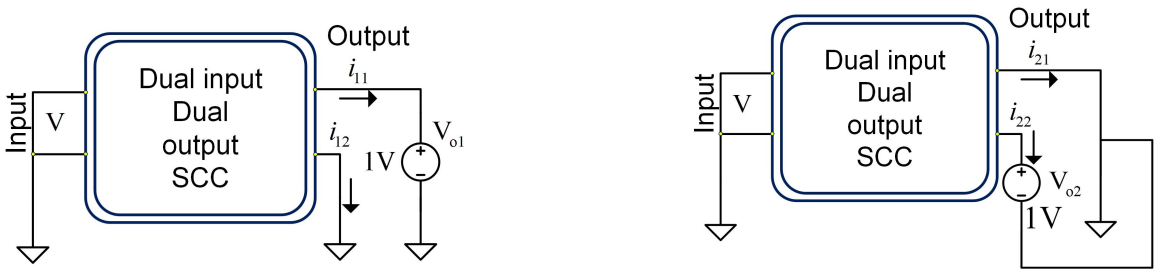
$$\mathrm{V_{o1}} = V_1 - I_{L1}R_{11} - I_{L2}R_{12}; \tag{4.13}$$

$$\mathrm{V_{o2}} = V_2 - I_{L1}R_{21} - I_{L2}R_{22}, \tag{4.14}$$

where load currents I_{L1} and I_{L2} can be written as:

$$I_{L1} = \frac{V_{01}}{R_1}; \qquad I_{L2} = \frac{V_{02}}{R_2}. \tag{4.15}$$

In (4.13), (4.14), V_{o1}, V_{o2} are actual output voltages, while V_1 and V_2 are targeted



(a) Output 1 (b) Output 2

Figure 4.8: General two-port system.

output voltages. Therefore, the dual output SCC model (4.16) and (4.17) becomes a function of resistance and transresistance parameters, which constitute for R_{eq} (R-parameters) of the converter. R_{11} and R_{22} account for normal equivalent resistances, while R_{12} and R_{21} are for coupling resistances (transresistances).

$$V_{01} = \frac{V_{TR1}R_1(R_2 + R_{22}) - V_{TR2}R_1R_{12}}{(R_{11} + R1)(R_{22} + R_2) - R_{12}R_{21}}; \tag{4.16}$$

$$V_{02} = \frac{V_{TR2}R_2(R_1 + R_{11}) - V_{TR1}R_2R_{21}}{(R_{11} + R1)(R_{22} + R_2) - R_{12}R_{21}}. \tag{4.17}$$

To find unknown R-parameters, four steps are to be considered using the concept of general two-port system.

1. Short-circuit all input voltage sources.

2. Connect 1 V voltage source (V) to the first output and short-circuit the second one as shown in Figure 4.8(a).

3. At this state, find the average load currents I_{11} and I_{21}.

4. Repeat steps 1 and 2 for finding I_{12} and I_{22}. However, in this case, short-circuit the first output and replace the second load with 1 V voltage source as shown in Figure 4.8(b).

Above four steps yield I-matrix of the two-port system. Since $Y = I/\mathrm{V}$ and $\mathrm{V} = 1$ V, I-matrix will simply be equal to Y-matrix. Inverse of Y-matrix will finally bring to R-matrix (R-parameters).

4.5 Accurate R_{eq} Calculation of DIDO SCC

Accurate equivalent resistance analysis is discussed separately for the two cases. Configuration is called decoupled if parameters R_{12} and R_{21}, called "transresistances" are relatively small. With decoupled loads dual output SCC can be treated as two separate single output SCCs. For coupled case, on the contrary, outputs cross regulation becomes more apparent. Implementation of voltage ratios $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$ is predetermined as decoupled, since two outputs never appear together in one topology, as shown in Figure 4.9. For both cases, accurate equivalent resistance analysis is solved using two-port system approach explained in Section 4.4. Coupled case is discussed briefly in Chapter 5 and decoupled case is discussed in the upcoming Sections 4.5.1.

4.5.1 Decoupled Case

In this accurate methodology, for deriving R_{eq} a few steps are to be assumed as follows:

1. Equal switch resistance (r), equal capacitance of flying capacitor (C), (ESR) of flying capacitor .

2. Filter (load) capacitors effect is neglected.

Using Table 4.6 and above assumptions, (4.18)-(4.21) were derived using different phases that are shown in Figure. 4.9. Time constants for different Phases (Phase 1 – T_1; Phase 2 – T_2, T_3; Phase 3 – T_4, T_5; Phase 4 – T_6) are found using Figure. 4.9 and are given in (4.22)-(4.25). Due to the symmetry of Phase 2 and Phase 3, the

Table 4.6: Pulse pattern of decoupled voltage ratio

voltage ratio	Phase	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
$V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$	Phase 1	1	0	0	1	0	0	0	1	0	0	0
	Phase 2	0	0	1	0	1	1	0	0	1	1	0
	Phase 3	0	1	1	0	1	1	1	0	0	0	0
	Phase 4	0	0	0	0	1	0	0	1	1	0	1

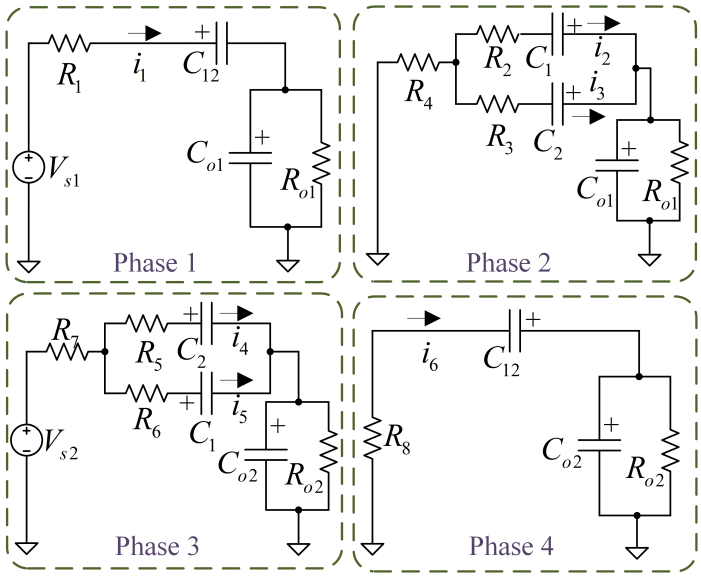


Figure 4.9: Different phases of proposed converter $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$.

corresponding time constants are similar to each other.

$$R_1 = 3r + 2ESR; \quad R_2 = 2r + ESR; \quad R_3 = r + ESR; \tag{4.18}$$

$$R_4 = 2r; \quad R_5 = 2r + ESR; \quad R_6 = r + ESR; \tag{4.19}$$

$$R_7 = 2r; \quad R_8 = 4r + 2ESR; \tag{4.20}$$

$$C_1 = C; \quad C_2 = C; \quad C_{12} = C/2. \tag{4.21}$$

$$T_1 = \frac{C(2ESR + 3r)}{2}; \tag{4.22}$$

$$T_2 = T_4 = \frac{2C(ESR^2 + 7ESRr + 8r^2)}{2ESR + 7r + (\sqrt{17})r}; \tag{4.23}$$

$$T_3 = T_5 = \frac{2C(ESR^2 + 7ESRr + 8r^2)}{2ESR + 7r - (\sqrt{17})r}; \tag{4.24}$$

$$T_6 = C(ESR + 2r). \tag{4.25}$$

4.5.1.1 Input Voltages and Output 2 are Short-Circuited

Voltage source (V) is applied at output 1 (input voltages and output 2 are short-circuited) as shown in Figure. 4.8(a). The capacitor voltage expressions for each phase as discussed in Figure. 4.9 are given in (4.26)-(4.31),

$$V_{1C12}(t) = -V + (V_{1C12}(0) + V)e^{(-t/T_1)}; \tag{4.26}$$

$$V_{2C1}(t) = V + a_{11}e^{(-t/T_2)} + a_{12}e^{(-t/T_3)}; \tag{4.27}$$

$$V_{2C2}(t) = V + a_{21}e^{(-t/T_2)} + a_{22}e^{(-t/T_3)}; \tag{4.28}$$

$$V_{3C1}(t) = a_{31}e^{(-t/T_4)} + a_{32}e^{(-t/T_5)}; \tag{4.29}$$

$$V_{3C2}(t) = a_{41}e^{(-t/T_4)} + a_{42}e^{(-t/T_5)}; \tag{4.30}$$

$$V_{4C12}(t) = V_{4C12}(0)e^{(-t/T_6)}. \tag{4.31}$$

To find unknown coefficients, a set of 10 linear equations need to be derived. Among those five equations are from capacitor voltage continuity principle which are given in (4.32)-(4.35) where T is a switching period.

$$V_{1C12}(T/4) = V_{2C1}(0) + V_{2C2}(0); \tag{4.32}$$

$$V_2C1(T/4) = V_3C1(0); \quad V_{2C2}(T/4) = V_{3C2}(0); \tag{4.33}$$

$$V_{3C1}(T/4) + V_{3C2}(T/4) = V_{4C12}(0); \tag{4.34}$$

$$V_{4C12}(T/4) = V_{1C12}(0), \tag{4.35}$$

The other two equations from partial KVL (only exponential terms) of Phase 2 are given in (4.36)-(4.38)

$$i_2(t)R_2 - V_{2C1}(t) = i_3(t)R_3 - V_{2C2}(t); \tag{4.36}$$

$$\left(\frac{R_2C_1}{T_2} - 1\right)a_{11} = \left(\frac{R_3C_2}{T_2} - 1\right)a_{21}; \tag{4.37}$$

$$\left(\frac{R_2C_1}{T_3} - 1\right)a_{12} = \left(\frac{R_3C_2}{T_3} - 1\right)a_{22}. \tag{4.38}$$

The other two equations from partial KVL (only exponential terms) of Phase 3 are given in (4.39)-(4.41)

$$i_4(t)R_2 - V_{3C2}(t) = i_3(t)R_6 - V_{3C1}(t); \tag{4.39}$$

$$\left(1 - \frac{R_5C_1}{T_4}\right) a_{41} = \left(1 - \frac{R_6C_1}{T_4}\right) a_{31}; \tag{4.40}$$

$$\left(1 - \frac{R_5C_1}{T_5}\right) a_{42} = \left(1 - \frac{R_6C_1}{T_5}\right) a_{32}. \tag{4.41}$$

Further one equation from charge conservation between two capacitor plates C_1 and C_2 during Phase 1 and Phase 4 is given in (4.42).

$$C_2V_{3C2}(T/4) - C_1V_{3C1}(T/4) = C_2V_{2C2}(0) - C_1V_{2C1}(0). \tag{4.42}$$

Average currents from the loads (I_{11} and I_{21}) are given by,

$$I_{11} = -\frac{1}{T}\left(\int_0^{(T/4)} i_1(t)dt + \int_0^{(T/4)} (i_2(t) + i_3(t))dt\right); \tag{4.43}$$

$$I_{21} = -\frac{1}{T}\left(\int_0^{(T/4)} i_6(t)dt + \int_0^{(T/4)} (i_4(t) + i_5(t))dt\right). \tag{4.44}$$

Y-parameters (Y_{11} and Y_{21}) are calculated as

$$Y_{11} = \frac{I_{11}}{V}; \quad Y_{21} = \frac{I_{21}}{V}. \tag{4.45}$$

4.5.1.2 Input Voltages and Output 1 are Short-Circuited

Voltage source (V) is applied at the output 2 (input voltages and output 1 are short-circuited) as shown in Figure. 4.8(b). The capacitor voltage expressions for each phase are given in (4.46)–(4.51)

$$V_{1C12}(t) = (V_{1C12}(0) + V)e^{(-t/T_1)}; \tag{4.46}$$

$$V_{2C1}(t) = a_{11}e^{(-t/T_2)} + a_{12}e^{(-t/T_3)}; \tag{4.47}$$

$$V_{2C2}(t) = a_{21}e^{(-t/T_2)} + a_{22}e^{(-t/T_3)}; \tag{4.48}$$

$$V_{3C1}(t) = -V + a_{31}e^{(-t/T_4)} + a_{32}e^{(-t/T_5)}; \tag{4.49}$$

$$V_{3C2}(t) = -V + a_{41}e^{(-t/T_4)} + a_{42}e^{(-t/T_5)}; \tag{4.50}$$

$$V_{4C12}(t) = V + (V_{4C12}(0) - V)e^{(-t/T_6)}. \tag{4.51}$$

Similar steps are followed for solving the set of 10 linear equations as discussed in previous equations (4.18) - (4.44). The derivation of average currents from the loads I_{12} is similar to I_{11}, while I_{22} is similar to I_{21}. Y-parameters (Y_{12} and Y_{22}) are calculated as given in (4.52).

$$Y_{12} = \frac{I_{12}}{V}; \quad Y_{22} = \frac{I_{22}}{V}. \tag{4.52}$$

R-parameters are reciprocal to Y-parameters and is given by,

$$\begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix}^{-1}. \tag{4.53}$$

The final expression of R-parameters is discussed[4] in APPENDIX C.1.

4.5.2 Simulation, Experimental Results and Discussion

The detailed simulation, experimental results are discussed in this Section where real time parameters are considered as discussed in Section 4.3.3. In Section 4.3.1 voltage ratio $V_{o1} = V_{s1}$ and $V_{o2} = (0.5 * V_{s1})$ is considered and it is solved using approximate analysis. For **decoupled case:** accurate R_{eq} analysis is considered, and for better understanding and simplicity decoupled analysis is performed for $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$ voltage ratio and solved mathematically and it is validated by simulation and the modelling results as shown in Table 4.7. To verify the design, PSIM simulation tool was used. Figure. 4.10(a) illustrates the output voltages of V_{o1} and V_{o2} VCR ($V_{o1} = \frac{1}{3}V_{s1}$) and ($V_{o2} = \frac{2}{3}V_{s2}$) and voltage ripples are plotted for 25 kHz frequency. Similarly Figure 4.10(b) illustrates the output voltages and voltage ripples of voltage ratio ($V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$) of 100 kHz frequency. Table 4.8 shows the compared results of model, the simulated and experimental results are in good agreement to verify the decoupled voltage ratios. Finally, comparison of decoupled

[4]The calculations were made symbolically in MATLAB software.

Table 4.7: Modelling, analysis comparison of voltage ratios

Decoupled case: $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$								
f, kHz	**Modelling**				**Simulation**			
	$R_{11}(\Omega)$	$R_{21}(\Omega)$	$R_{12}(\Omega)$	$R_{22}(\Omega)$	$R_{11}(\Omega)$	$R_{21}(\Omega)$	$R_{12}(\Omega)$	$R_{22}(\Omega)$
10	2.50	-0.18	-0.32	2.61	2.49	-0.16	-0.29	2.60
50	2.01	0.02	-0.05	2.17	2.01	0.02	-0.05	2.17
100	1.99	0.01	-0.03	2.15	1.99	0.01	-0.03	2.15

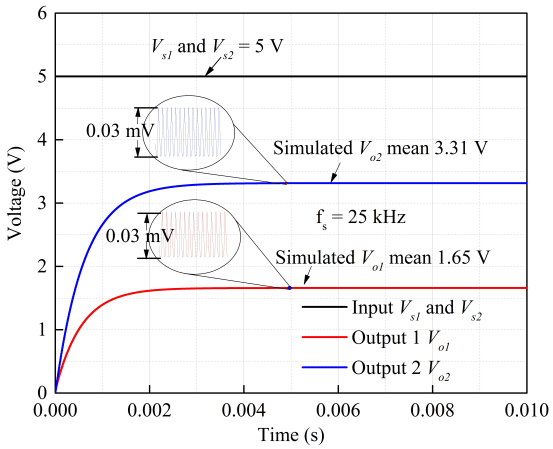
Table 4.8: Modelled, simulated and experimental comparison of voltage ratios [a]

Voltage ratios	Frequency [kHz]	V_{o1}			V_{o2}		
		Model [V]	Simulated [V]	Hardware [V]	Model [V]	Simulated [V]	Hardware [V]
Decoupled	50	1.66	1.66	1.57	3.32	3.32	2.98
	100	1.66	1.66	1.6	3.32	3.32	3.01

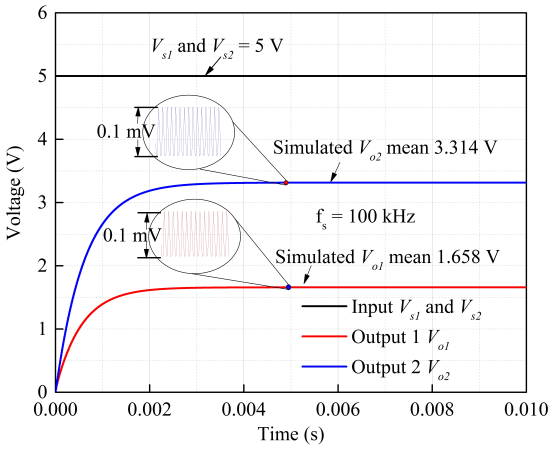
Table 4.9: Fig. 4.11 comparison table for different voltage ratios

VCRs	State 1	State 2	Actual V_{o1} [V]	Simulated V_{o1} [V]	Actual V_{o2} [V]	Simulated V_{o2} [V]
$V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{1}{3}V_{s2}$	1	1	1.66	1.65	1.66	1.65
$V_{o1} = \frac{1}{3}V_{s2}$ and $V_{o2} = \frac{1}{3}V_{s1}$	2	2	1.66	1.65	1.66	1.66
$V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$	1	4	1.66	1.65	3.33	3.30
$V_{o1} = \frac{1}{3}V_{s2}$ and $V_{o2} = \frac{2}{3}V_{s1}$	2	5	1.66	1.65	3.33	3.32
$V_{o1} = \frac{2}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$	3	4	3.33	3.32	3.33	3.30
$V_{o1} = \frac{2}{3}V_{s2}$ and $V_{o2} = \frac{2}{3}V_{s1}$	4	5	3.33	3.31	3.33	3.32
$V_{o1} = V_{s1}$ and $V_{o2} = \frac{1}{2}V_{s2}$	5	3	5.00	4.96	2.50	2.44
$V_{o1} = V_{s2}$ and $V_{o2} = \frac{1}{2}V_{s1}$	6	3	5.00	4.97	2.50	2.44
$V_{o1} = V_{s1}$ and $V_{o2} = \frac{1}{3}V_{s2}$	5	1	5.00	4.96	1.66	1.65
$V_{o1} = V_{s2}$ and $V_{o2} = \frac{1}{3}V_{s1}$	6	2	5.00	4.97	1.66	1.66
$V_{o1} = V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$	5	5	5.00	4.96	3.33	3.32
$V_{o1} = V_{s2}$ and $V_{o2} = \frac{2}{3}V_{s1}$	6	6	5.00	4.97	3.33	3.33

[a] All the values in the table are rounded to nearest points

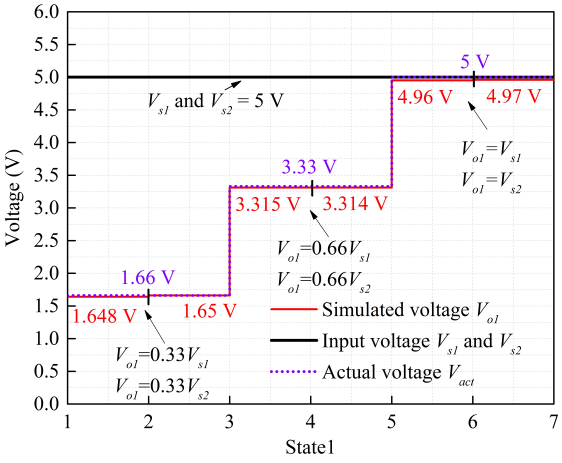


(a) Output voltage, input voltage and voltage ripple of V_{o1} and V_{o2} of f_s= 25 kHz

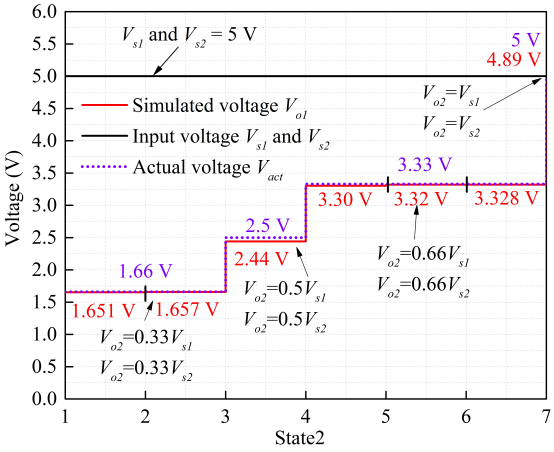


(b) Output voltage, input voltage and voltage ripple of V_{o1} and V_{o2} of f_s= 100 kHz

Figure 4.10: Simulation results of $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$.



(a) Output voltage V_{o1} voltage ratios

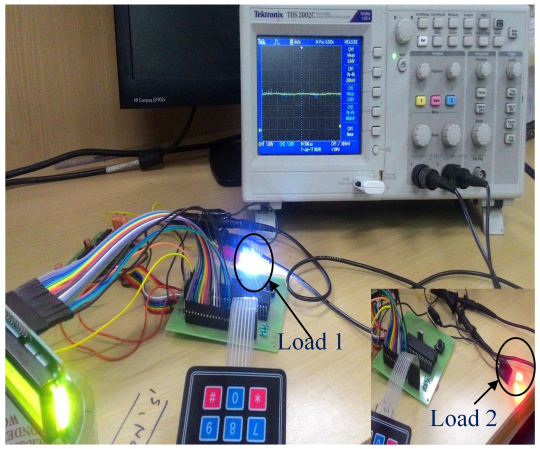


(b) Output voltage V_{o2} voltage ratios

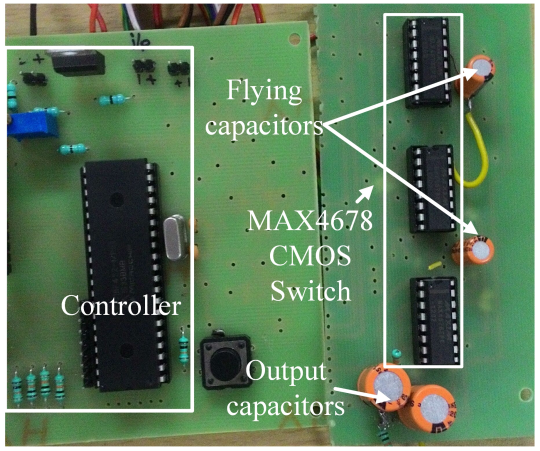
Figure 4.11: Comparison of simulated and actual output voltages of different votlage ratios.

voltage ratios are discussed using Figure. 4.11 and Table 4.9. Figure 4.12(a) and Figure 4.12(b) show the proposed SCC prototype[5]. Figure 4.12(c) - Figure 4.12(f) show the output voltage of V_{o1} and V_{o2} for voltage ratios of ($V_{o1} = \frac{1}{3}V_{s1}$) and ($V_{o2} = \frac{2}{3}V_{s2}$) and ($V_{o1} = \frac{2}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$) for different load current of 10 mA and 100 mA. Switching Frequency (f_s) is varied accordingly to verify the proposed converter

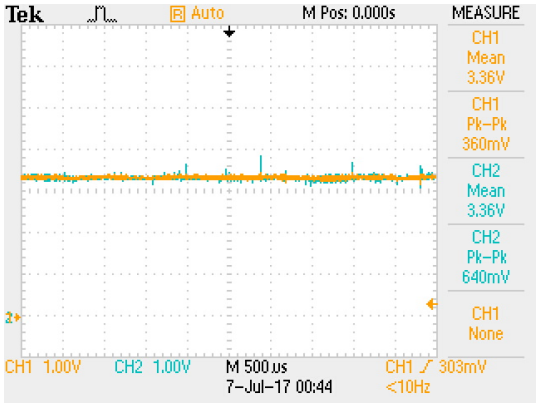
[5]The proteous model is shown in Figure C.1 and PCB circuit is shown in Figure C.2



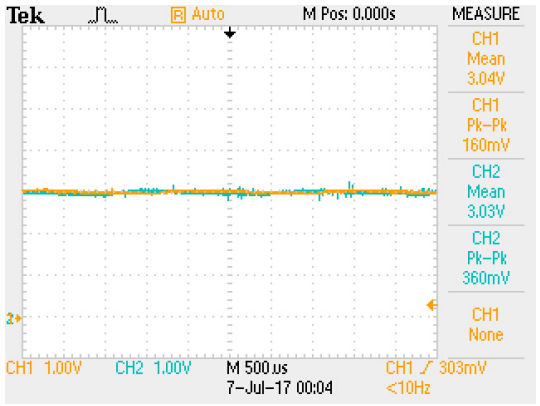
(a) Protoype of Dual input and Dual output SCC with different load condition



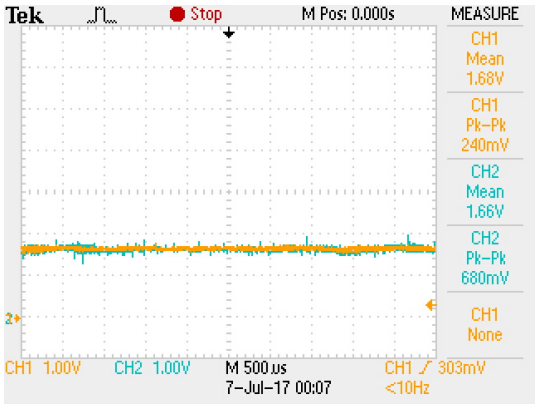
(b) Protoype of Dual input and Dual output SCC



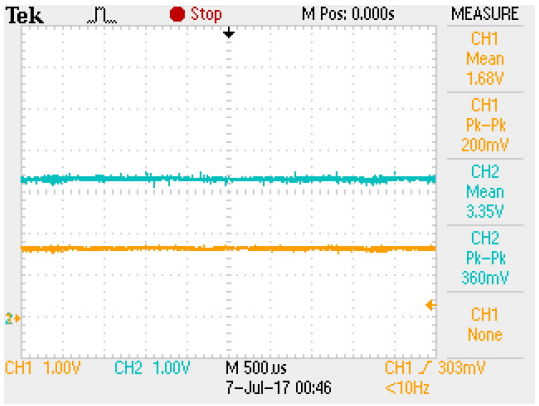
(c) Output Voltage of V_{o1} and V_{o2}



(d) Output Voltage of V_{o2} and V_{o1}



(e) Output Voltage of V_{o1} and V_{o2}



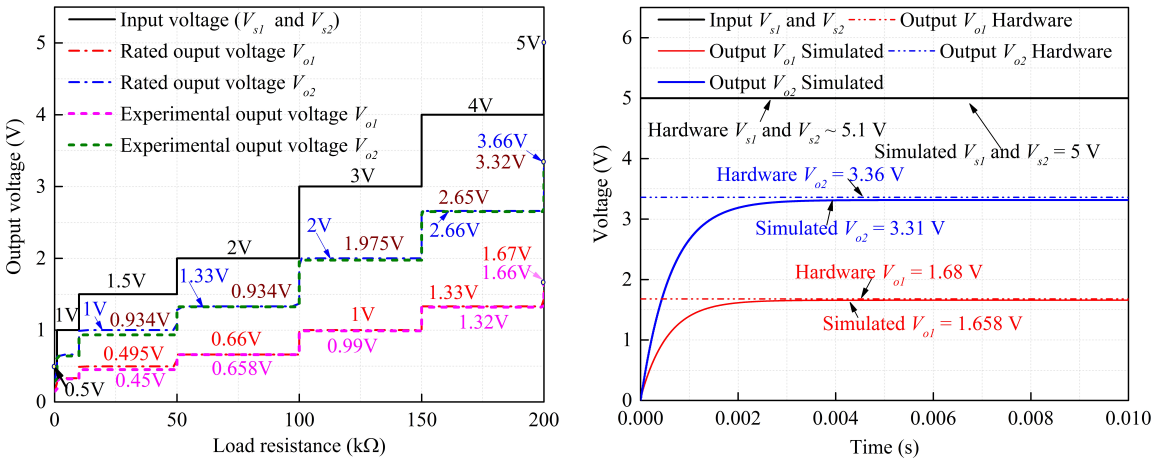
(f) Output Voltage of V_{o1} and V_{o2}

Figure 4.12: Experimental results[a] for different voltage ratios for 10 mA and 100 mA. (c) $V_{o1} = \frac{2}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$ for 10 mA (d) $V_{o1} = \frac{2}{3}V_{s1}$ and $V_{o2} = \frac{1}{3}V_{s2}$ for 100 mA (e) $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{1}{3}V_{s2}$ for 100 mA (f) $V_{o1} = \frac{1}{3}V_{s1}$ and $V_{o2} = \frac{2}{3}V_{s2}$[b] for 10 mA.

[a]This experimental setup shown here is for validating the prototype model of DIDO converter using hardware components. With the help of this model we can easily design a PMIC.

[b]For hardware setup input (V_{s1} and V_{s2}) are treated as ≅5.1 V.

efficiency. Figure. 4.13(a) shows various load conditions of DIDO SCC. Figure. 4.13(b) shows good agreement for hardware and simulation output.



(a) Simulation result of different load condition with different frequency

(b) Comparison of experimental and simulation results of load 10 mA voltage ratio

Figure 4.13: Experimental and Simulation results of voltage ratios ($V_{o1} = \frac{1}{3}V_{s1}$) and ($V_{o2} = \frac{2}{3}V_{s2}$) DIDO SCC

4.6 Coupled Case

In Section 4.3.2, the voltage ratios of $V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ and $V_{o2} = 0.5 * V_{s1}$ are considered. According to (Zhaikhan et al., 2017) coupled case voltage ratio R_{eq} analysis is difficult to solve using general KCL and KVL analysis (Seeman, 2009, Seeman and Sanders, 2008, Abraham et al., 2017, Evzelman and Ben-Yaakov, 2013, Ben-Yaakov and Evzelman, 2009). To overcome the issue, detailed algorithm is developed with the help of the two port system using R-parameter methodology which is discussed in Section 4.4. The key point to be considered for developing the algorithm is, R-parameters where it includes all conduction and ohmic losses accounting for coupling effects. To validate the performance of designed coupled SCC, modeling and mathematical analysis has been carried out. Coupled case of DIDO SCC is discussed briefly in the upcoming Chapter 5.

4.7 Conclusion

DIDO SCC is analysed and modelled for all decoupled/coupled voltage ratios by using equivalent resistance and verified by applying the same values in simulation. The simulation values and modelling values are in good agreement for DIDO design and it is compared with previous SCC which is discussed in Table 4.10. Moreover, analysis of coupling effects are studied and it is discussed in the next upcoming Chapter.

Table 4.10: Comparison of previous SCC topologies

Authors	Number of switches	No of input	No of output	No of capacitors	VCRs	Specification
A*	15	1	1	5	2	1 V, <250 mA
B*	4	2	1	2	1	36 V, <120 mA
C*	7	1	1	3	2	5.4 V, <120 mA
D*	14(include diodes)	2	1	3	11	9 V, <120 mA
This work	11	2	2	3	32	10 V, <100 mA

A* = Le et al. (2011).

B* = Yuanmao and Cheng (2012), Yuan-mao and Cheng (2013).

C* = Pumps (2014).

D* = Abraham et al. (2017).

Chapter 5

ANALYSIS OF COUPLED CASE R_{eq} OF DIDO SCC

In Chapter 4, DIDO SCC topology was discussed and R_{eq} analysis was performed for both cross coupled and decoupled cases. Charge balance methodology was used for solving the decoupled case and the coupled case. Due to coupling effects charge balance method went inaccurate. To overcome the issue, two-port system was introduced in Chapter 4 for decoupled case. In this Chapter using two port system, accurate R_{eq} analysis is derived for cross-coupling cases. This is one of the major issues of dual output converter but using two-port system the issues are solved for all the coupled voltage ratios. For low power and low current converters coupling effect will be too small hence it is negligible. If current exceeds 100 mA, coupling effect may be present in the converter. In this chapter, coupling effects are included and derived analytically. Equivalent model R-parameters are calculated analytically and validated by simulation and experiment.

Parts of this chapter were previously presented at the TENCON 2018, in Jeju island, Korea (Zhaikhan et al., 2018) and published in the IET Circuits, Devices & Systems, in December 2018 (Subburaj et al., 2018b).

5.1 Voltage Source Method of R-parameters Calculation

It should be noted that this method neglects the effect of filter (load) capacitors. As a result, theoretical calculations are less complex. For simulation and experimental measurements of R-parameters, it is suggested to use current sources and to measure average output voltages to account for filter capacitors effects. R_{eq} analysis for coupled case two voltage ratios are considered and explained in detail for easy understanding. The voltage ratios V_{o1} =$(0.5 * V_{s1})$+$(0.5 * V_{s2})$, $V_{o2} = (0.5 * V_{s1})$ and the $V_{o1} = (2{*}V_{s1})+(2{*}V_{s2})$ and $V_{o2} = (2{*}V_{s1})$ are considered. (R_{eq}) is solved using R-parameters analysis and the detailed explanation is discussed in the upcoming Section 5.3.

5.2 Circuit Description of DIDO

The DIDO SCC configuration was discussed in Chapter 4 and it is illustrated in Figure 4.1. It is basically a two capacitor series-parallel SCC, modified with DIDO converter. All DIDO SCC voltage ratios which include coupled and decoupled ratios were listed in Chapter 4 referring to Table 4.1. Sample coupled voltage ratios are

Table 5.1: Coupled voltage ratio

Voltage ratios
$V_{o1} = V_{s2}$ and $V_{o2} = (0.5 * V_{in1}) + V_{s2}$
$V_{o1} = (2 * V_{in1})$ and $V_{o2} = (1.5 * V_{in1})$
$V_{o2} = (2 * V_{s2})$ and $V_{o1} = (2 * V_{in1}) + (2 * V_{s2})$
$V_{o1} = (2 * V_{s2})$ and $V_{o2} = V_{s2}$
$V_{o2} = V_{s2}$ and $V_{o1} = (0.5 * V_{in1}) + V_{s2}$
$V_{o1} = (0.5 * V_{in1}) + (0.5 * V_{s2})$ and $V_{o2} = 0.5 * V_{in}$
$V_{o2} = (2 * V_{in1})$ and $V_{o1} = (1.5 * V_{in1})$
$V_{o1} = (2 * V_{s2})$ and $V_{o2} = (2 * V_{in1}) + (2 * V_{s2})$
$V_{o2} = (2 * V_{s2})$ and $V_{o1} = V_{s2}$

shown in Table 5.1. Main principle of operation based on two phase (parallel or series) charging and discharging of flying capacitors has already been discussed in Chapter 4. In dual output, the number of phases is doubled so that each of the output voltage ratio implementation is characterized with separate charging and discharging states.

Separate implementation of each output voltage ratio reduces the possibility of cross coupling effects (Zhaikhan et al., 2016a).

5.3 Steps to be Followed for Solving Coupled Case

The R-parameters are derived using the following analytical process, i.e., RC network and partial KVL methods. For simplicity, two voltage ratios are considered for the upcoming R-parameters analysis, i.e., a) $V_{o1} = (0.5{*}V_{s1}){+}(0.5{*}V_{s2})$ and $V_{o2} = 0.5{*}V_{s1}$ b) $V_{o1} = (2{*}V_{s1}){+}(2{*}V_{s2})$ and $V_{o2} = (2{*}V_{s1})$. Some of the assumptions and solutions are required to be followed for solving the R-parameter analysis which is discussed in Section 4.5.1.

5.3.1 Voltage Ratios of Coupled Case $V_{o1} = (0.5{*}V_{s1}){+}(0.5{*}V_{s2})$ and $V_{o2} = (0.5 * V_{s1})$ are Considered

The equivalent circuit of $V_{o1} = (0.5 * V_{s1}) + (0.5 * V_{s2})$ and $V_{o2} = (0.5 * V_{s1})$ voltage ratios was discussed in Chapter 4. Referring to Figure 4.5 the R_{eq} analysis is derived using Figure 4.3 where phase 1 and phase 3 are the first order RC-circuits, while phase 2 and phase 4 are the higher order ones. Therefore, phases 1 and 3 have one time constant (T_1 and T_4), whereas phases 2 and 4 - two time constants (T_2 and T_3; T_5 and T_6). In addition, time constant values for phases 1 and 3 (as well as phase 2 and 4) are similar due to the symmetry.

$$\begin{aligned} T_1 = \frac{3}{2}rC;\ T_2 = 1.438rC;\ T_3 = 5.562rC; \\ T_4 = \frac{3}{2}rC;\ T_5 = 1.438rC;\ T_6 = 5.562rC. \end{aligned} \tag{5.1}$$

Referring to Figure 4.8(a), DC voltage source (V) is connected at the output terminal (V_{o1}) when the input voltages (V_{s1} and V_{s2}) and V_{o2} are shorted with respect to ground. Capacitor voltage expression for each phase is given by,

$$V_{1C_{12}} = V_{1C_{12}}(0)e^{-\frac{t}{T_1}}; \tag{5.2}$$

$$V_{2C_1} = V + a_{11}e^{-\frac{t}{T_2}} + a_{12}e^{-\frac{t}{T_3}}; \tag{5.3}$$

$$\tag{5.4}$$

$$V_{2C_2} = V + a_{21}e^{-\frac{t}{T_2}} + a_{22}e^{-\frac{t}{T_3}}; \tag{5.5}$$

$$V_{3C_{12}} = V_{3C_{12}}(0)e^{-\frac{t}{T_4}}; \tag{5.6}$$

$$V_{4C_1} = a_{31}e^{-\frac{t}{T_5}} + a_{32}e^{-\frac{t}{T_6}}; \tag{5.7}$$

$$V_{4C_2} = a_{41}e^{-\frac{t}{T_5}} + a_{42}e^{-\frac{t}{T_6}}. \tag{5.8}$$

To find 10 unknown coefficients, a set of 10 linear equations should be constructed. The 1st four equations are from capacitor voltage continuity principle and they are given by,

$$V_{1C_{12}}\left(\frac{T}{4}\right) = V_{2C_1}(0) + V_{2C_2}(0); \tag{5.9}$$

$$V_{2C_1}\left(\frac{T}{4}\right) + V_{2C_2}\left(\frac{T}{4}\right) = V_{3C_{12}}(0); \tag{5.10}$$

$$V_{3C_{12}}\left(\frac{T}{4}\right) = V_{4C_1}(0) + V_{4C_2}(0); \tag{5.11}$$

$$V_{4C_1}\left(\frac{T}{4}\right) + V_{4C_2}\left(\frac{T}{4}\right) = V_{1C_{12}}(0). \tag{5.12}$$

Similarly, the other two equations are from charge conservation between two capacitors plates (C_1 and C_2 in phase 1 and phase 3) are given by,

$$C_1V_{2C_1}\left(\frac{T}{4}\right) - C_2V_{2C_2}\left(\frac{T}{4}\right) = C_1V_{4C_1}(0) - C_2V_{4C_2}(0); \tag{5.13}$$

$$C_1V_{4C_1}\left(\frac{T}{4}\right) - C_2V_{4C_2}\left(\frac{T}{4}\right) = C_1V_{2C_1}(0) - C_2V_{2C_2}(0). \tag{5.14}$$

When output 1 is connected and output 2 is short circuited, then the current i_1 to i_6 is given by (5.15)-(5.21)

$$i_1 = C_{12}\left(-\frac{1}{T_1}V_{1c12}\,(0)\,e^{-\frac{t}{T_1}}\right) \tag{5.15}$$

$$i_2 = C_1\left(\frac{1}{T_2}a_{11}e^{-\frac{t}{T_2}} + \frac{1}{T_3}a_{12}e^{-\frac{t}{T_3}}\right) \tag{5.16}$$

$$i_3 = C_2\left(\frac{1}{T_2}a_{21}e^{-\frac{t}{T_2}} + \frac{1}{T_3}a_{22}e^{-\frac{t}{T_3}}\right) \tag{5.17}$$

$$\tag{5.18}$$

$$i_4 = C_{12}\left(-\frac{1}{T_4}V_{3c12}\left(0\right)e^{-\frac{t}{T_4}}\right) \tag{5.19}$$

$$i_5 = C_1\left(\frac{1}{T_5}a_{31}e^{-\frac{t}{T_5}} + \frac{1}{T_6}a_{32}e^{-\frac{t}{T_6}}\right) \tag{5.20}$$

$$i_6 = C_2\left(\frac{1}{T_5}a_{41}e^{-\frac{t}{T_5}} + \frac{1}{T_6}a_{42}e^{-\frac{t}{T_6}}\right) \tag{5.21}$$

The remaining two equations are derived from phase 2 and phase 4 using partial KVL (only exponential terms) which are given in (5.22) and (5.26)

$$\begin{aligned}&\left(\frac{R_2C_1}{T_2}a_{11}e^{-\frac{t}{T_2}} + \frac{R_2C_1}{T_3}a_{12}e^{-\frac{t}{T_3}}\right) - a_{11}e^{-\frac{t}{T_2}} - a_{12}e^{-\frac{t}{T_3}};\\ =&\left(\frac{R_3C_2}{T_2}a_{21}e^{-\frac{t}{T_2}} + \frac{R_3C_2}{T_3}a_{22}e^{-\frac{t}{T_3}}\right) - a_{21}e^{-\frac{t}{T_2}} - a_{22}e^{-\frac{t}{T_3}};\end{aligned} \tag{5.22}$$

$$\tag{5.23}$$

By solving 5.22), the reduced form is given in (5.24) and (5.25)

$$\left(\frac{R_2C_1}{T_2} - 1\right)a_{11} = \left(\frac{R_3C_2}{T_2} - 1\right)a_{21} \tag{5.24}$$

$$\left(\frac{R_2C_1}{T_3} - 1\right)a_{12} = \left(\frac{R_3C_2}{T_3} - 1\right)a_{22} \tag{5.25}$$

$$\begin{aligned}&\left(\frac{R_6C_1}{T_5}a_{31}e^{-\frac{t}{T_5}} + \frac{R_6C_1}{T_6}a_{32}e^{-\frac{t}{T_6}}\right) - a_{31}e^{-\frac{t}{T_5}} - a_{32}e^{-\frac{t}{T_6}};\\ =&\left(\frac{R_7C_2}{T_5}a_{41}e^{-\frac{t}{T_5}} + \frac{R_7C_2}{T_6}a_{42}e^{-\frac{t}{T_6}}\right) - a_{41}e^{-\frac{t}{T_5}} - a_{42}e^{-\frac{t}{T_6}}.\end{aligned} \tag{5.26}$$

By solving (5.26), the reduced form is given in (5.27) and (5.28)

$$\left(\frac{R_6C_1}{T_5} - 1\right)a_{31} = \left(\frac{R_7C_2}{T_5} - 1\right)a_{41} \tag{5.27}$$

$$\left(\frac{R_6C_1}{T_6} - 1\right)a_{32} = \left(\frac{R_7C_2}{T_6} - 1\right)a_{42} \tag{5.28}$$

Once the coefficients are identified from (5.9) - (5.26) the Y- parameters (Y_{11} and Y_{21}) need to be calculated using the ratio between average current that is flowing through

each load (I_{11} and I_{21}) to source voltage (V) which is given by

$$Y_{11} = \frac{I_{11}}{\mathrm{V}}; \quad Y_{21} = \frac{I_{21}}{\mathrm{V}}. \tag{5.29}$$

Steady state output 1 and output 2 currents of I_{11} are given in (5.31) and I_{11} is derived using (5.15) - (5.19),

$$I_{11} = \frac{1}{T}\left(C_1 a_{11}\left(e^{-\frac{T}{4T_2}} - 1\right) + C_1 a_{12}\left(e^{-\frac{T}{4T_3}} - 1\right) + C_2 a_{21}\left(e^{-\frac{T}{4T_2}} - 1\right) + C_2 a_{22}\left(e^{-\frac{T}{4T_3}} - 1\right)\right); \tag{5.30}$$

$$\frac{1}{T/4}\int_0^{T/4}\left(\frac{C_1}{T_2}a_{11}e^{-\frac{t}{T_2}} + \frac{C_1}{T_3}a_{12}e^{-\frac{t}{T_3}}dt\right) + \frac{1}{T/4}\int_0^{T/4}\left(\frac{C_2}{T_2}a_{21}e^{-\frac{t}{T_2}} + \frac{C_2}{T_3}a_{22}e^{-\frac{t}{T_3}}dt\right) =$$
$$-\frac{4}{T}\left(C_1 a_{11}\left(e^{-\frac{T}{4T_2}} - 1\right) + C_1 a_{12}\left(e^{-\frac{T}{4T_3}} - 1\right) + C_2 a_{12}\left(e^{-\frac{T}{4T_2}} - 1\right) + C_2 a_{22}\left(e^{-\frac{T}{4T_3}} - 1\right)\right). \tag{5.31}$$

Steady state output 1 and output 2 currents of I_{22} are given in (5.33) and I_{22} is derived using (5.20)- (5.21),

$$I_{22} = -\frac{1}{T}\left(C_1 a_{11}\left(e^{-\frac{T}{4T_2}} - 1\right) + C_1 a_{12}\left(e^{-\frac{T}{4T_3}} - 1\right) + C_2 a_{21}\left(e^{-\frac{T}{4T_2}} - 1\right) + C_2 a_{22}\left(e^{-\frac{T}{4T_3}} - 1\right)\right)$$
$$+\frac{1}{T}\left(C_1 a_{31}\left(e^{-\frac{T}{4T_5}} - 1\right) + C_1 a_{32}\left(e^{-\frac{T}{4T_6}} - 1\right) + C_2 a_{41}\left(e^{-\frac{T}{4T_5}} - 1\right) + C_2 a_{42}\left(e^{-\frac{T}{4T_6}} - 1\right)\right) \tag{5.32}$$

$$\frac{1}{T/4}\int_0^{T/4}\left(\frac{C_1}{T_5}a_{31}e^{-\frac{t}{T_5}} + \frac{C_1}{T_6}a_{32}e^{-\frac{t}{T_6}}dt\right) + \frac{1}{T/4}\int_0^{T/4}\left(\frac{C_2}{T_5}a_{41}e^{-\frac{t}{T_5}} + \frac{C_2}{T_6}a_{42}e^{-\frac{t}{T_6}}dt\right) =$$
$$-\frac{4}{T}\left(C_1 a_{31}\left(e^{-\frac{T}{4T_5}} - 1\right) + C_1 a_{32}\left(e^{-\frac{T}{4T_6}} - 1\right) + C_2 a_{41}\left(e^{-\frac{T}{4T_5}} - 1\right) + C_2 a_{42}\left(e^{-\frac{T}{4T_6}} - 1\right)\right) \tag{5.33}$$

Similarly, referring to the Figure 4.8(b) source voltage (V) is applied at the V_{o2} and V_{s1}, V_{s2}, V_{o2} are shorted with respect to ground. Capacitor voltage expression for each phase is given by

$$V_{1C_{12}} = V_{1C_{12}}(0)e^{-\frac{t}{T_1}}; \tag{5.34}$$

$$V_{2C_1} = -V + a_{11}e^{-\frac{t}{T_2}} + a_{12}e^{-\frac{t}{T_3}}; \tag{5.35}$$

$$V_{2C_2} = -V + a_{21}e^{-\frac{t}{T_2}} + a_{22}e^{-\frac{t}{T_3}}; \tag{5.36}$$

$$V_{3C_{12}} = V_{3C_{12}}(0)e^{-\frac{t}{T_4}}; \tag{5.37}$$

$$V_{4C_1} = V + a_{31}e^{-\frac{t}{T_5}} + a_{32}e^{-\frac{t}{T_6}}; \tag{5.38}$$

$$V_{4C_2} = V + a_{41}e^{-\frac{t}{T_5}} + a_{42}e^{-\frac{t}{T_6}}. \tag{5.39}$$

Similarly, for another case of unknown coefficients, a set of 10 linear equations and Y-parameters are calculated by following the same procedure as derived in the previous steps. Using the capacitor voltage continuity principle the other four equations are derived and are shown in (5.40) – (5.43).

$$V_{1C12}\left(\frac{T}{4}\right) = V_{2C1}(0) + V_{2C2}(0) \tag{5.40}$$

$$V_{2C1}\left(\frac{T}{4}\right) = V_{2C2}\left(\frac{T}{4}\right) = V_{3C12}(0) \tag{5.41}$$

$$V_{3C12}\left(\frac{T}{4}\right) = V_{4C1}(0) + V_{4C2}(0) \tag{5.42}$$

$$V_{4C1}\left(\frac{T}{4}\right) = V_{4C2}\left(\frac{T}{4}\right) = V_{1C12}(0) \tag{5.43}$$

Similarly, the other two equations from charge conservation between two capacitors plates (C_1 and C_2 in phase 1 and phase 3) are given by,

$$C_1V_{2C1}\left(\frac{T}{4}\right) - C_2V_{2C2}\left(\frac{T}{4}\right) = C_1V_{4C1}(0) + C_2V_{4C2}(0) \tag{5.44}$$

$$C_1V_{4C1}\left(\frac{T}{4}\right) - C_2V_{4C2}\left(\frac{T}{4}\right) = C_1V_{2C1}(0) + C_2V_{2C2}(0) \tag{5.45}$$

When the output 2 is connected and output 1 is short circuited, then the current i_1 to i_6 is given by (5.46)-(5.51).

$$i_1 = C_{12}\left(-\frac{1}{T_1}V_{1C12}\left(0\right)e^{-\frac{t}{T_1}}\right) \tag{5.46}$$

$$i_2 = C_1\left(\frac{1}{T_2}a_{11}e^{-\frac{t}{T_2}} + \frac{1}{T_3}a_{12}e^{-\frac{t}{T_3}}\right) \tag{5.47}$$

$$i_3 = C_2\left(\frac{1}{T_2}a_{21}e^{-\frac{t}{T_2}} + \frac{1}{T_3}a_{22}e^{-\frac{t}{T_3}}\right) \tag{5.48}$$

$$i_4 = C_{12}\left(-\frac{1}{T_4}V_{3C12}\left(0\right)e^{-\frac{t}{T_4}}\right) \tag{5.49}$$

$$i_5 = C_1\left(\frac{1}{T_5}a_{31}e^{-\frac{t}{T_5}} + \frac{1}{T_6}a_{32}e^{-\frac{t}{T_6}}\right) \tag{5.50}$$

$$i_6 = C_2\left(\frac{1}{T_5}a_{41}e^{-\frac{t}{T_5}} + \frac{1}{T_6}a_{42}e^{-\frac{t}{T_6}}\right) \tag{5.51}$$

The remaining two equations each are derived respectively from phase 2 and phase 4 using partial KVL (only exponential terms) which are given in (5.52) and (5.53).

$$\left(\frac{R_2C_1}{T_2}a_{11}e^{-\frac{t}{T_2}} + \frac{R_2C_1}{T_3}a_{12}e^{-\frac{t}{T_3}}\right) - a_{11}e^{-\frac{t}{T_2}} - a_{12}e^{-\frac{t}{T_3}} \tag{5.52}$$

$$= \left(\frac{R_3C_2}{T_2}a_{21}e^{-\frac{t}{T_2}} + \frac{R_2C_1}{T_3}a_{22}e^{-\frac{t}{T_3}}\right) - a_{21}e^{-\frac{t}{T_2}} - a_{22}e^{-\frac{t}{T_3}} \tag{5.53}$$

$$\left(\frac{R_2C_1}{T_2} - 1\right)a_{11} = \left(\frac{R_3C_2}{T_2} - 1\right)a_{21} \tag{5.54}$$

$$\left(\frac{R_2C_1}{T_3} - 1\right)a_{12} = \left(\frac{R_3C_2}{T_3} - 1\right)a_{22} \tag{5.55}$$

By solving the (5.52) and (5.53), reduced form is given in (5.54) and (5.55). Similarly, (5.56) and (5.57), the reduced form is given in (5.58) and (5.59) .

$$\left(\frac{R_6C_1}{T_5}a_{31}e^{-\frac{t}{T_5}} + \frac{R_6C_1}{T_6}a_{32}e^{-\frac{t}{T_6}}\right) - a_{31}e^{-\frac{t}{T_5}} - a_{32}e^{-\frac{t}{T_6}} \tag{5.56}$$

$$= \left(\frac{R_7C_2}{T_5}a_{41}e^{-\frac{t}{T_5}} + \frac{R_7C_2}{T_6}a_{42}e^{-\frac{t}{T_6}}\right) - a_{41}e^{-\frac{t}{T_5}} - a_{42}e^{-\frac{t}{T_6}} \tag{5.57}$$

$$\left(\frac{R_6C_1}{T_5}-1\right)a_{31}=\left(\frac{R_7C_2}{T_5}-1\right)a_{41} \tag{5.58}$$

$$\left(\frac{R_6C_1}{T_6}-1\right)a_{32}=\left(\frac{R_7C_2}{T_6}-1\right)a_{42} \tag{5.59}$$

Steady state output 1 and output 2 currents of I_{12} are given in (5.60); I_{12} is derived using (5.46) and (5.49),

$$I_{12}=-\frac{1}{T}\left(C_1a_{11}\left(e^{-\frac{T}{4T_2}}-1\right)+C_1a_{12}\left(e^{-\frac{T}{4T_3}}-1\right)+C_2a_{21}\left(e^{-\frac{T}{4T_2}}-1\right)+C_2a_{22}\left(e^{-\frac{T}{4T_3}}-1\right)\right) \tag{5.60}$$

Steady state output 1 and output 2 currents of I_{22} are given in (5.61); I_{22} is derived using (5.50) - (5.51),

$$\frac{1}{T/4}\int_0^{T/4}\left(\frac{C_1}{T_5}a_{31}e^{-\frac{t}{T_5}}+\frac{C_1}{T_6}a_{32}e^{-\frac{t}{T_6}}dt\right)+\frac{1}{T/4}\int_0^{T/4}\left(\frac{C_2}{T_5}a_{41}e^{-\frac{t}{T_5}}+\frac{C_2}{T_6}a_{42}e^{-\frac{t}{T_6}}dt\right)=$$
$$-\frac{4}{T}\left(C_1a_{31}\left(e^{-\frac{T}{4T_5}}-1\right)+C_1a_{32}\left(e^{-\frac{T}{4T_6}}-1\right)+C_2a_{41}\left(e^{-\frac{T}{4T_5}}-1\right)+C_2a_{42}\left(e^{-\frac{T}{4T_6}}-1\right)\right) \tag{5.61}$$

Due to reciprocal relation between resistance and conductance parameters, R-parameters can be found as,

$$\begin{bmatrix}R_{11} & R_{12}\\ R_{21} & R_{22}\end{bmatrix}=\begin{bmatrix}Y_{11} & Y_{12}\\ Y_{21} & Y_{22}\end{bmatrix}^{-1}. \tag{5.62}$$

Finally, the simplified R-parameters calculations for R-parameters coupled case[1] are given in (5.63) - (5.65),

[1]The parameter $R_{12}=R_{21}$ is symmetrized. Therefore, the output 1 affects output 2 in the same way as output 2 affects output 1.

$$R_{11} = -\frac{\left[0.015*exp\left(\frac{0.341}{C*f*r}\right)+0.985*exp\left(\frac{0.174}{C*f*r}\right)+0.015*exp\left(\frac{0.045}{C*f*r}\right)-1.0*exp\left(\frac{0.385}{C*f*r}\right)+0.985*exp\left(\frac{0.212}{C*f*r}\right)-1.0\right]}{C*f*\left[exp\left(\frac{0.167}{C*f*r}\right)-1.0*exp\left(\frac{0.341}{C*f*r}\right)+exp\left(\frac{0.174}{C*f*r}\right)+exp\left(\frac{0.045}{C*f*r}\right)+exp\left(\frac{0.385}{C*f*r}\right)-1.0*exp\left(\frac{0.212}{C*f*r}\right)-1.0*exp\left(\frac{0.219}{C*f*r}\right)-1.0\right]}; \tag{5.63}$$

$$R_{21} = R_{12} = -\frac{9.701*10^{-5}*\left[77*exp\left(\frac{0.341}{C*f*r}\right)+5077*exp\left(\frac{0.174}{C*f*r}\right)+77*exp\left(\frac{0.045}{C*f*r}\right)-5154*exp\left(\frac{0.385}{C*f*r}\right)+5077*exp\left(\frac{0.212}{C*f*r}\right)-5154\right]}{C*f*\left[exp\left(\frac{0.167}{C*f*r}\right)-1.0*exp\left(\frac{0.341}{C*f*r}\right)+exp\left(\frac{0.174}{C*f*r}\right)+exp\left(\frac{0.045}{C*f*r}\right)+exp\left(\frac{0.385}{C*f*r}\right)-1.0*exp\left(\frac{0.212}{C*f*r}\right)-1.0*exp\left(\frac{0.219}{C*f*r}\right)-1.0\right]}; \tag{5.64}$$

$$R_{22} = -\frac{\begin{array}{r}151.6*[0.127*exp\left(\frac{0.507}{C*f*r}\right)-0.127*exp\left(\frac{0.264}{C*f*r}\right)-0.250*exp\left(\frac{0.552}{C*f*r}\right)-0.127*exp\left(\frac{0.597}{C*f*r}\right)-0.002*exp\left(\frac{0.681}{C*f*r}\right)+\\ C*f*\left[2577*exp\left(\frac{0.167}{C*f*r}\right)+2500*exp\left(\frac{0.341}{C*f*r}\right)+2500*exp\left(\frac{0.174}{C*f*r}\right)-2500*exp\left(\frac{0.045}{C*f*r}\right)-2577*exp\left(\frac{0.385}{C*f*r}\right)-2500*exp\left(\frac{0.212}{C*f*r}\right)-2577*exp\left(\frac{0.219}{C*f*r}\right)-2577\right]*\\ +0.127*exp\left(\frac{0.174}{C*f*r}\right)+8.248*exp\left(\frac{0.045}{C*f*r}\right)+8.373*exp\left(\frac{0.045}{C*f*r}\right)+0.002*exp\left(\frac{0.090}{C*f*r}\right)-8.373*exp\left(\frac{0.726}{C*f*r}\right)+8.373*exp\left(\frac{0.378}{C*f*r}\right)]\\ *\left[exp\left(\frac{0.167}{C*f*r}\right)-1.0*exp\left(\frac{0.341}{C*f*r}\right)+exp\left(\frac{0.174}{C*f*r}\right)+exp\left(\frac{0.045}{C*f*r}\right)+exp\left(\frac{0.385}{C*f*r}\right)-1.0*exp\left(\frac{0.212}{C*f*r}\right)-1.0*exp\left(\frac{0.219}{C*f*r}\right)-1.0\right]\\ +\left[8.5*exp\left(\frac{0.771}{C*f*r}\right)-8.373*exp\left(\frac{0.393}{C*f*r}\right)-8.248*exp\left(\frac{0.423}{C*f*r}\right)+0.250*exp\left(\frac{0.219}{C*f*r}\right)-8.5\right]\end{array}}{1}. \tag{5.65}$$

5.3.2 Voltage Ratios of Coupled Case $V_{o1} = (2 * V_{s1}) + (2 * V_{s2})$ and $V_{o2} = 2 * V_{s1}$ are Considered

To solve the coupling case the R-parameters are derived using following analytical process, i.e. RC network and partial KVL methods. For simplicity, $\mathrm{V_{o1}} = (2 * \mathrm{V_{s1}}) + (2 * \mathrm{V_{s2}})$ and $\mathrm{V_{o2}} = 2 * \mathrm{V_{s1}}$ voltage ratio are considered for upcoming R-parameters analysis. The same assumptions, which are discussed in Section 5.3, are followed. From Figure 5.1, Phase 2 and Phase 4 are the first order RC-circuits, while Phase 1 and Phase 3 are the higher order ones. Therefore, Phase 2 and Phase 4 have one time constant (T_3 and T_6 respectively), whereas Phase 1 and Phase 3 - two time constants (T_1 and T_2; T_4 and T_5 respectively). In addition, time constant values for Phase 1 and Phase 3 (as well as Phase 2 and Phase 4) are similar due to the equivalence of topologies.

Table 5.2: Pulse pattern of coupled voltage ratio

voltage ratio	Phase	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
	Phase 1	0	1	1	0	1	1	0	0	1	0	0
$V_{o1} = 2 * V_{s1}$	Phase 2	0	0	0	0	1	0	0	1	1	1	0
$V_{o2} = (2 * V_{s1}) + (2 * V_{s2})$	Phase 3	1	0	1	0	1	1	0	0	1	0	0
	Phase 4	0	0	0	1	1	0	0	1	0	0	1

$$R_1 = 2r; \quad R_2 = 2r + ESR; \quad R_3 = r + ESR; \tag{5.66}$$

$$R_4 = 4r + 2ESR; \quad R_5 = 2r; \quad R_6 = 2r + ESR; \tag{5.67}$$

$$R_7 = r + ESR; \quad R_8 = 4r + 2ESR; \tag{5.68}$$

$$C_1 = C; \quad C_2 = C; \quad C_{12} = C/2; \tag{5.69}$$

$$T_1 = T_4 = 2C\frac{(ESR^2 + 7ESRr + 8r^2)}{(2ESR + 7r + (\sqrt{17})r)}; \tag{5.70}$$

$$T_2 = T_5 = 2C\frac{(ESR^2 + 7ESRr + 8r^2)}{(2ESR + 7r - (\sqrt{17})r)}; \tag{5.71}$$

$$T_3 = T_6 = C(ESR + 2r). \tag{5.72}$$

Referring to Figure 4.8(a), voltage source (V) is applied at output 1 (input voltages and output 2 are short-circuited). Capacitor voltage expressions for each phase are

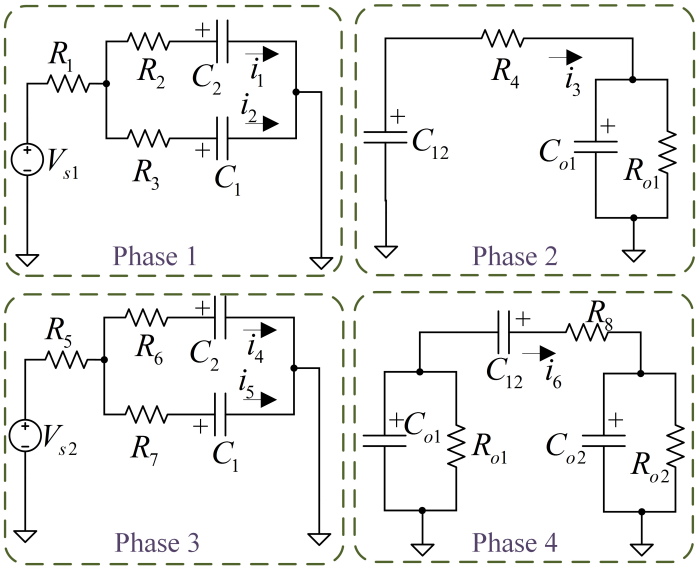


Figure 5.1: Different phases of proposed converter $\mathrm{V_{o1}} = (2 * \mathrm{V_{in1}}) + (2 * \mathrm{V_{in2}})$ and $\mathrm{V_{o2}} = 2 * \mathrm{V_{in1}}$.

given by

$$V_{1C1}(t) = a_{11}e^{(-t/T_1)} + a_{12}e^{(-t/T_2)}; \tag{5.73}$$

$$V_{1C2}(t) = a_{21}e^{(-t/T_1)} + a_{22}e^{(-t/T_2)}; \tag{5.74}$$

$$V_{2C12}(t) = V + (V_{2C12}(0) - V)e^{(-t/T_3)}; \tag{5.75}$$

$$V_{3C1}(t) = a_{31}e^{(-t/T_4)} + a_{32}e^{(-t/T_5)}; \tag{5.76}$$

$$V_{3C2}(t) = a_{41}e^{(-t/T_4)} + a_{42}e^{(-t/T_5)}; \tag{5.77}$$

$$V_{4C12}(t) = -V + (V_{4C12}(0) + V)e^{(-t/T_6)}. \tag{5.78}$$

To find unknown coefficients a set of 10 linear equations needs to be derived. Among those, five equations are from capacitor voltage continuity principle and given in (5.79)-(5.82)

$$V_{1C1}(T/4) + V_{1C2}(T/4) = V_{2C12}(0); \tag{5.79}$$

$$V_{2C12}(T/4) = V_{3C1}(0) + V_{3C2}(0); \tag{5.80}$$

$$V_{3C1}(T/4) + V_{3C2}(T/4) = V_{4C12}(0); \tag{5.81}$$

$$V_{4C12}(T/4) = V_{1C1}(0) + V_{1C2}(0). \tag{5.82}$$

Other two equations (5.83) and (5.84) are from charge conservation between two capacitor plates C_1 and C_2 during phase 2 and 4 which are given by,

$$C_2V_{1C2}(T/4) - C_1V_{1C1}(T/4) = C_2V_{3C2}(0) - C_1V_{3C1}(0); \tag{5.83}$$

$$C_2V_{3C2}(T/4) - C_1V_{3C1}(T/4) = C_2V_1C2(0) - C_1V_{1C1}(0). \tag{5.84}$$

The other two equations (5.86) and (5.87) are from partial KVL (only exponential terms) of Phase 1 and are given by

$$i_1(t)R_2 + V_{1C2}(t) = i_2(t)R_3 + V_{1C1}(t); \tag{5.85}$$

$$\left(1 - \frac{R_2C_2}{T_1}\right) a_{21} = \left(1 - \frac{R_3C_1}{T_1}\right) a_{11}; \tag{5.86}$$

$$\left(1 - \frac{R_2C_2}{T_1}\right) a_{22} = \left(1 - \frac{R_3C_1}{T_1}\right) a_{12}. \tag{5.87}$$

The last two equations (5.89) and (5.90) are from partial KVL of Phase 3 and are given by

$$i_4(t)R_6 + V_{3C2}(t) = i_5(t)R_7 + V_{3C1}(t); \tag{5.88}$$

$$\left(1 - \frac{R_6C_2}{T_4}\right) a_{41} = \left(1 - \frac{R_7C_1}{T_4}\right) a_{31}; \tag{5.89}$$

$$\left(1 - \frac{R_6C_2}{T_5}\right) a_{42} = \left(1 - \frac{R_7C_1}{T_5}\right) a_{32}. \tag{5.90}$$

Average currents from the loads (I_{11} and I_{21}) are given by

$$I_{11} = \frac{1}{T}\left(\int_0^{(T/4)} i_6(t)dt - \int_0^{(T/4)} i_3(t)dt)\right); \tag{5.91}$$

$$I_{21} = -\frac{1}{T}\int_0^{(T/4)} i_6(t)dt. \tag{5.92}$$

Similarly, Y-parameters (Y_{11} and Y_{21}) are calculated as

$$Y_{11} = \frac{I_{11}}{V}; \quad Y_{21} = \frac{I_{21}}{V}. \tag{5.93}$$

Referring to Figure 4.8(b), voltage source (V) is applied at the output 2 (input voltages

and output 1 are short-circuited). Capacitor voltage expressions for each phase (same as previous except $V_{2C12}(t)$ and $V_{4C12}(t)$) are given by

$$V_{2C12}(t) = V_{2C12}(0)e^{(-t/T_3)}; \tag{5.94}$$

$$V_{4C12}(t) = V + (V_{4C12}(0) - V)e^{(-t/T_6)}. \tag{5.95}$$

The set of 10 linear equations are similar to the previous case. The derivation of average currents from the loads I_{12} is similar to I_{11}, while I_{22} is similar to I_{21}. Y-parameters (Y_{12} and Y_{22}) are calculated as is shown in (5.96)

$$Y_{12} = \frac{I_{12}}{V}; \quad Y_{22} = \frac{I_{22}}{V}. \tag{5.96}$$

Using (5.62) we can easily find the R-parameters. The final expression of R-parameters is quite long and cannot be expressed. It is expressed using MATLAB[2] code.

5.4 Measurements and Discussion

Simulation and experiment of the DIDO coupled case are discussed in this Section and the simulation parameters strictly follow the circuit ratings as discussed in Section 4.3.3.

5.4.1 Voltage ratios of V_{o1} =$(0.5 * V_{s1})$+$(0.5 * V_{s2})$ and $V_{o2} = 0.5 * V_{s1}$

For modeling the coupled converter, equivalent resistance needs to be calculated and it is verified by PSIM simulation. Finally, Table 5.3 presents modelled, simulated and experimental comparison of coupled and decoupled voltage ratios. The simulation output voltages of the voltage ratios (V_{o1} =$(0.5 * \mathrm{V_{s1}})$+$(0.5 * \mathrm{V_{s2}})$ and $\mathrm{V_{o2}} = 0.5 * \mathrm{V_{s1}}$) were discussed in Chapter 4 referring to Figure 4.7. From Table 5.3 it is clear that modelled and simulated results are in good agreement and to verify the coupled case of proposed converter, are in good agreement to each other.

[2]Symbolic calculations were made in MATLAB software. The final results are are discussed in Appendix C.2.

Table 5.3: Comparison results of R-parameters with different frequencies

Frequency	Parameter	R_{11}, Ω	R_{21}, Ω	R_{12}, Ω	R_{22}, Ω
100 kHz	Modelling	9.210	4.605	4.605	4.018
	Simulation	9.201	4.599	4.599	4.015
50 kHz	Modelling	9.241	4.621	4.621	4.046
	Simulation	9.234	4.621	4.616	4.043

5.4.2 Voltage ratios of $V_{o1} = 2 * V_{s1}$ and $V_{o2} = (2 * V_{s1}) + (2 * V_{s2})$

In Coupled case, boost converter usage is very low compared to buck converter for low power applications, i.e., whenever boost converter is required, V_{s2} source is used. For simplicity, $V_{o1} = (2 * V_{s1}) + (2 * V_{s2})$ and $V_{o2} = 2 * V_{s1}$ voltage ratios are considered for simulation, modelling and experimental verification. Figure 5.2 shows the

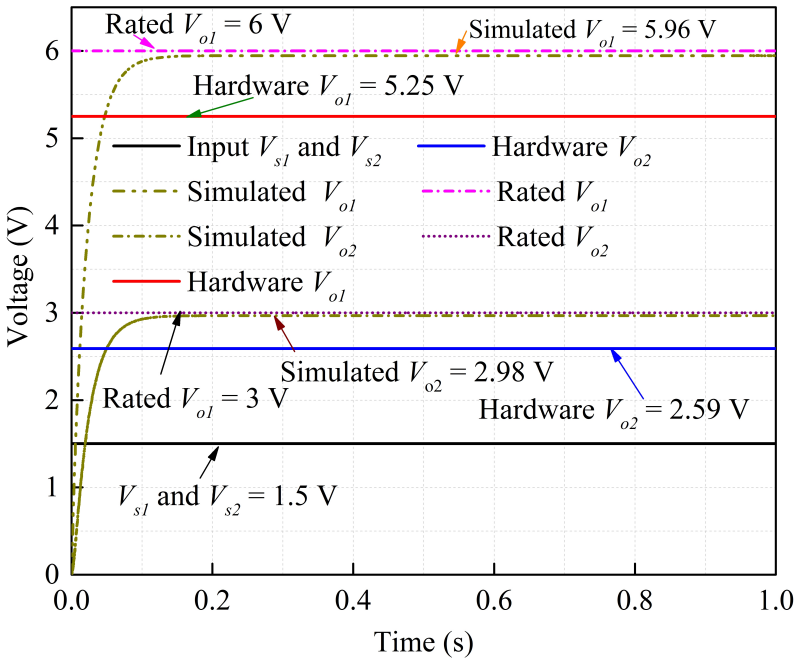


Figure 5.2: Simulation, experimental and analytical voltage of V_{o1} and V_{o2} Voltage ratio of $V_{o1} = 2 * V_{s1}$ and $V_{o2} = (2 * V_{s1}) + (2 * V_{s2})$.

coupled case voltage ratio of the DIDO coupled case and validates by comparing with hardware[3] and simulation results. The voltage ratios are solved mathematically and validated by simulation and experimental results which are shown in Table 5.4. The

[3]The hardware prototype is designed and it is discussed in the previous Chapter 4. The Board size is shown in Figure E.1(d)

input voltage used for coupled voltage ratio is 1.5 V – 3 V because MAX4567 switch (Abraham et al., 2018) has limitation of 10 V. The DIDO converter provides high efficiency and maximum voltage ratios can be generated. The major advantage of the DIDO SCC is that voltage ratio can be generated independently in each output terminal.

Table 5.4: Modelling, analysis comparison of coupled voltage ratios

f, kHz	Modelling				Simulation			
	R_{11}	R_{21}	R_{12}	R_{22}	R_{11}	R_{21}	R_{12}	R_{22}
10	14.75	21.28	21.28	42.56	14.69	21.12	21.12	42.38
50	12.69	19.67	19.67	39.34	12.58	19.46	19.46	38.96
100	12.62	19.62	19.62	39.23	12.51	19.41	19.41	38.85

5.5 Conclusion

R-parameters analysis for coupled cases of dual output SCC is implemented. Coupling was analyzed by a new approach which treated dual output SCC as two-port system. Cross regulation parameters were calculated and validated with simulations and mathematical proof.

Chapter 6

INVERTED SCC

In Chapter 3 general ideology for developing inverted voltage ratios is illustrated and validated using 10 switches and 2 capacitors. In this chapter, Inverting SCC (ISCC) for driving the white light emitting diodes (WLEDs) is implemented and analyzed. The various voltage ratios are selected to control the WLEDs blacklight and it helps to save the battery life. Developing maximum voltage ratios for power converter ICs and equivalent resistance (R_{eq}) accurate calculation include all conduction and ohmic losses. Accurate R_{eq} analyses validates the accuracy of the proposed topology and the calculation results are verified with the experimental ones, particularly at the transition region (between slow switching limit (SSL) and fast switching limit (FSL)).

Parts of this chapter were previously published in the IEEE Transactions on Circuits and Systems II: Express Briefs in December 2018 (Subburaj et al., 2018a).

6.1 Reconfigured Inverted SCC

ISCC plays a vital role in micro power electronics devices and mainly it is used for driving[1] the WLEDs blacklight in different voltage conditions. The power circuit of ISCC is depicted in Figure 6.1 which is developed using general Fibonacci schematic (Kushnerov, 2014b) using 10 bidirectional switches and three flying capacitors. The proposed ISCC generates 7 voltage ratios (Mahnashi and Peng, 2017), (-1/2V_{in}, -1/3V_{in}, -1/4V_{in}, -1V_{in}, -2V_{in}, -3V_{in} and -4V_{in}) and the switching sequence of the

[1]On-chip model of WLEDs driving circuit

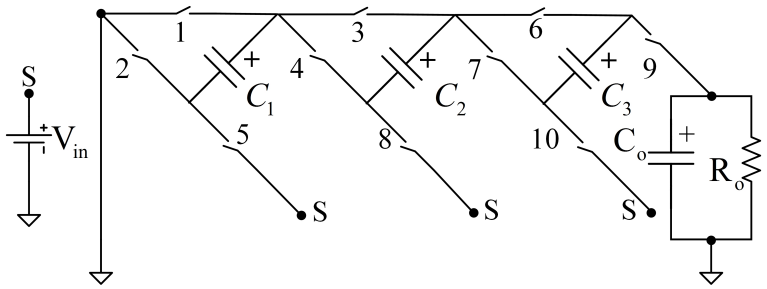


Figure 6.1: Proposed circuit implementation of ISCC.

voltage ratios are shown in Table 6.1. Two phases, ϕ_1 and ϕ_2, are used for driving the bidirectional switches (1 to 10). ϕ_1 and ϕ_2 are 50% duty cycle non-overlapping clocks, where ϕ_1 is considered as the charging phase and ϕ_2 is the discharging phase. The voltage ratio of the negative outputs (Mahnashi and Peng, 2017) can be quantified as follows:

$$\frac{\mathrm{V_{in}}}{\mathrm{V_o}} = -\frac{P}{Q}; \quad 1 \leq max|P,Q| < \mathrm{F}_{i+2}, \tag{6.1}$$

where P and Q follow Fibonacci series, and F_i is a Fibonacci number. The flying capacitors ($\mathrm{C_1}$ to $\mathrm{C_3}$) are charged through negative terminal and discharged via positive terminal to generate negative voltage ratios. For each voltage ratio, individual gating

Table 6.1: Negative voltage ratios

voltage ratios	Switches									
	1	2	3	4	5	6	7	8	9	10
-2 $*$ $\mathrm{V_{in}}$	ϕ_1	ϕ_2	ϕ_2	ϕ_1	ϕ_1	ϕ_1	-	ϕ_2	ϕ_1	-
-3 $*$ $\mathrm{V_{in}}$	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1	ϕ_1	ϕ_2	ϕ_1	ϕ_2	ϕ_1

is chosen and used to generate the signals for controlling the bidirectional switches. For the simplicity, -2$\mathrm{V_{in}}$ voltage ratio is considered for designing the converter and calculating the corresponding R_{eq}. The switches 2, 3, and 8 are connected to charge the flying capacitors in negative directions (Phase 2) and discharge (Phase 1) using switches 1, 4, 5, 6, and 9. Equivalent circuit of ISCC for both Phase 1 and Phase 2 and the accurate calculations for both phases are discussed in the following Sections.

6.2 Equivalent Resistance, R_{eq} Analysis

R_{eq} is helpful for SCC to calculate conduction and ohmic losses in semiconductor components used in the reconfigured ISCC. Kushnerov in (Kushnerov, 2014b) explains the generalised equivalent circuit model of SCC for an average output voltage ($\mathrm{V_{out}} = -\mathrm{n} * \mathrm{V_{in}}$) where, n is the target ratio and $\mathrm{V_{in}}$ is the input voltage, which was discussed in Chapter 3 with reference to Figure 3.2. Simple way to understand the measurement of R_{eq} (Abraham et al., 2018) consists of connecting the current source at load and setting the input DC source to 0 V as depicted in Figure 6.2. Finally, the probe is connected to measure the average output voltage across output capacitor as shown in Figure 6.2. Abraham et al. (Abraham et al., 2018) explained the analysis of R_{eq} in basic circuit theory concept using first order RC network. If the switch-

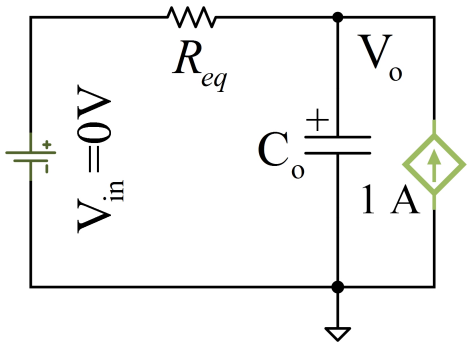


Figure 6.2: Validation model of R_{eq} (Abraham et al., 2018)

ing frequency is low, the associated time period is large, then, the flying capacitor may be fully charged and discharged, the first case being called the slow switching limit (SSL). On the contrary, if the switching frequency is high, then the time period is small and consequently, the flying capacitor cannot be completely charged. This second case is said to be the fast switching limit (FSL) mode (Kushnerov, 2014b, Abraham et al., 2017). R_{eq} analysis is studied by many researchers (Zhaikhan et al., 2017, Kushnerov, 2014b, Junussov and Ruderman, 2015) but assuming infinite filter capacitances, they provide approximate results. The most popular Seeman (Seeman and Sanders, 2008), who derived the R_{eq} formula is given by,

$$R_{eq} = \left[(\mathrm{R_{SSL}})^2 + (\mathrm{R_{FSL}})^2\right]^{1/2}. \tag{6.2}$$

where R_{FSL} and R_{SSL} are fast switching and slow switching R_{eq}. On the other hand, Makowski (Seeman, 2009) explains another formula for R_{eq}, given by,

$$R_{eq} = \left[(R_{SSL})^{2.545} + (R_{FSL})^{2.545}\right]^{1/2.545}. \tag{6.3}$$

According to equation (6.2) and (6.3), R_{eq} calculations are approximate. To overcome these issues, accurate equivalent resistance is calculated and it is validated using ISCC which is designed for mobile applications.

Kushnerov (Kushnerov, 2014b) explains to identify the charge flow equation on SCC on each switching intervals. The steps to be followed for generating linear equation are:

1. Consider steady state value as zero.

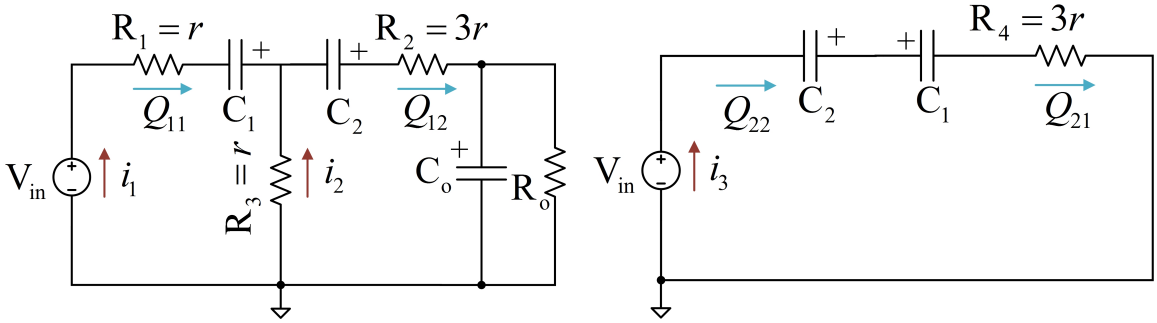
2. Apply Kirchoff current law (KCL).

3. Total charge is added and equated to linear equations.

According to Kushernov's solution in (Kushnerov, 2014b), charge balance equations define a relation in magnitude between the charges flowing during each phase. The last one defines their absolute value (scale) based on the net charge supplied to the load. Kushnerov's method (Kushnerov, 2014b) finds accurate equivalent resistance by computing average phase currents in terms of load current, based on the charge balance equations. However, this approach was applicable only for the first order RC circuits.

Accurate R_{eq} method that can deal with higher order RC circuits was proposed by Mustafa et al. in (Mustafa et al., 2018b). In this method, R_{eq} is calculated by using the charge balance and partial KVL equations.

To analyse the ISCC, assumptions are to be considered as explained in (Mustafa et al., 2018b). High order RC circuit are used for each switching phase. ISCC charged capacitors are determined by solving linear algebraic equation. Calculation of overall losses can be solved by considering the exponential currents in the circuit and then by successively measuring squared current in the given time intervals and computing R_{eq}. The comparison between R_{eq} methods (Kushnerov, 2014b, Seeman, 2009, Mustafa et al., 2018b) is made in Section 6.5.



(a) Phase 1 (ϕ_1) (b) Phase 2 (ϕ_2)

Figure 6.3: Equivalent circuit of proposed converter for -2V_{in} voltage ratio.

6.3 Detailed Accurate Equivalent Resistance Calculation

The basic concept of accurate equivalent resistance calculation for multiphase are discussed in Section 4.5. Accurate equivalent resistance calculations are derived using charge flow balance equations using Figure 6.3 as given below,

$$Q_{21} - Q_{11} = 0; \tag{6.4}$$

$$Q_{22} + Q_{12} = 0; \tag{6.5}$$

$$Q_{12} = Q, \tag{6.6}$$

where Q - net charge is delivered to the load. By solving the (6.4) – (6.6) charge flow solution is given by

$$Q_{11} = Q_{21} = Q_{22} = -Q; \quad Q_{12} = Q. \tag{6.7}$$

For accurate calculation, equal switch resistances (r) and switched capacitances (C) are considered. Capacitor ESR was not considered in calculations and based on the requirement, ESR can be included. Phase 1 (Figure 6.3(a)) is the 2nd order circuit that has two time constants (T_1 and T_2). Phase 2 (Figure 6.3(b)) has only series connections that correspond to the 1st order circuit with one time constant (T_3) where the time constants T_1, T_2, and T_3 are given by

$$T_1 = 1.59r\text{C}; \quad T_2 = 4.41r\text{C}; \quad T_3 = (3/2)r\text{C}. \tag{6.8}$$

Following the methodology in (Mustafa et al., 2018b) for Phase 1 and methodology in (Zhaikhan et al., 2017) for Phase 2, the equivalent resistance (R_{eq}) of ISCC can be calculated.

6.3.1 Phase 1 Capacitor Currents

In order to find 4 unknown coefficients of Phase 1 capacitor currents (6.9), (6.10), a set of 4 linear equations are developed as given in (6.11), (6.12),

$$i_1(t) = a_{11}e^{-t/T_1} + a_{12}e^{-t/T_2}; \tag{6.9}$$

$$i_2(t) = a_{21}e^{-t/T_1} + a_{22}e^{-t/T_2}, \tag{6.10}$$

where three equations are developed using capacitor charge flow methodology as explained in (6.11). The other two equations are developed from partial KVL method which is explained in (6.12) using Figure 6.3(a).

$$\int_0^{T/2} i_1(t)dt = -\int_0^{T/2} (i_1(t) + i_2(t))dt = -Q; \tag{6.11}$$

$$i_1(t)r + \frac{1}{\mathrm{C}}\int_0^{T/2} i_1(t)dt = i_2(t)r, \tag{6.12}$$

where T is a switching period.

6.3.2 Phase 2 Capacitor Current

To find unknown coefficient of Phase 2 capacitor current (6.13), one equation (6.14) is sufficient from charge flow methodology and it is derived using Figure 6.3(b) that is given by,

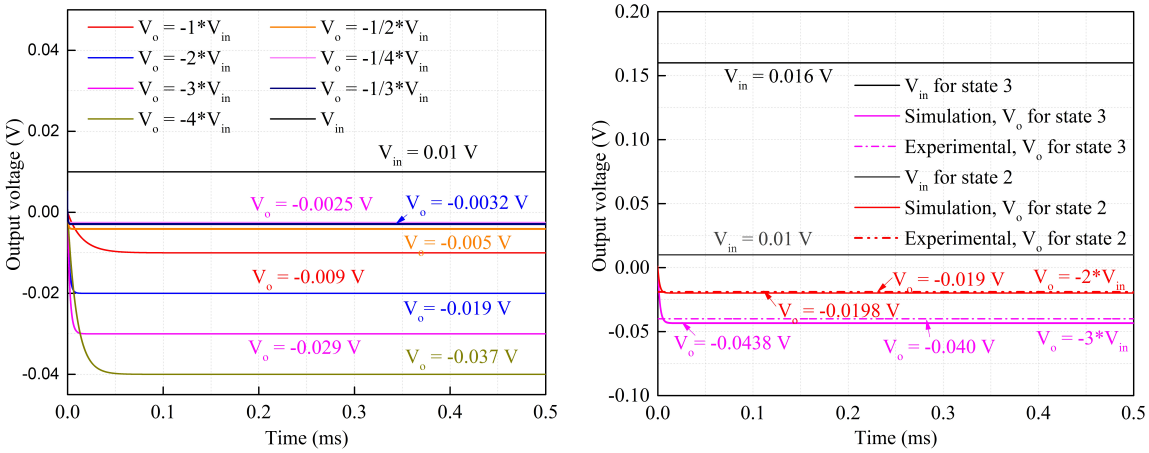
$$i_3(t) = Ae^{-t/T_3}; \tag{6.13}$$

$$\int_0^{T/2} i_3(t)dt = -Q. \tag{6.14}$$

R_{eq} that is calculated by finding power loss (squared currents integrals) on each segment is given by

$$R_{eq} = \frac{1}{\mathrm{C}f}\coth\left(\frac{1}{6r\mathrm{C}f}\right) + \frac{1}{6.83\mathrm{C}f}\coth\left(\frac{1}{6.34r\mathrm{C}f}\right) + \\ + \frac{1}{1.17\mathrm{C}f}\coth\left(\frac{1}{17.66r\mathrm{C}f}\right). \tag{6.15}$$

where f is the switching frequency. The first term[2] of expression (6.15) corresponds to Phase 2, while the last two terms concern Phase 1 (one for each time constant).



(a) (b)

Figure 6.4: Simulation results of ISCC: (a) V_o time response for all voltage ratios; (b) Comparison between Experiment and Simulation results for -2V_{in} and -3V_{in} voltage ratios.

6.4 Experimental Verification and Discussion

The proposed converter is validated using MAX4567 switches (Abraham et al., 2018) and the capacitors, 22 μF flying capacitors and 220 μF output capacitors with ESR equal to 100 mΩ. To drive the backlight WLEDs, minimum output voltage needs to be 800 mV. But the MAX4567 switch can be varied from 10 V to -50 mV. For simplicity and validation of the converter voltage ratios the prototype model is im-

[2]Matlab code for R_{eq} code is discussed in APPENDIX D

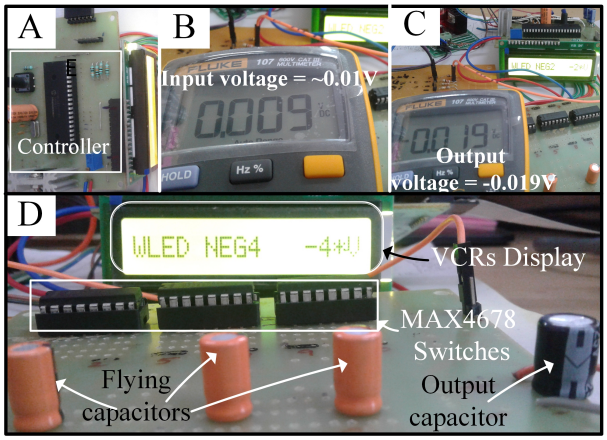


Figure 6.5: Experimental setup of the proposed ISCC.

plemented using the input voltage[3] ≈0.01 V. Simulation results of all ISCC voltage ratios are shown in Figure 6.4(a). Experimental results for two different input and different voltage ratios are shown in Figure 6.4(b). From Figure 6.4(b) simulation and experimental results are in good agreement with each other even in larger load conditions. The overall prototype[4] of the ISCC[5] with the switching controller for ISCC CMOS bidirectional switches is depicted in Figure 6.5. Experimental results[6] for (-2∗V_{in}) are shown in Figure 6.5. B and Figure 6.5. C where the input voltage is ≈0.01 V and the output voltage is -0.019 V. Figure 6.5. D shows the overall prototype of the reconfigured ISCC. On the other hand, tests were also performed for -3V_{in}. The corresponding experimental results is depicted in Figure 6.6 where the input voltage for this particular voltage ratio is 16 mV and the output voltage is -40 mV. Comparison of all voltage ratios model, simulated and hardware results are discussed in Figure 6.7(a). Figure 6.7(b) shows a comparative study and details of accurate R_{eq} analysis, simulation and experimental results. The conditions were identical with the 3 approaches: ESR of 0.1 Ω and R_o = 1 kΩ. From Figure 6.7(b), it is seen that the ISCC accurate R_{eq}, the simulation R_{eq} and the experimental R_{eq} are in good agreement.

[3]It is generated using voltage divider circuit and the ESR is not considered for the analysis. It losses are very low and it is negligible.

[4]Board size is shown in Figure E.1(e)

[5]The Proteous model is shown in Figure D.1

[6]Multi-purpose designed PCB circuit is used and it is shown in Figure C.2

Table 6.2: Comparison with different ISCC and R_{eq} analysis.

Parameters	(Makowski, 2012)	(Evzelman and Ben-Yaakov, 2013)	(Zhaikhan et al., 2017)	This work
voltage ratio	-	4	19	7
Voltage ratios	-	Negative	Positive	Both
V_{in}	1.8 V	1 V	1 V to 8 V	10 mV – 0.5V
V_o	-4 V	-1, 1, 2	Variable	-100 mV – -1.5 V
f	0.5 MHz	500 kHz	NA	50 – 100 kHz
Flying capacitors	NA	2	3	3
R_{eq} Analysis	NA	NA	Approximate	Accurate
R_{eq} Methods	NA	NA	KCL and KVL	R-Parameters
R_o	NA	NA	500 Ω – 5 kΩ	1 kΩ – 1 MΩ
Efficiency	81.9%	NA	90%-95%	85-95%

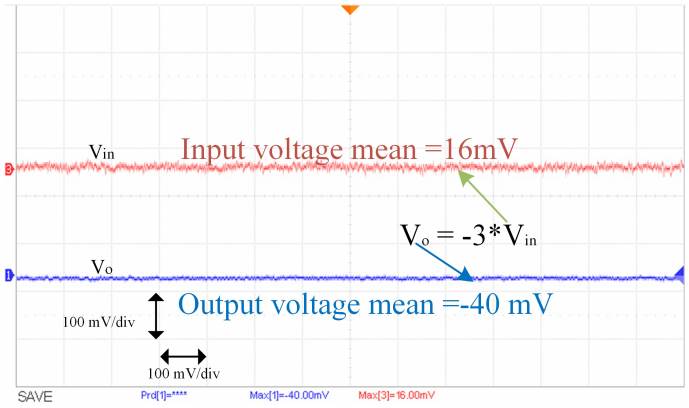


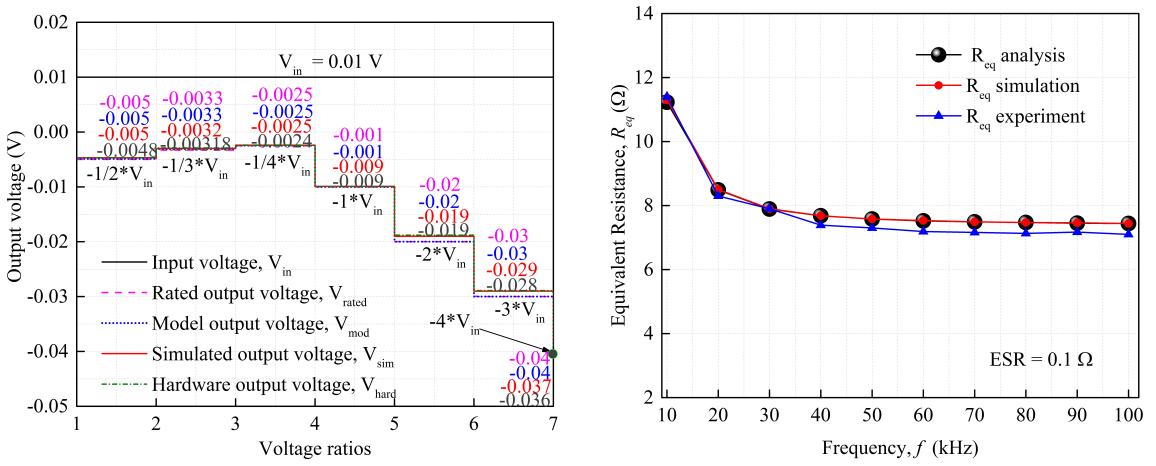
Figure 6.6: Experimental results of -3V_{in} when R_o is 1 kΩ.

6.5 Comparison With Accurate and Approximate ISCC R_{eq} Analysis

Equivalent resistance is calculated for each method and discussed in this Section. The equivalent resistance of accurate calculation is derived in Section 6.3 and the final R_{eq} equation is given in (6.15). Approximate R_{eq} using SSL and FSL solution is given in (6.16),

$$\mathrm{R_{SSL}} = 2/(\mathrm{C}f); \quad \mathrm{R_{FSL}} = 22r. \tag{6.16}$$

Seeman (Seeman, 2009) and Makowski (Makowski, 2012) approximate equations for ISCC are discussed in Section 6.2 equations (6.2) and (6.3). Comparison result of accurate and approximate method of ISCC is depicted in Figure 6.8. Two cases are plotted in the Figure 6.8. One is for equal flying capacitances C = 10 μF and switch resistances $r = 1\ \Omega$. Similarly, experimental data are compared and plotted for equal flying capacitances C = 22 μF and switch resistances $r = 0.3\ \Omega$. It should be noted that approximate equivalent resistance calculation coincides with the accurate one only in the FSL and SSL regions. However, in the transition region the difference is considerable as shown in Figure 6.8. The recent finding of accurate equivalent resistance calculation (Mustafa et al., 2018b) shows that there is no need to calculate FSL and SSL separately. Therefore, there is a better elegant way to accurately calculate equivalent resistance over the whole switching interval by using the approach proposed in (Mustafa et al., 2018b).



(a) Comparison of modeled, simulated and experimental results

(b) Comparison between accurate R_{eq} analysis, experimental and simulation results for -2V_{in} voltage ratio

Figure 6.7: Comparison between results for ISCC.

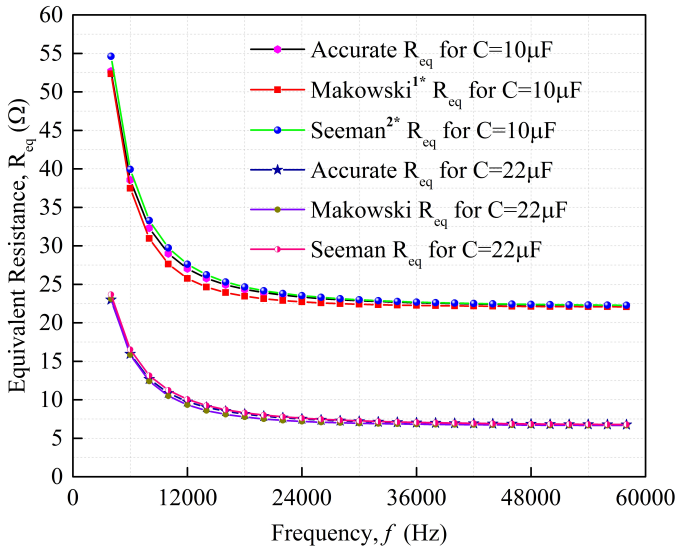


Figure 6.8: Comparison of ISCC accurate R_{eq} with Seeman (Seeman, 2009) and Makowski (Makowski, 2012).

1* = Makowski, 2012 et al. and **2*** = Seeman, 2009 et al.

6.6 Conclusion

The working concept of the ISCC which is mostly used in micro power applications is analysed and verified experimentally. Compared to all ISCC methods, the reconfigured ISCC provides high efficiency and maximum voltage ratios as shown in Table 6.2.

Comparison shows that for the range of frequencies between SSL and FSL those two methods cannot be accurate enough for modeling losses of SCC.

Chapter 7

CONCLUSION AND FUTURE WORK

7.1 Conclusion

This research aimed at providing an insight into the fascinating new areas of SCC, having the potential to replace the inductor based conventional converters. There are numerous low power applications where SCC due to its high energy density, compact size (due to absence of inductors) and easy on chip integration can be a preferred choice. The thesis is presented in seven chapters. A thorough review about the basic working principle, types of SCC and accepted equivalent circuit representation has been extensively made and presented in the first chapter. A few industrial SCC based regulators have also been highlighted.

In Chapter 2 Fibonacci SCCs was developed for both step-up/step-down configuration for missing voltage ratios (1/6 and 5/6) using the Tribonacci series of Farey sequence order 2^3. Arbitrary values (0, 1, 0) were chosen for generating the sequence to solve the missing voltage ratios and validated using experimental and simulation results. To overcome fractional voltage ratios, non unity and unity voltage ratios were developed using DISO SCC topologies which were discussed in Chapter 3. A reconfigurable highly efficient CMOS based dual input variable output buck boost SCC topologies were designed and validated using simulation and experiment. DISO SCC used only 10 CMOS switches and 2 flying capacitors with less complicated renewable energy source and battery. The converter was modelled to predict the exact output

voltage based on the equivalent resistance. The modelled, simulated and experimental results were in good agreement with the theoretical predictions. The converter delivered high efficiency in open loop conditions and there was significant increase in efficiency due to reduced switch count, low weight and size making it an excellent choice for on chip integration. In DISO SCC topologies, only non unity voltage ratios were developed and less voltage ratios being possible to develop to overcome the issue, DIDO SCC was designed and discussed in Chapter 4. The design for DIDO SCC used two capacitors and 11 switches without any magnetic elements. DIDO converter was analyzed and modeled for all 56 votlage ratios by using equivalent resistance and verified by applying the same values in simulation. The simulation values and modelling values were in good agreement for a new converter design. The proposed design was mainly advantageous for power management ICs. In DIDO converter two cases were considered; they are coupled and decoupled cases. Decoupled cases were performed and validated using general equivalent resistance analysis but coupled case was difficult to solve using generalized equivalent resistance calculation. The detailed equivalent resistance calculation was solved and explained using two port system which was explained in Chapter 5. The DIDO design for coupled output SCC was implemented and validated using R-parameters. In this designed converter, detailed analysis and modelling was performed for coupled cases. Modelling was based on R-parameters coming from two-port network approach. Voltage ratios implementation which had series connection of loads was found to have large coupling resistances, which affected the regulation of outputs. Mathematical model for output voltage cross regulation was provided and verified with simulations and experiment. Decoupled case was also analysed with R-parameters. The effect of transresistances was practically negligible for this case. Therefore, with decoupled outputs mathematical modelling could be simplified by treating dual output SCC as two separate single output SCCs. Finally, in Chapter 6 the working concept of the ISCC which is mostly used in micro power applications was analysed and verified experimentally. Compared to all ISCC methods the proposed ISCC provided high efficiency and maximum voltage ratios. ISCC was designed for three stage converter using ten switches and three flying capacitors which generated seven voltage ratios. It achieved 95% peak efficiency where the losses were not considered. Further, the accurate equivalent resistance analysis of ISCC included ohmic and conduction losses, which were analysed and validated using experimental setup. ISCC showed good results in theoretical, simulation and experimental vali-

dations. The accurate equivalent resistance calculation and simulation results were almost overlapping. Finally, accurate equivalent resistance calculation which was validated for ISCC was compared with two approximate methods suggested by (Seeman and Sanders, 2008) and (Maksimovic and Dhar, 1999). Comparison showed that for the range of frequencies between SSL and FSL those two methods may not be accurate enough for modelling losses of SCC.

7.2 Future scope

The possible future improvements on the converter that has been presented in this work along with possible extension and new application domain are indicated below:

1. The application of proposed SCC topologies to On-chip integration circuit in SCL 180 nm technology may be investigated.

2. Design and implementation of fractional voltage ratios such as 1/3, 1/4, . . in DIDO SCC may be considered.

3. Development and implementation of fractional negative voltage ratios for controlling reverse battery flow and the battery management systems may be attempted.

4. Desiging SCC topologies with capacitor voltage sharing to gain maximum voltage ratios in SIDO, DISO, DIDO topologies may be worth researching.

Appendix A

Fibonacci SCC

A.1 Digital controller code for generating pulse for bidirectional switches using PSIM C block.

```
unsigned char a=0;
unsigned char b=0;
unsigned char c=0;
static unsigned char count=0;
// *** Different Phases of Voltage ratios
// *** the Generated code {1 -1 0 -1}
const unsigned char Top1[] =
{
// *** S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
0,0,1,0,0,1,1,0,0,0,1,0};
// *** the code {0 1 0 -1}
const unsigned char Top2[] =
{
// *** S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
1,0,0,0,1,0,1,0,0,0,1,0};
// *** the code {0 0 1 1}
const unsigned char Top3[] =
{
//*** S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
```

```
1,1,0,0,0,0,0,0,0,1,1,0};
// *** the code {1 -1 -1 1}
const unsigned char Top4[] =
{
//*** S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
1,1,0,0,0,0,1,0,0,0,0,1};

b=in[0];

if(b!=a)
{
a=b;
count++;
if(count>12){count=1;}
switch(count)
{
case 1:
for(c=0;c<12;c++)
{
out[c]=Top1[c];
}
break;

case 2:
for(c=0;c<12;c++)
{
out[c]=Top2[c];
}
break;

case 3:
for(c=0;c<12;c++)
{
out[c]=Top3[c];
```

```
}
break;

case 4:
for(c=0;c<12;c++)
{
out[c]=Top4[c];
}
break;
}
}
```

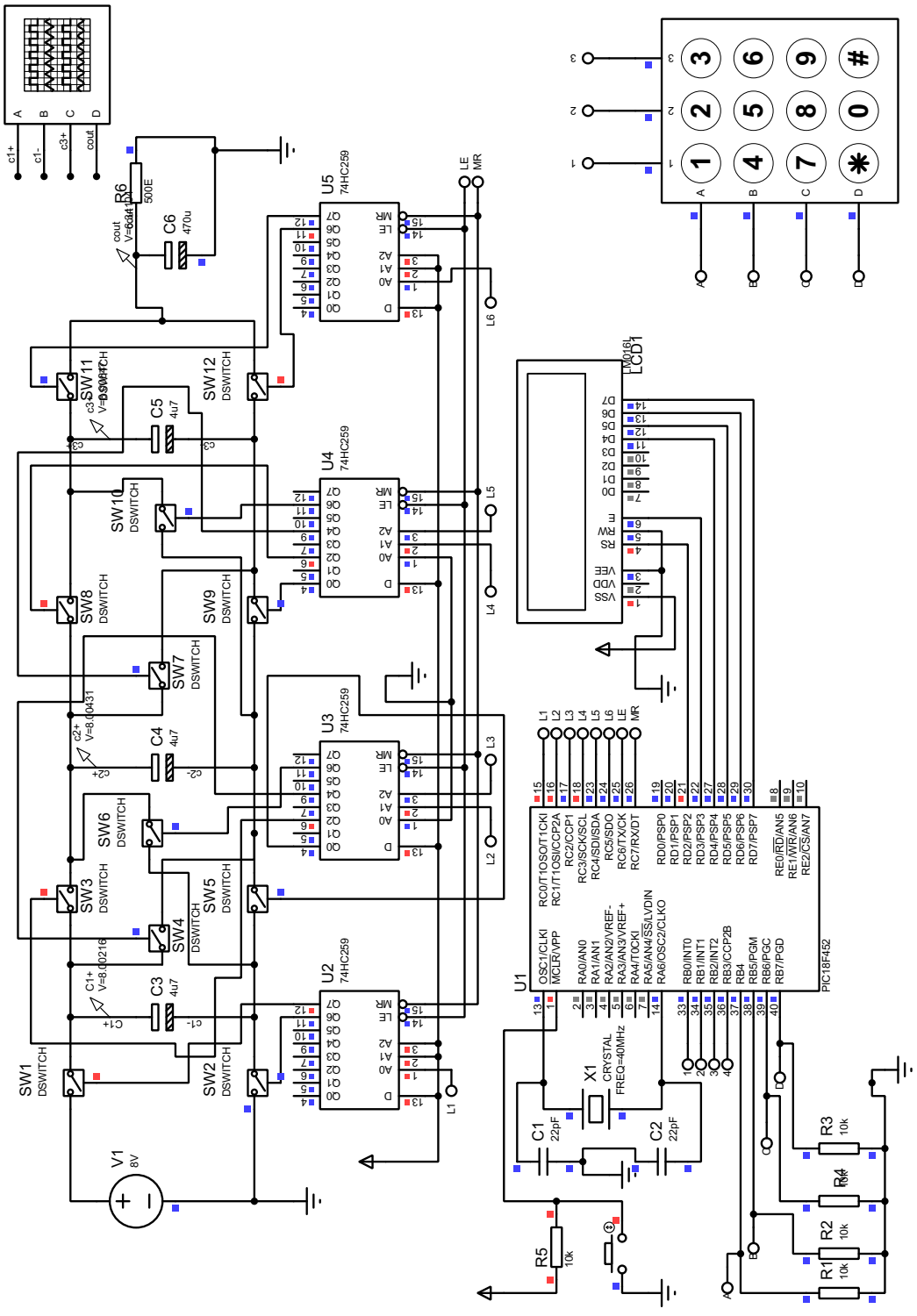


Figure A.1: Proteous model of Fibonacci SCC

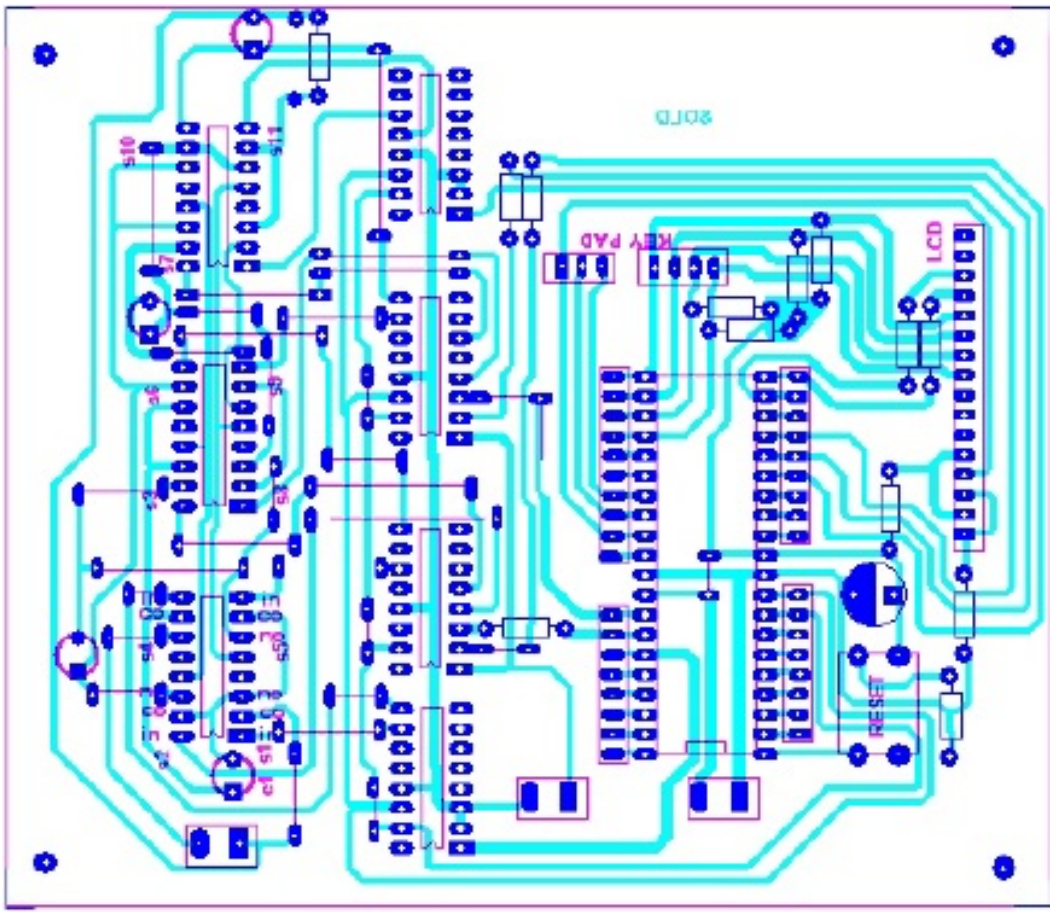


Figure A.2: Printed circuit board of Fibonacci SCC

Appendix B

DISO

B.1 Sample matlab code for R_{eq} calculation.

```
fs=100e3
C=22e-6;Co=220e-6;phc=0.5; pht=1;Vin=0.01;rload=1e3;
Ts=1/fs;
Tc=1/fs;
ron=35e-3;
esr=100e-3;
Rcs=(2*ron)+(esr);
Ccs=C;
Rts=(4*ron)+(esr);
Cts=(C*Co)/(C+Co);
lambda_c=Tc/(Rcs*Ccs)
lambda_t=Ts/(Rts*Cts)
Routc=((phc)^2)*(1/(2*fs*Ccs))*coth(lambda_c/2)
Routt=((pht)^2)*(1/(2*fs*Cts))*coth(lambda_t/2)
Rout=(Routc+Routt)
Rout1=(rload+Rout);
Iout=Vin/Rout1;
Vout=-(Iout*rload)
```

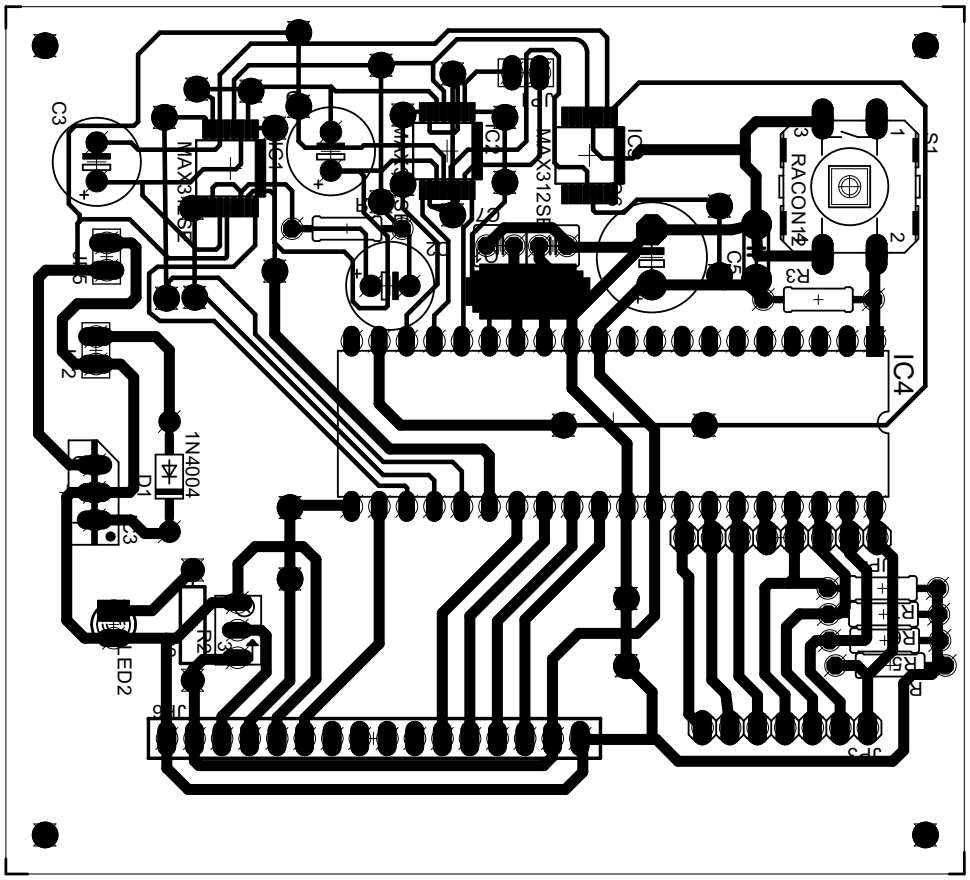


Figure B.1: Printed circuit board of DISO

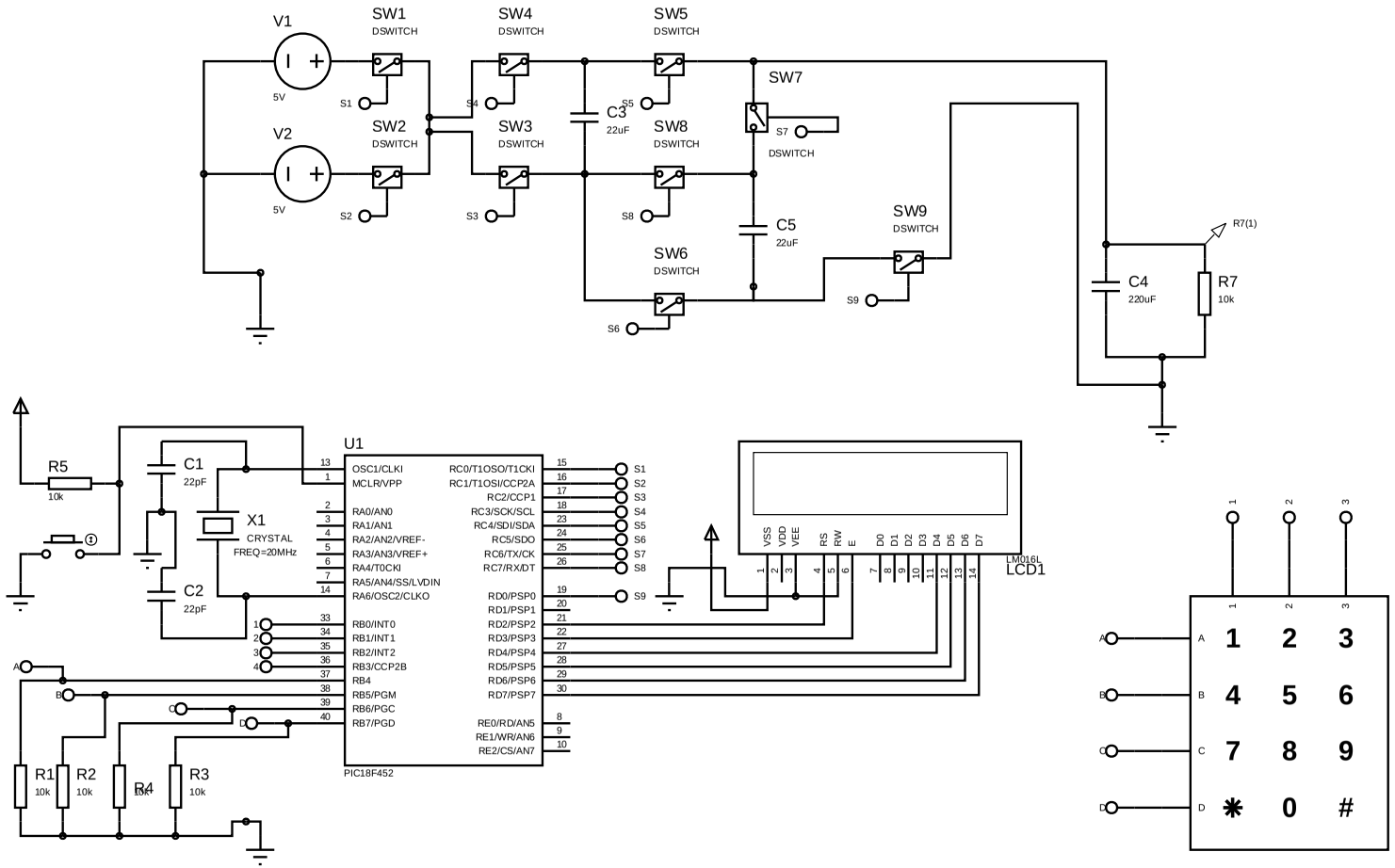


Figure B.2: Proteous model of DISO

Appendix C

DIDO

C.1 Matlab code for Decoupled case using R-Parameters

For the voltage ratio V_{o1} =($\frac{1}{3} * V_{s1}$)+and $V_{o2} = \frac{2}{3} * V_{s2}$ matlab code is discussed below.

```
clear
clc

syms V1120ph1 V1120ph4 a111 a112 a121 a122 a131 a132 a141 a142
V2120ph1 V2120ph4 a211  a212 a221 a222 a231 a232 a241 a242

r = 1;
C = 10*10^-6;
f = 5000;
T = 1/f;
V = 1;
ESR = 0;

% syms r ESR C

R1 = 3*r + 2*ESR;
R2 = 2*r + ESR;
R3 = r + ESR;
```

```
R4 = 2*r;
R5 = 2*r + ESR;
R6 = r + ESR;
R7 = 2*r;
R8 = 4*r + 2*ESR;
C1 = C;
C2 = C;
C12 = C/2;



T1 = R1*C12;
T6 = R8*C12;

V11coeff = ((1/R3)/(1/R2+1/R3+1/R4)-1)/(R3*C2);
V12coeff = (1/R2)/(1/R2+1/R3+1/R4)/(R3*C2);
V21coeff = (1/R3)/(1/R2+1/R3+1/R4)/(R2*C1);
V22coeff = ((1/R2)/(1/R2+1/R3+1/R4)-1)/(R2*C1);

A=[V11coeff V12coeff; V21coeff V22coeff];
[C,D]=eig(A);

T2=-1/D(1,1);
T3=-1/D(2,2);

V11coeff = ((1/R5)/(1/R6+1/R5+1/R7)-1)/(R5*C2);
V12coeff = (1/R6)/(1/R6+1/R5+1/R7)/(R5*C2);
V21coeff = (1/R5)/(1/R6+1/R5+1/R7)/(R6*C1);
V22coeff = ((1/R6)/(1/R6+1/R5+1/R7)-1)/(R6*C1);

A=[V11coeff V12coeff; V21coeff V22coeff];
[C,D]=eig(A);

T4=-1/D(1,1);
```

```
T5=-1/D(2,2);

V11C12 = @(t) -V+(V1120ph1+V)*exp(-t/T1);
V12C1 = @(t) V+a111*exp(-t/T2)+a112*exp(-t/T3);
V12C2 = @(t) V+a121*exp(-t/T2)+a122*exp(-t/T3);
V13C1 = @(t) a131*exp(-t/T4)+a132*exp(-t/T5);
V13C2 = @(t) a141*exp(-t/T4)+a142*exp(-t/T5);
V14C12 = @(t) V1120ph4*exp(-t/T6);

eqn1 = V11C12(T/4)==V12C1(0)+V12C2(0);
eqn2 = V12C1(T/4)==V13C1(0);
eqn3 = V12C2(T/4)==V13C2(0);
eqn4 = V13C1(T/4)+V13C2(T/4)==V14C12(0);
eqn5 = V14C12(T/4)==V11C12(0);
eqn6 = C2*V13C2(T/4)-C1*V13C1(T/4)==C2*V12C2(0)-C1*V12C1(0);
eqn7 = (R2*C1/T2-1)*a111==(R3*C2/T2-1)*a121;
eqn8 = (R2*C1/T3-1)*a112==(R3*C2/T3-1)*a122;
eqn9 = (1-R5*C2/T4)*a141==(1-R6*C1/T4)*a131;
eqn10 = (1-R5*C2/T5)*a142==(1-R6*C1/T5)*a132;



[A,B] = equationsToMatrix([eqn1, eqn2, eqn3, eqn4, eqn5, eqn6,
eqn7, eqn8, eqn9, eqn10],[V1120ph1, a111, a112, a121, a122, a131,
 a132, a141, a142, V1120ph4]);
X=linsolve(A,B);
V1120ph1 = double(X(1));
a111 = double(X(2));
a112 = double(X(3));
a121 = double(X(4));
a122 = double(X(5));
a131 = double(X(6));
a132 = double(X(7));
a141 = double(X(8));
```

```
a142 = double(X(9));
V1120ph4 = double(X(10));

I11 = -1/T*(C12*(V1120ph1+V)*(exp(-T/(4*T1))-1)-(C1*a111+C2*a121)
*(exp(-T/(4*T2))-1)-(C1*a112+C2*a122)*(exp(-T/(4*T3))-1));
I21 = -1/T*((C2*a141+C1*a131)*(exp(-T/(4*T4))-1)+(C2*a142+C1*a132)
*(exp(-T/(4*T5))-1)-C12*V1120ph4*(exp(-T/(4*T6))-1));
Y11 = I11/V;
Y21 = I21/V;



V21C12 = @(t) V2120ph1*exp(-t/T1);
V22C1 = @(t) a211*exp(-t/T2)+a212*exp(-t/T3);
V22C2 = @(t) a221*exp(-t/T2)+a222*exp(-t/T3);
V23C1 = @(t) -V+a231*exp(-t/T4)+a232*exp(-t/T5);
V23C2 = @(t) -V+a241*exp(-t/T4)+a242*exp(-t/T5);
V24C12 = @(t) V+(V2120ph4-V)*exp(-t/T6);

eqn1 = V21C12(T/4)==V22C1(0)+V22C2(0);
eqn2 = V22C1(T/4)==V23C1(0);
eqn3 = V22C2(T/4)==V23C2(0);
eqn4 = V23C1(T/4)+V23C2(T/4)==V24C12(0);
eqn5 = V24C12(T/4)==V21C12(0);
eqn6 = C2*V23C2(T/4)-C1*V23C1(T/4)==C2*V22C2(0)-C1*V22C1(0);
eqn7 = (R2*C1/T2-1)*a211==(R3*C2/T2-1)*a221;
eqn8 = (R2*C1/T3-1)*a212==(R3*C2/T3-1)*a222;
eqn9 = (1-R5*C2/T4)*a241==(1-R6*C1/T4)*a231;
eqn10 = (1-R5*C2/T5)*a242==(1-R6*C1/T5)*a232;



[A,B] = equationsToMatrix([eqn1, eqn2, eqn3, eqn4, eqn5, eqn6,
eqn7, eqn8, eqn9, eqn10],[V2120ph1, a211, a212, a221, a222,
```

```
a231, a232, a241, a242, V2120ph4]);
X=linsolve(A,B);
V2120ph1 = double(X(1));
a211 = double(X(2));
a212 = double(X(3));
a221 = double(X(4));
a222 = double(X(5));
a231 = double(X(6));
a232 = double(X(7));
a241 = double(X(8));
a242 = double(X(9));
V2120ph4 = double(X(10));

I12 = -1/T*(C12*V2120ph1*(exp(-T/(4*T1))-1)-(C1*a211+C2*a221)*
(exp(-T/(4*T2))-1)-(C1*a212+C2*a222)*(exp(-T/(4*T3))-1));
I22 = -1/T*((C2*a241+C1*a231)*(exp(-T/(4*T4))-1)+(C2*a242+C1*a232)*
(exp(-T/(4*T5))-1)-C12*(V2120ph4-V)*(exp(-T/(4*T6))-1));
Y12 = I12/V;
Y22 = I22/V;

Y = [Y11 Y12; Y21 Y22]
R = inv(Y)
```

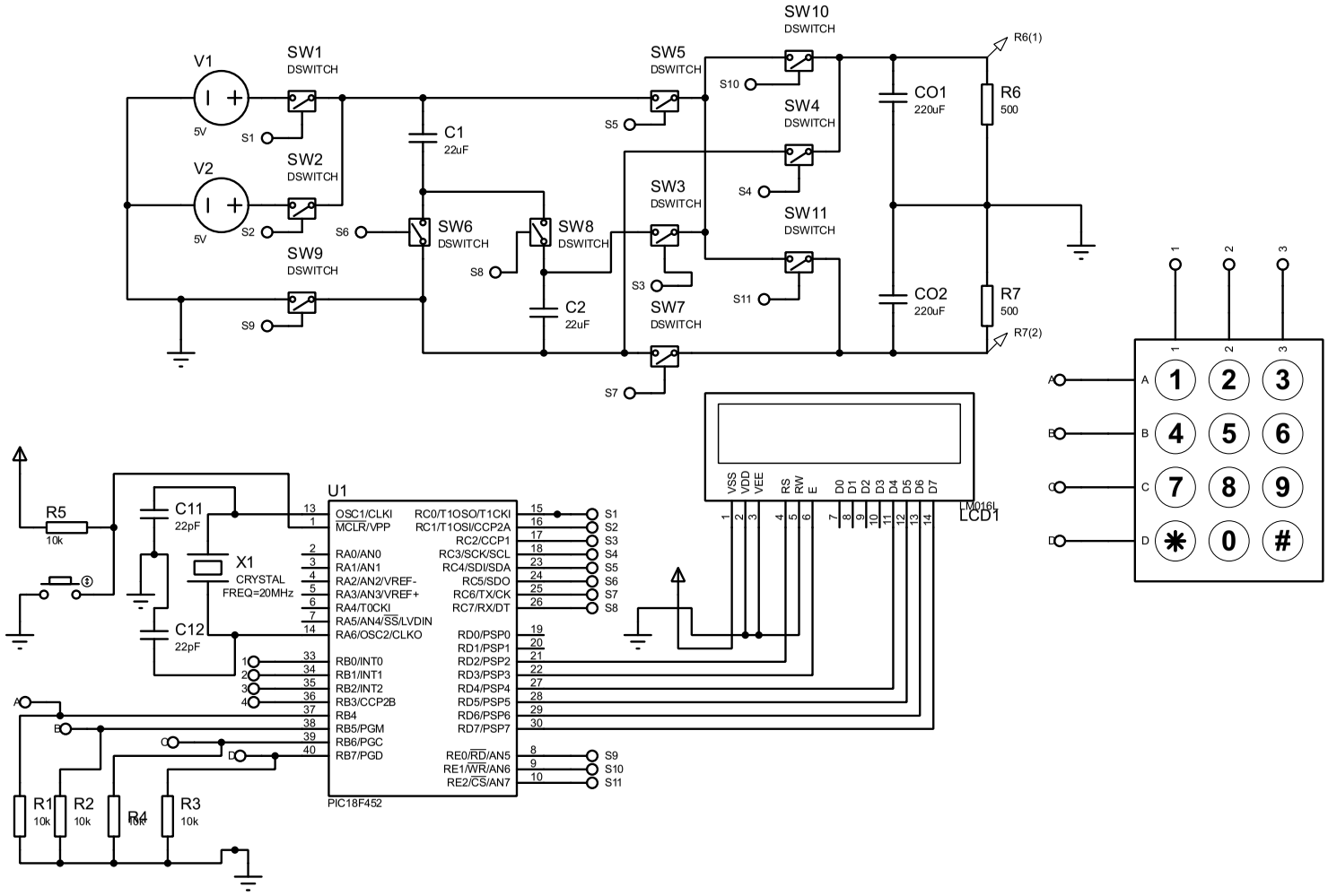


Figure C.1: Proteous model of DIDO

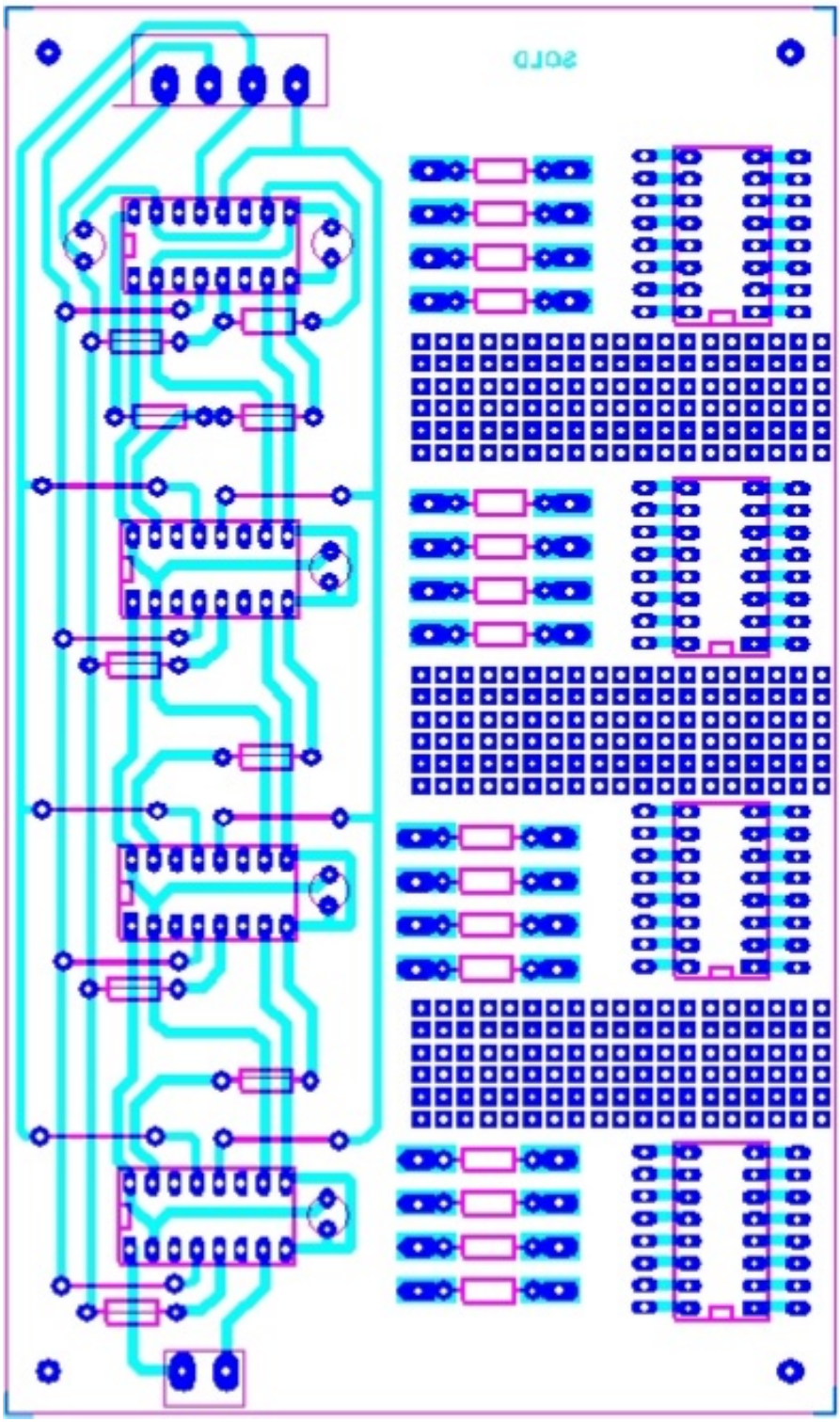


Figure C.2: Printed circuit board of DIDO (multi purpose)

C.2 Matlab code for coupled case using R-Paramters.

For the voltage ratio V_{o1} =$(2*V_{s1})$+$(2*V_{s2})$ and $V_{o2} = 2*V_{s1}$ matlab code is discussed below.

```
clear
clc

syms r C
r = 0.4;
C = 15*10^-6;
f = 10000;
T = 1/f;
V = 1;
ESR = 0;

R1 = 2*r;
R2 = 2*r + ESR;
R3 = r + ESR;
R4 = 4*r + 2*ESR;
R5 = 2*r;
R6 = 2*r + ESR;
R7 = r + ESR;
R8 = 4*r + 2*ESR;

C1 = C;
C2 = C;
C12 = C/2;

V11coeff = ((1/R2)/(1/R3+1/R2+1/R1)-1)/(R2*C2);
V12coeff = (1/R3)/(1/R3+1/R2+1/R1)/(R2*C2);
V21coeff = (1/R2)/(1/R3+1/R2+1/R1)/(R3*C1);
V22coeff = ((1/R3)/(1/R3+1/R2+1/R1)-1)/(R3*C1);

A=[V11coeff V12coeff; V21coeff V22coeff];
```

```
[C,D]=eig(A);

T1=-1/D(1,1);
T2=-1/D(2,2);

T3 = R4*C12;

V11coeff = ((1/R6)/(1/R7+1/R6+1/R5)-1)/(R6*C2);
V12coeff = (1/R7)/(1/R7+1/R6+1/R5)/(R6*C2);
V21coeff = (1/R6)/(1/R7+1/R6+1/R5)/(R7*C1);
V22coeff = ((1/R7)/(1/R7+1/R6+1/R5)-1)/(R7*C1);

A=[V11coeff V12coeff; V21coeff V22coeff];
[C,D]=eig(A);

T4=-1/D(1,1);
T5=-1/D(2,2);

T6 = R8*C12;

syms a111 a112 a121 a122 V12C120 a131 a132 a141 a142 V14C120
syms a211 a212 a221 a222 V22C120 a231 a232 a241 a242 V24C120

%V is applied at Load 1
V11C1 = @(t) a111*exp(-t/T1)+a112*exp(-t/T2);
V11C2 = @(t) a121*exp(-t/T1)+a122*exp(-t/T2);
V12C12 = @(t) V+(V12C120-V)*exp(-t/T3);
V13C1 = @(t) a131*exp(-t/T4)+a132*exp(-t/T5);
V13C2 = @(t) a141*exp(-t/T4)+a142*exp(-t/T5);
V14C12 = @(t) -V+(V14C120+V)*exp(-t/T6);


eqn1 = V11C1(T/4)+V11C2(T/4) == V12C12(0);
eqn2 = V12C12(T/4) == V13C1(0)+V13C2(0);
```

```
eqn3 = V13C1(T/4)+V13C2(T/4) == V14C12(0);
eqn4 = V14C12(T/4) == V11C1(0)+V11C2(0);
eqn5 = C2*V11C2(T/4)-C1*V11C1(T/4) == C2*V13C2(0)-C1*V13C1(0);
eqn6 = C2*V13C2(T/4)-C1*V13C1(T/4) == C2*V11C2(0)-C1*V11C1(0);
eqn7 = (1-R2*C2/T1)*a121 == (1-R3*C1/T1)*a111;
eqn8 = (1-R2*C2/T2)*a122 == (1-R3*C1/T2)*a112;
eqn9 = (1-R6*C2/T4)*a141 == (1-R7*C1/T4)*a131;
eqn10 = (1-R6*C2/T5)*a142 == (1-R7*C1/T5)*a132;

[A,B] = equationsToMatrix([eqn1, eqn2, eqn3, eqn4, eqn5, eqn6,
 eqn7, eqn8, eqn9,  eqn10],[a111, a112, a121, a122, V12C120,
 a131, a132, a141, a142, V14C120]);
X=linsolve(A,B);
a111 = double(X(1));
a112 = double(X(2));
a121 = double(X(3));
a122 = double(X(4));
V12C120 = double(X(5));
a131 = double(X(6));
a132 = double(X(7));
a141 = double(X(8));
a142 = double(X(9));
V14C120 = double(X(10));

syms t
i13 = C12*(V12C120-V)*exp(-t/T3)/T3;
i16 = C12*(V14C120+V)*exp(-t/T6)/T6;

I11 = 1/T*(int(i16,t,0,T/4)-int(i13,t,0,T/4));
I21 = -1/T*int(i16,t,0,T/4);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%V is applied at Load 2
V21C1 = @(t) a211*exp(-t/T1)+a212*exp(-t/T2);
```

```
V21C2 = @(t) a221*exp(-t/T1)+a222*exp(-t/T2);
V22C12 = @(t) V22C120*exp(-t/T3);
V23C1 = @(t) a231*exp(-t/T4)+a232*exp(-t/T5);
V23C2 = @(t) a241*exp(-t/T4)+a242*exp(-t/T5);
V24C12 = @(t) V+(V24C120-V)*exp(-t/T6);


eqn1 = V21C1(T/4)+V21C2(T/4) == V22C12(0);
eqn2 = V22C12(T/4) == V23C1(0)+V23C2(0);
eqn3 = V23C1(T/4)+V23C2(T/4) == V24C12(0);
eqn4 = V24C12(T/4) == V21C1(0)+V21C2(0);
eqn5 = C2*V21C2(T/4)-C1*V21C1(T/4) == C2*V23C2(0)-C1*V23C1(0);
eqn6 = C2*V23C2(T/4)-C1*V23C1(T/4) == C2*V21C2(0)-C1*V21C1(0);
eqn7 = (1-R2*C2/T1)*a221 == (1-R3*C1/T1)*a211;
eqn8 = (1-R2*C2/T2)*a222 == (1-R3*C1/T2)*a212;
eqn9 = (1-R6*C2/T4)*a241 == (1-R7*C1/T4)*a231;
eqn10 = (1-R6*C2/T5)*a242 == (1-R7*C1/T5)*a232;

[A,B] = equationsToMatrix([eqn1, eqn2, eqn3, eqn4, eqn5, eqn6,
eqn7, eqn8, eqn9,  eqn10],[a211, a212, a221, a222, V22C120, a231,
a232, a241, a242, V24C120]);
X=linsolve(A,B);
a211 = double(X(1));
a212 = double(X(2));
a221 = double(X(3));
a222 = double(X(4));
V22C120 = double(X(5));
a231 = double(X(6));
a232 = double(X(7));
a241 = double(X(8));
a242 = double(X(9));
V24C120 = double(X(10));
```

```
i23 = C12*V22C120*exp(-t/T3)/T3;
i26 = C12*(V24C120-V)*exp(-t/T6)/T6;

I12 = 1/T*(int(i26,t,0,T/4)-int(i23,t,0,T/4));
I22 = -1/T*int(i26,t,0,T/4);

Y11 = I11/V;
Y21 = I21/V;
Y12 = I12/V;
Y22 = I22/V;



Y = [Y11 Y12; Y21 Y22];
R = inv(Y);

double(Y)
double(R)
%------------------------------End-------------------------%
```

Appendix D

ISCC

D.1 Generalised code to validate R_{eq} value for two phase SCC configuration.

```
>> f = 100000;
>> esr = 0.1;
>> R1 = 0.3+esr;
>> R2 = 3*0.3+esr;
>> R3 = 0.3;
>> C1 = 22*10^-6;
>> C2 = 22*10^-6;
>> V11coeff = ((1/R2)/(1/R1+1/R2+1/R3)-1)/(R2*C2);
V12coeff = (1/R1)/(1/R1+1/R2+1/R3)/(R2*C2);
V21coeff = (1/R2)/(1/R1+1/R2+1/R3)/(R1*C1);
V22coeff = ((1/R1)/(1/R1+1/R2+1/R3)-1)/(R1*C1);

A=[V11coeff V12coeff; V21coeff V22coeff];
[C,D]=eig(A);

T1=-1/D(1,1)
T2=-1/D(2,2)
```

```
>> K = [2*T1*(1-exp(-1/(2*f*T1))) 2*T2*(1-exp(-1/(2*f*T2)))
T1*(1-exp(-1/(2*f*T1)))  T2*(1-exp(-1/(2*f*T2)));
T1*(1-exp(-1/(2*f*T1))) T2*(1-exp(-1/(2*f*T2))) 0 0;
(R1-T1/C1) 0 -R3 0;
0 (R1-T2/C1) 0 -R3];
>> B = [0; -1/f; 0; 0];
>> a = inv(K)*B;
>> a11 = a(1);
>> a12=a(2);
>> a21=a(3);
>> a22=a(4);

>> sqi1 = @(t) a11^2*exp(-2*t/T1)+2*a11*a12*
exp(-t*(1/T1+1/T2))+a12^2*exp(-2*t/T2);
>> Req11 = R1*f*integral(sqi1,0,1/(2*f));
>> sqi2 = @(t) a21^2*exp(-2*t/T1)+2*a21*a22*
exp(-t*(1/T1+1/T2))+a22^2*exp(-2*t/T2);
>> Req12 = R3*f*integral(sqi2,0,1/(2*f));
>> sqi1plus2 = @(t) (a11+a21)^2*exp(-2*t/T1)+
2*(a11+a21)*(a12+a22)*exp(-t*(1/T1+1/T2))+(a12+a22)^2*exp(-2*t/T2);
>> Req13 = R2*f*integral(sqi1plus2,0,1/(2*f));

>> Rph2 = Req11+Req12+Req13;
>> r = 0.3;
>> C = 22*10^-6;
>> Rph1 = coth(3/(22*r*C*f))/(C*f);
>> Rtotal = Rph1+Rph2

b11 = a11*f*(1-exp(-1/(2*f*T1)));
b12 = a12*f*(1-exp(-1/(2*f*T2)));
b21 = a21*f*(1-exp(-1/(2*f*T1)));
b22 = a22*f*(1-exp(-1/(2*f*T2)));

C = 10^-5;
```

```
coeff1 = b11^2*C*R1*T1/2 + b21^2*C*R3*T1/2 + (b11+b21)^2*C*R2*T1/2;
invCoeff1 = 1/coeff1;

coeff2 = b12^2*C*R1*T2/2 + b22^2*C*R3*T2/2 + (b12+b22)^2*C*R2*T2/2;
invCoeff2 = 1/coeff2;

r = 1;
Req_analytic = coth(1/(6*r*C*f))/(C*f)+ coth(1/(6.3431*r*C*f))/
(6.8284*C*f)+ coth(1/(17.657*r*C*f))/(1.1716*C*f)
```

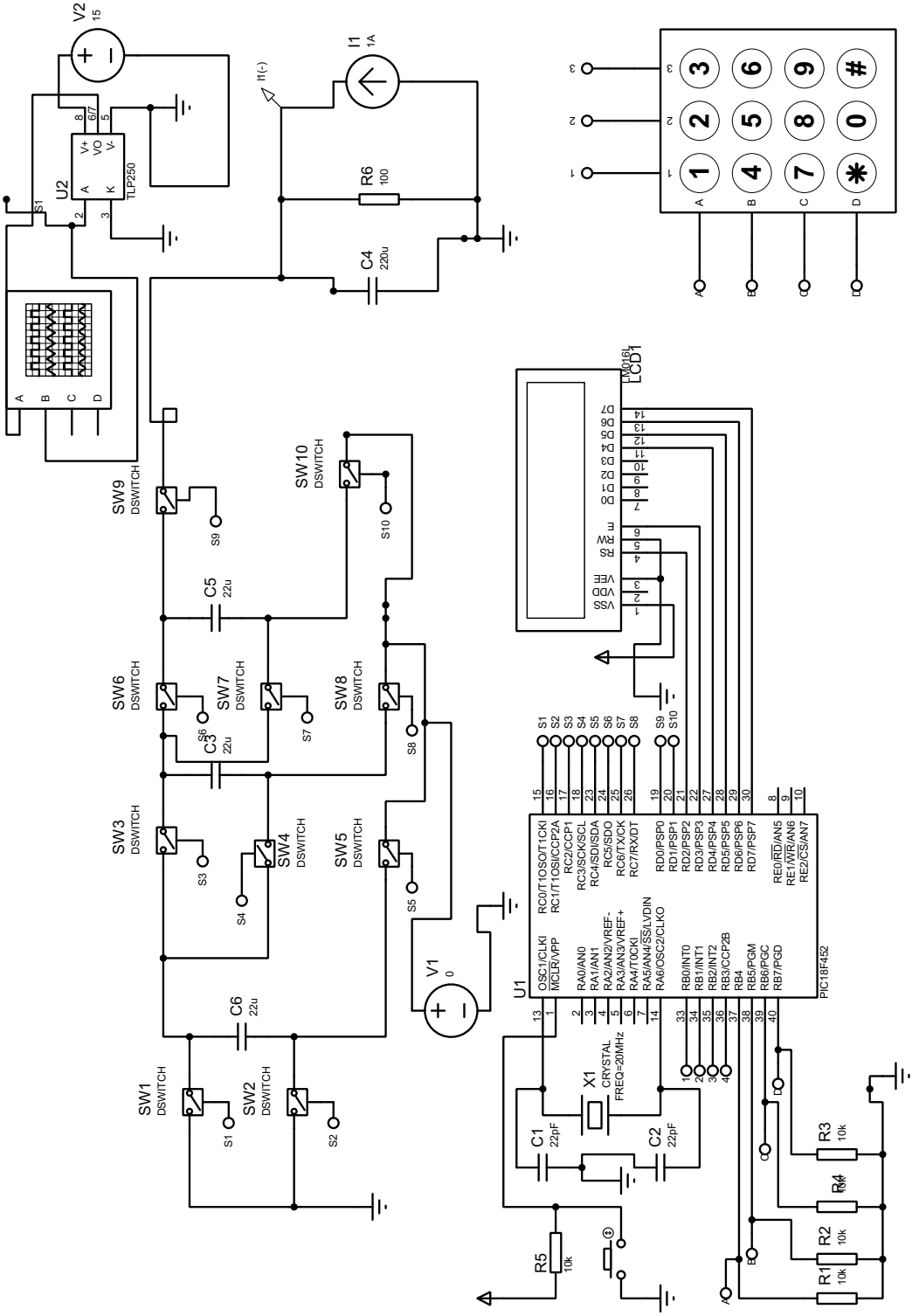
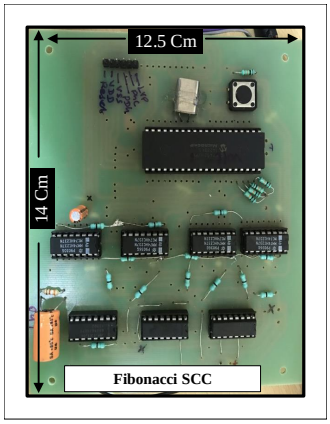


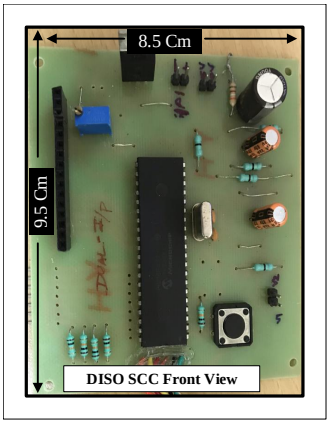
Figure D.1: Proteous model of ISCC

Appendix E

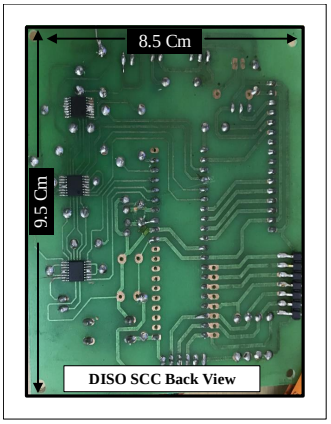
Hardware board clicks



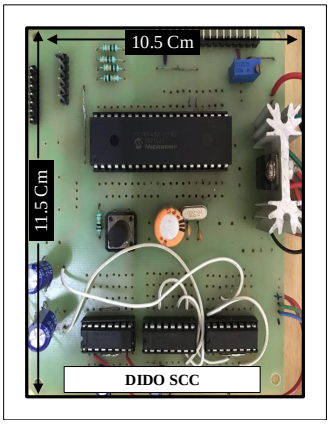
(a) Fibonacci SCC Prototype



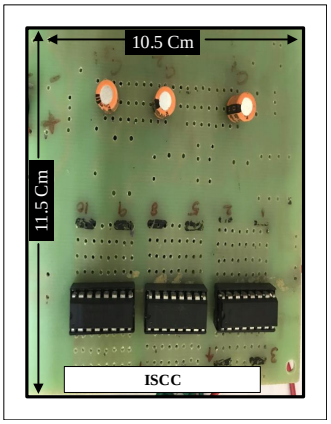
(b) DISO SCC Prototype front view



(c) DISO SCC Prototype back view



(d) DIDO SCC Prototype



(e) ISCC Prototype

Figure E.1: Hardware clicks of different SCC toplogies

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