DESIGN AND DEVELOPMENT OF HIGH STEP-UP AND STEP-DOWN VOLTAGE RATIO CONVERTERS FOR ELECTRIC VEHICLE APPLICATION

Thesis

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

by

A.O.L.TRIPURA SUNDARI

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING,
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA,
SURATHKAL, MANGALORE -575025

April, 2024

DECLARATION

by the Ph.D. Research Scholar

I hereby *declare* that the Research Thesis entitled "Design and Development of High Step-up and Step-down Voltage Ratio Converters for Electric Vehicle Application" which is being submitted to the National Institute of Technology Karnataka, Surathkal in partial fulfillment of the requirement for the award of the Degree of Doctor of Philosophy in Electrical and Electronics Engineering is a *bonafide report of the research work carried out by me*. The material contained in this Research Thesis has not been submitted to any University or Institution for the award of any degree.

22/4/24

.....

A.O.L.Tripura Sundari, 145093EE14P01R
Department of Electrical and Electronics Engineering

Place: NITK-Surathkal
Date: 22/4/2024

CERTIFICATE

This is to *certify* that the Research Thesis entitled "Design and Development of High Step-up and Step-down Voltage Ratio Converters for Electric Vehicle Application" submitted by A.O.L.Tripura Sundari (Register Number:145093 EE14P01R) as the record of the research work carried out by her, is *accepted as the Research Thesis submission* in partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

P. Parthiban 22/04/2024

Dr. P. Parthiban
(Research Guide)

22/04/2024

Dr. D. N. Gaonkar
(Chairman-DRPC, EEE Dept.)

PROFESSOR AND HEAD
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA
SRINIVASNAGAR, SURATHKAL, MANGALORE - 575 025, INDIA

Acknowledgements

It gives me immense pleasure and great sense of satisfaction to express my heartfelt gratitude to those who made this dissertation possible.

I would like to express my sincere gratitude to Associate Professor P Parthiban. for his guidance, unending support, encouragement, and for having been my Ph.D. supervisor. He has been a constant source of inspiration throughout this journey. I feel proud to have worked under his guidance.

I thank National Institute of Technology Karnataka (NITK) for giving me an opportunity for doing research.

I wish to thank my research progress assessment committee (RPAC) members Dr. Debashisha Jena and Dr. A. V. Narasimhadhan, for their constructive feedback and guidance. I would like to thank Dr. B Venkatesa Perumal for his thought-provoking ideas and suggestions during various interactions. I would like to thank Prof. G.S.Punekar, Prof. Panduranga Vittal K and Dr. Kalpana for their support and enouragement.

Thanks also goes to all the former HOD's for providing the necessary resources in the department to carry out my research. I would also like to thank HOD, Dr. D.N.Gaonkar for his support and encouragement.

I also thank all the research scholars of EE Dept for their continued support. Specially I thank Swapna, Vijay, Ramu, Vivekanandan, Kiran, Rajkumar, Krishnareddy, Santosh, Preeti, Pavana, Remya and also each and everyone, who made my stay convenient, comfortable and memorable . I also thank all the other teaching and non-teachinga staff for their support and help. I also thank Mahesh, Pranaya, Arjun, Praneeth and other U.G students who worked with me over the period of time.

I would like to express my deepest gratitude towards my mother Devasena, my guru Swami Brahmananda Saraswati, my husband Dr. Nithyananda Sastry and my son Srikara for their support, love, patience and encouragement which kept me going in this journey. I also thank my brother, sister, extended family and in-laws who encouraged me in my progress.

I thank the SGBIT management for encouraging me in my research work and permitting my absence and granting leave for 2.5 years which I used for completing course work and working with the hardware failities available at NITK.I thank all the faculty and staff of EEE Dept. who supported me during various stages of my tenure.

Finally, I thank God Almighty for giving me strength at all times.

Abstract

Transportation electrification helps to mitigate the effect of the emissions along with saving valuable foreign exchange. The development of Electric Vehicle(EV) will bring in requirement of capacity expansion of the existing system. The need for clean and efficient energy can be achieved through the migration to charging schemes based on photovoltaic sources or other renewable energy systems.

Study of the nature of charging characteristics of the battery with the nature of the Photovoltaic(PV) based source profile will give an estimation of the charging time and help in the design. Using the National Solar Radiation Database(NSRDB) data viewer, the irradiance, temperature profile of a 200 W panel was studied and presented. The observations reveal that the PV source can be used to charge the EV effectively for 8 months of the year. With the change in irradiance and temperature, maximum power point varies and the terminal voltage would vary around (22-26 V) for a 200 W system. To charge a battery of 48 V, the conventional converters need to be operated at a very high duty cycle. This results in higher device ratings and lower switching frequency due to the inherent switch limitations on the turn-on/turn-off times. A high gain step-up converter is explored to address this issue.

Investigations of available topologies of high gain converters in the literature reveals converters were designed with gain over 8 times for high voltage and low current appliations. The study of such converters for the medium voltage and current applications is not reported. In the present thesis, a modified boost converter was presented which yields a moderately higher voltage gain than that of the conventional boost converter. Simulation studies on the converters are done using MATLAB/Simulink. Hardware prototype models of conventional and modified boost converter were rigged up and tested.

The sun shines for more than 300 days in many parts of the country. The irradiance and temperature vary with time of the day and seasons which

limit the extraction of maximim power. Prototype model of a compact tracker using Particle Swarm Optimization(PSO) algorithm was developed and tested to extract the maximum power from the PV Source.

To mitigate the effect of the varying irradiance and provide alternate charging schemes, conventional grid support would be required. To charge these EV batteries from the grid, AC-DC chargers are required, which meet the IEC 61000-3-2 standards. Conventional bridge rectifiers need Power Factor Correction (PFC) due to their poor power quality apart from drawing peaky currents from the input side. Conventional bridge rectifiers have over 55% Total Harmonic Distortion (THD) and a poor power factor. The absence of PFC would result in poor efficiency, higher current pulses being drawn at the source side, higher peak ratings of the devices, and hence increased losses. Converters need to operate at an extremely low duty cycle in applications that require a low output from higher input. Due to the limitation of the turn-on / turn-off of the devices, switching frequency needs to be reduced, and hence the size of the inductors and capacitors become bulkier. Conventional active power factor correction topologies employ boost-based correction schemes for unity power factor operation. This will require a still steeper step-down ratio and higher switch voltage stress apart from complexity in the control scheme with sensors.

In this thesis, a high step-down ratio AC-DC converter employing a Quadratic Buck Converter(QBC) with PFC was designed and developed. The proposed topology presents an investigation and comparative evaluation of the conventional bridgeless buck system with the QBC. MATLAB R2020b is used for carrying out simulation studies. Xilinx FPGA-based controller using system generator is implemented for the generation of pulses of appropriate duty cycle. Simulation and experimental results for a 150 W prototype are presented.

Contents

List of Figures

List of Tables

List of Abbrevations

AC	Alternating Current
DC	Direct Current
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal-Oxide Semicondutor Field Effect Transistor
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion
P&O	Perturb and Observe
PSO	Particle Swarm Optimization
EV	Electric Vehicle
PV	Photovoltaic
PFC	Power Factor Correction
SOC	State of Charge
MPPT	Maximum Power Point Tracking
GHI	Global Horizontal Irradiance
DNI	Direct Normal Irradiance
STP	Standard Temperature and Pressure
NTP	Normal Temperature and Pressure
QBC	Quadratic Buck Converter
FPGA	Field Programmable Gate Array
DSO	Digital Storage Oscilloscope
PID	Proportional Integral and Derivative
ESR	Equivalent Series Resistance
NREL	The National Renewable Energy Laboratory
NSRDB	The National Solar Radiation Database
SS	Single Stage
SR	Series Resonant
CC	Constant Current
CV	Constant Voltage
CP	Constant Power
SOC	State of Charge
NEMMP	National Electric Mobility Mission Plan

FAME	Faster Adoption and Manufacturing of EV in India
BEE	Bureau of Energy Efficiency

Chapter 1

Introduction

Contents

1.1 Research Background

The number of vehicles for private transport is increasing in India with the number of two-wheelers exceeding 169 million in 2016 alone and growing at a rate of 20% each year. This increase has lead to the requirement of valuable foreign exchange in the form of import of oils and also health risks due to emissions in the form of CO, CO_2, and NO_2. The increased demand for conventional energy sources, rising pollution and related health issues, vehicular emissions causing global warming, melting ice across arctic's and rising oceans are the driving forces for the development of Electric Vehicles (EV) and alternate fuel technologies. More than fifty percent of the world's oil resources are consumed by the transportation sector. Government of

India's "National mission on electric mobility" sets a deployment target of 6 to 7 million EV and hybrid EV's by 2020.(NEMMP, 2013). The primary objective was to cut down the costs of oil imports and also meet global emission standards. The targets were not fully met due to numerous challenges including COVID 19, unavailability of electronic components required for EV inductry, poor charging infrastructure and higher costs.

Subsequently in June 2021, to promote growth of EV, Faster Adoption and Manufacturing of EV in India (FAME-II) scheme was ammended and launched, which aims to encourage battery manufacturers, commercial EVs including buses, threewheelers and passenger four wheelers. As per the Bureau of Energy Efficiency (BEE), the number of EV's in the country in the year 2022, is 10,76,420, and the country has a total of 1,742 public charging stations . The Ministry of Heavy Industries has reported sanctioning of 2877 public EV charging stations in 68 cities (MRTH, 2022). The government's ambition is to have EV sales accounting for 30% of private cars, 70% for commercial vehicles and 80% for two- and three-wheelers by 2030. Effective charging infrastructure is required to promote the growth of EV's in the country. Range anxiety, higher initial cost and lack of adequate infrastructure support for charging of vehicles are the issues effecting the adoption of EV's. The already overburdened existing power transmission network will not be able to cater to this huge demand enhanced by the additional burden of EVs imposed on the power system as envisaged, and hence alternate sources to charge EVs need to be explored. Photovoltaic(PV) based systems can offer a viable alternative solution.

1.1.1 Photovoltaic Source

A Solar PV Panel can be represented as a current source in parallel with a diode. Shunt resistance (R_{sh}) is very high and series resistance (R_s) is very low. The P-V and I-V curves are highly dependent on the irradiance and also inversely proportional to temperature. An extensive study on the representation of PV Panel with its single diode model was carried out in (Villalva et al., 2009). V-I characteristics of a panel depend on the PV cells which are connected in series, parallel combination (Ns, Np), Series and parallel resistances (Rs, Rp), Latitude of the area and the angle of inclination. The maximum power that could be obtained from a PV Panel continuously varies throughout the day with a change in irradiation and temperature.

A number of MPP topologies were developed, evaluated and implemented in literature. Perturb and Observe (P&O), Incremental Conductance, Direct Measurement (Open Circuit Voltage, Short Circuit Current), Lookup table, Parasitic Capacitance, Constant Voltage (CV), Constant Current (CC), Constant Power (CP), Fuzzy are some of the algorithms reported in the literature. P&O algorithm is best suited for rapidly varying irradiance conditions and has an ease of implementation due to the minimum number of sensors required. But conventional P&O also results in oscillations around the mean position. Modified P&O algorithms with estimated step size, adaptive P&O, and others are proposed to avoid the drift(Femia et al., 2005),(Esram and Chapman, 2007),(Safari and Mekhilef, 2010),(Altas and Sharaf, 2008). P &O was able to track the MPP, but when solar cells have partially shaded, the algorithm couldn't track the MPP as there were multiple peaks, and the algorithm was stuck among any one of the peaks. Hence Particle Swarm Optimization(PSO) algorithm was used to be much more efficient in tracking single and multiple peaks faster and accurately. The PSO algorithm contains search elements that search for the local optimum solution and exchange their status and data with other existing search elements, and finally, all the search elements converge at the global optimum solution. In this model, there is a need to find the duty at which the converter should operate, which in turn extracts the maximum power from the panel and delivers the same to load (Koad et al., 2016),(Rezk et al., 2017).

In the establishment of charging infrastructure, the efficient utilization of PV as a primary source needs to be further explored. As PV in intermittent, grid support might be required to ensure charging when PV source is unavailable during nights and rainy seasons. The maximum power that could be obtained from a PV source continuously varies throughout the day with a change in irradiation and temperature.

The National Renewable Energy Laboratory (NREL) has made a detailed repository of temperature, irradiance, pressure, etc. data which can be used for the designing of the PV systems. Data for the irradiance for the city of Mangalore was downloaded from NREL, The National Solar Radiation Database (NSRDB) data viewer and 3 years' data 2012-14 was collected analyzed. The representative variation for the year 2013 was plotted as in Figure1.1. From the data it was observed that the PV Panels can be used to charge EV battery from morning 8.30 AM when the irradiance exceeds $400W/m^2$ till evening 5.30 PM, when the

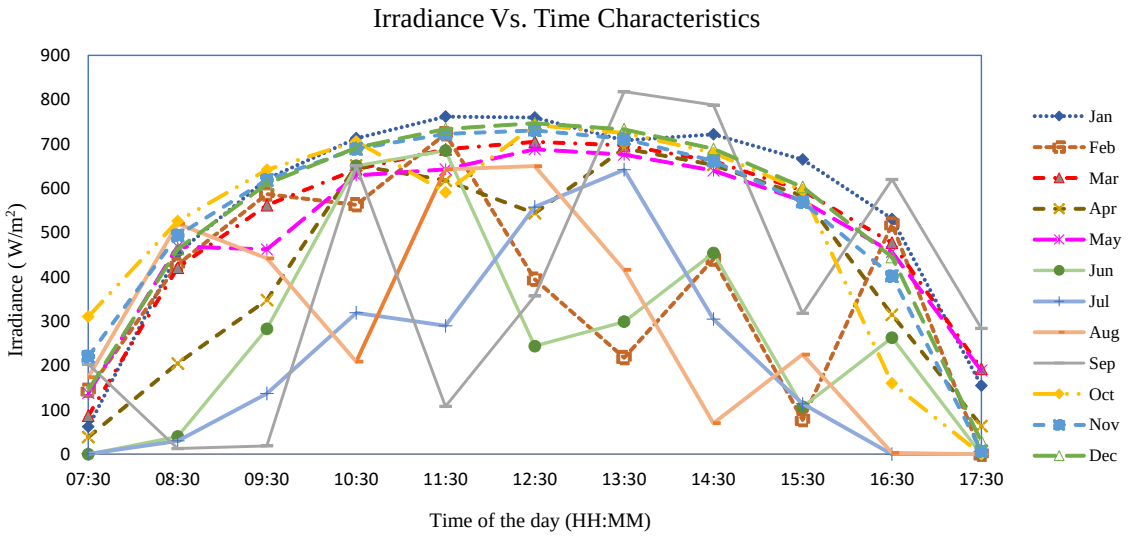


Figure 1.1: Irradiance characteristics throughout the year

irradiance falls below the same for almost 8 months of the year as shown.

The Global Horizontal Irradiance (GHI) for each month of the year was obtained. Estimation of energy output was computed & plotted for the PV panels with 100 W, 150 W, 200 W, 250 W. From the Figure 1.2, it was found that a 200 W panel can charge 80% of the battery for over 8 months of the year except for the months of June to September where the irradiance falls below the average due to the rainy season.

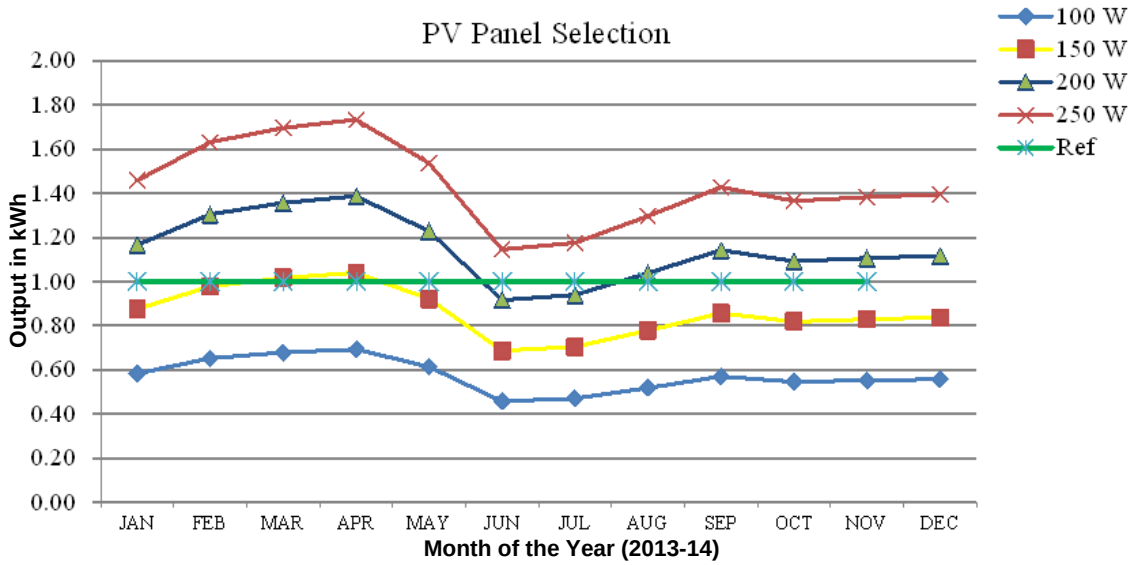


Figure 1.2: Estimation of PV panel wattage from NREL data

Table 1.1: Specifications of PV Panel (Waaree 200 W)

Power	200 W
V_{OC}	32 V
I_{SC}	8.7 A
V_{MPP}	26 V
I_{MPP}	7.7 A
R_{SH}	42.5 Ω
R_{SE}	0.2608 Ω

From the MATLAB model & the data obtained from NREL, a PV panel of 200 W (Waree make) with the specifications as in Table 1.1 was selected for further studies. By varying temperature, the characteristics of voltage, current and power at MPP were evaluated and plotted as in Figure 1.3. The study indicates that with a rise in temperature, I_{SC} increases, V_{OC} reduces, power output and efficiency of the panel reduces. For a 200 W panel at 25° C temperature MPP voltage is around 26 V and at 40° C it reduces to 24 V. From the NREL data, the normal room temperature in the city of Mangalore is found to be around 33° C and PV panel temperature is considered to have 10° C higher temperature than the room. For lower irradiance, the V_{MPP} further reduces. Thus the voltage at MPP point lies at 21 V at $400W/m^2$ irradiance to 26 V for $800W/m^2$ at the Normal Temperature and Pressure(NTP).

The characteristics of the PV Panel, with varying insolation levels from $500W/m^2$ to $800W/m^2$ are also observed as in Figure 1.4 through simulation studies. Variation in open circuit voltage V_{OC} is not much observed but the short circuit I_{SC} and the I_{MPP} vary widely from 4 A to 7 A. The studies show that variation in temperature has more effect on the V_{MPP} of the PV panel and the variation in irradiance has more effect on the I_{MPP} of the panel. Higher is the irradiance, greater is the power output of the PV panel and also higher is the current.

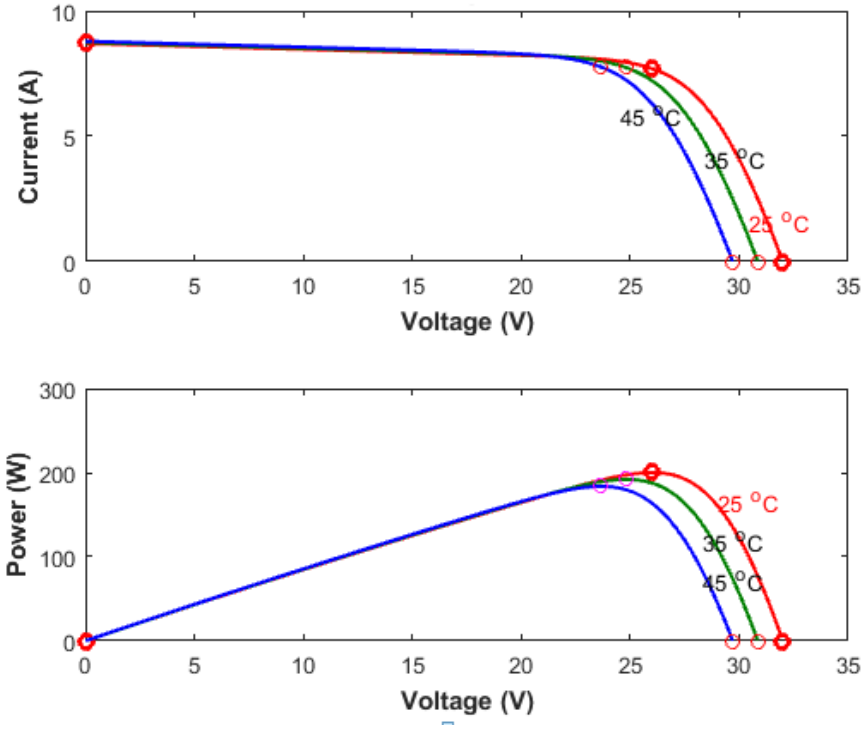


Figure 1.3: Variation of MPP Current and Voltage with Temperature

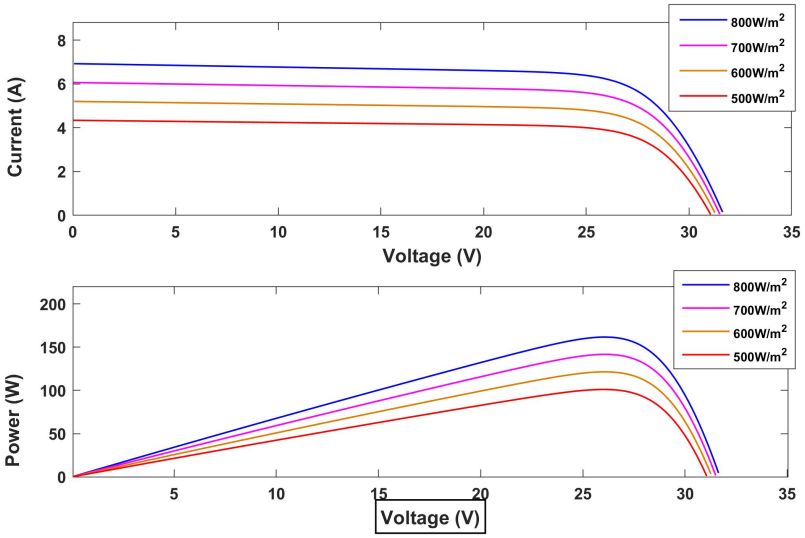


Figure 1.4: Study of PV Panel Characteristics with Irradiance Variation

1.1.2 Battery Load

A battery is a combination of two or more units of electro chemical cells connected in series parallel combination. Batteries could be non-rechargeable or chargeable. Commonly used rechargeable batteries are made of Lead-Acid, Nickel Cadmium, Nickel Metal Hydride, Lithium-Ion, Lithium-Ion Polymer. etc. The characteristic traits which are used to evaluate various battery chemistries are energy density, modularity, affordability, wide operating temperature, safety, long life cycle and lower re-charge duration. Comparision of lead-acid and lithium-ion of EV batteries is presented in Table 1.2. The limitations of battery chemistry impose restrictions with respect to the charge & discharge restrictions, storage capacity, cost and life of the battery (Wang and Stuart, 2002). The battery can be modeled as an electrochemical model, Thevenin based electrical model and impedance based model. Large capacitor representing the battery capacity to store and release charge and smaller capacitor to represent surface capacitance in parallel, resistors representing different internal resistances of the battery are discussed in the literature as represented by the Figure 1.5 (Lam et al., 2011),(Einhorn et al., 2012). Multi stage CC charging, current decay charging, pulse charging are few charging strategies widely reported in the literature (Lukic and Emadi, 2008).

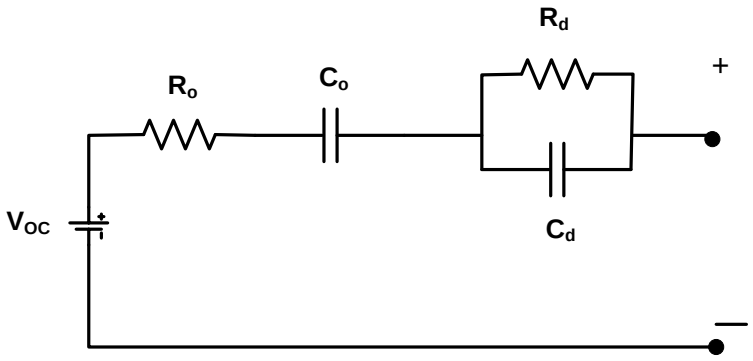


Figure 1.5: Battery Model

1.1.3 Lead-Acid Battery

The observations from lead-acid battery 48 V, 24 Ah during charging duration as plotted in Figure 1.6 reveal that the charge cycle follows 6 hours of CC, followed by 8 hours of CV operation. There is a Constant Power requirement of (80-100) W for the

first 6 hours and the requirement falls from 100 W to 20 W for the next cycle. The capacity addition is only 16 Ah though charged for more than 14 hours, but the cost of lead-acid battery is less than 50% of lithium-ion, and it also tolerates over voltages and suports prolonged charging. The charge cycle is cut off when the terminal voltage reaches 57 V and current falls to 200 mA. 4 modules, each rated at 12 V are required to be connected in series to make up 48 V. In order to achieve the cell balancing, connection pattern of these pack is changed during servicing.

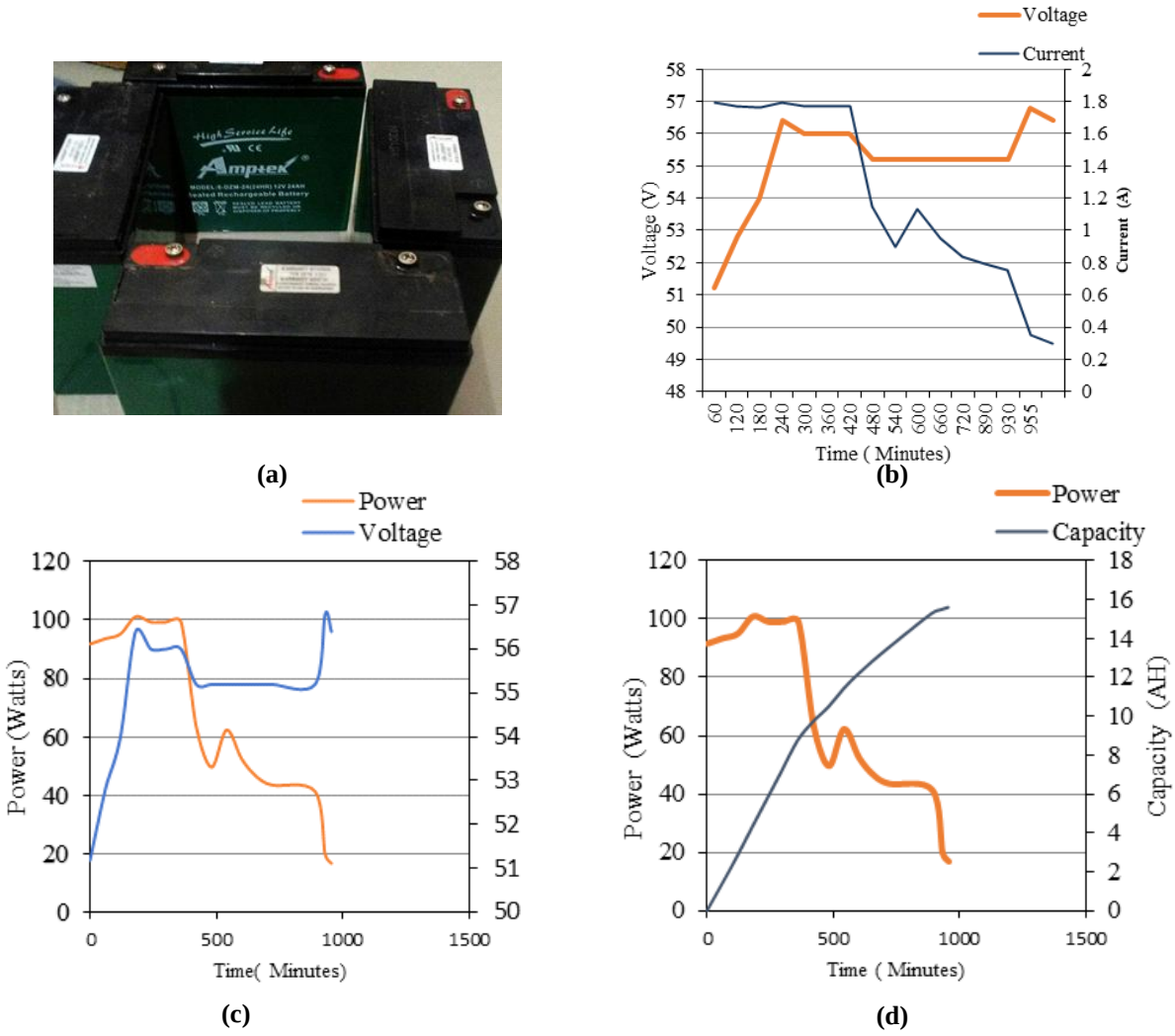


Figure 1.6: (a) 48 V, 24 Ah Lead-acid battery used for study (b) V-I characteristics during the charging process (c) Stored power with variation in terminal voltage(d) Power and capacity profile.

1.1.4 Lithium -Ion Battery

A good charging protocol considers the cell chemistry for appropriate design. Performance of Li-Ion cell was investigated using CC,CV,CP schemes. It was found

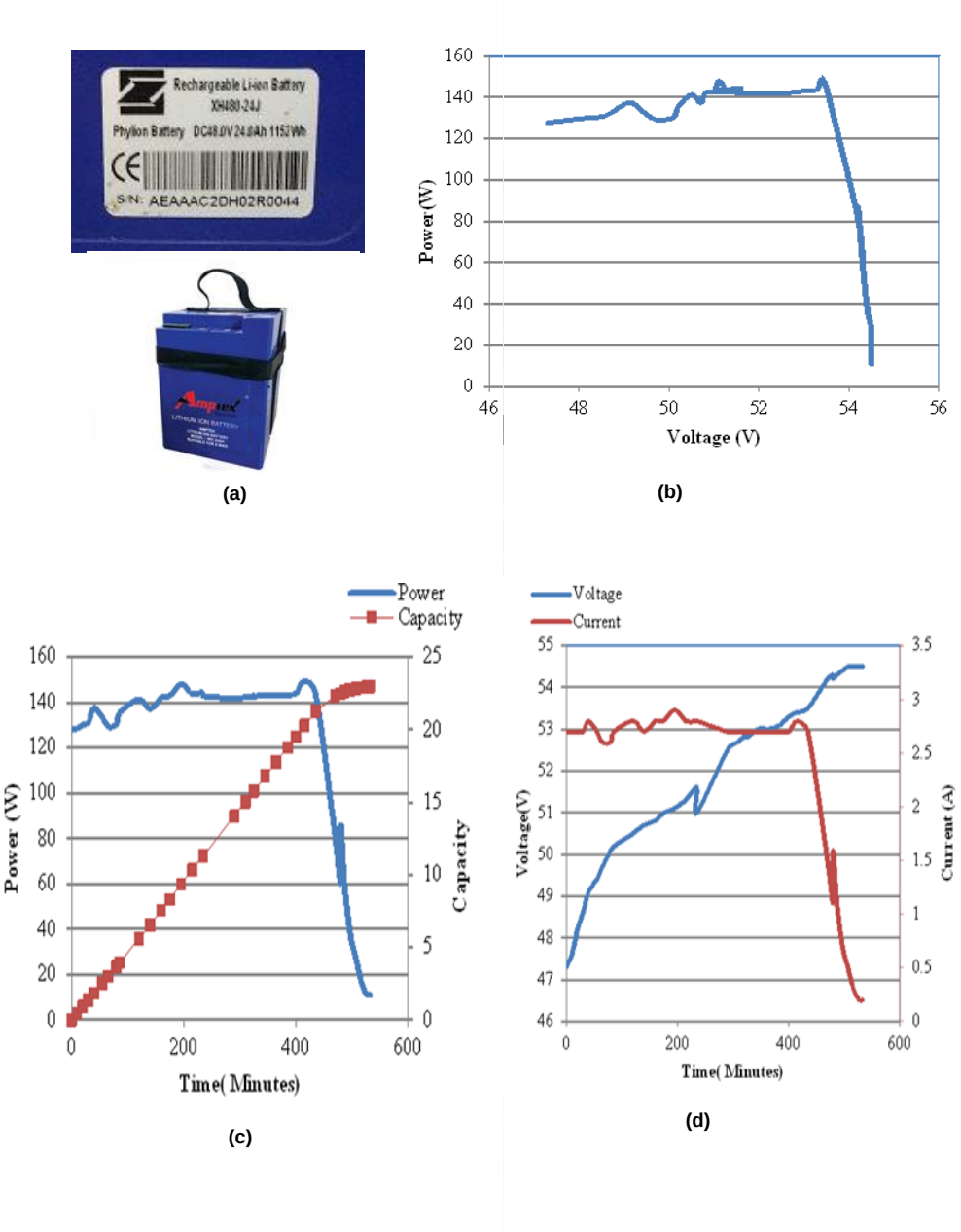


Figure 1.7: (a) 24 Ah, 48 V Lithium-Ion battery used for study(b) Variation of terminal voltage with power stored(during charging)(c) Power and capacity profile (d) V-I characteristics during charging process

Table 1.2: Comparision of Lead-Acid and Lithium-Ion Batteries

Characteristics /Type	Lead Acid	Lithium
Energy Density(per kg)	30 Wh	90 Wh
Charge / Discharge Cycles	700	3000
Nominal Cell Voltage	2 V	3.2 V
Working Voltage	1.75 to 2.6 V	2.5 to 3.65 V

that charging protocol strongly influences life cycle of a cell. Fast charging results in reduction in the storage capacity due to loss of Li^+ ions. Low State of Charge(SOC) battery with less than 0.1 C has high impedance. Hence it is desirable to apply low current initially and towards the end of charge cycle to avoid over-charge. After the battery current reaches zero, the open circuit voltage will drift for a certain time. The terminal voltage measured after this time lag is termed as SOCV. This SOCV is an excellent indicator of SOC for lead-acid and lithium-ion batteries(Zhang, 2006).

The study on Lead-Acid and Lithium-Ion battery (48 V, 24 Ah) characteristics which are conventionally used in two wheeler indicates that Lead-acid battery requires over 100 W in CC region for six hours and the requirement reduces for the next 8-10 hours in CV region. Lithium-ion battery needs 160 W for 7 hours in CC zone to charge 80% of the battery. There is a need to effectively extract power using an appropriate converter under these constraints. The time required for charging of Lead-acid battery is more, and it has the disadvantage of higher weight, lower energy density and lower number of charge-disharge cyles indicating lower lifetime. EV sector is dominated by Lithium-Ion batteries though the cost of Lithium-Ion battery is more than thrice, because of these disadvantages of lead-acid batteries. In stationary UPS or other back-up storage options, lead-acid batteries are preferred.

1.1.5 Converters

Power converter topologies in literature for battery charging could be broadly classified into DC-DC or AC-DC chargers. DC-DC converters can be broadly divided into unidirectional and bidirectional based on the direction of power flow. Unidirectional topologies reported in the literature can be primarily classified into single phase and three phase based on power requirement. These can be further subdivided into non-isolated and isolated topologies. Non-isolated topologies with single stage conversion such as quadratic and interleaved buck are reported for low

voltage and high current applications(Revathi and Prabhakar, 2016).

Buck, boost and buck-boost are the conventional topologies of converters used for multiple applications. These have low component count and simpler control(Zhao et al., 2015). Isolated topologies are being widely preferred due to safety and wider control range. Flyback, Forward, Push-Pull, Half-Bridge, Full-Bridge, Cuk and SEPIC converters are being widely researched.

Bidirectional topologies reported include half- bridge, full- bridge, multi-level and matrix converters. Bidirectional DC-DC converters have attracted a great deal of applications in the area of the energy storage systems for hybrid vehicles, renewable energy storage systems, UPS and fuel cell storage systems. Traditionally they were used for the motor drives for the speed control and regenerative braking. Bidirectional DC-DC converters are employed when the DC bus voltage regulation has to be achieved along with the power flow capability in both the direction. One such example is the power generation by wind or solar power systems, where there is a large fluctuation in the generated power because of the large variation and uncertainty of the energy supply to the conversion unit (wind turbines & PV panels) by the primary source. These systems cannot serve as a standalone system for power supply and requires support by backup rechargeable systems. Conventional battery chargers can produce harmonic effects which are harmful for the electric utility distribution systems. Chargers with active rectifier front end can mitigate this impact. Unidirectional charging limits hardware requirement, simplifies interconnection issues and tend to reduce battery degradation. Uncoordinated charging is the charging taking place immediately once the vehicle is connected. Uncoordinated charging can increase load at peak hours and can cause local distribution grid problems and can result in voltage deviations which affect the power quality. A model study in Netherlands indicates that the national peak load is increased by 7 % to 30%(Masoum et al., 2012). Unscheduled charging of EV's might exert an adverse effect on the existing power grid, especially when the charging coincides with daily peak load at distribution level. A scalable real-time scheduling scheme for EV charging in low-voltage residential distribution system was described(Luo and Chan, 2014).

EV battery chargers can be primarily classified as off-board and on-board type. On-board chargers restrict the power that can be transferred because of the constraints due to cost, space occupied and weight. These on-board chargers can be

conductive or inductive. Off-board chargers can be designed for higher charging levels and are less constrained by weight and space issues. Level-1 chargers are known as convenience chargers where charging takes place over-night and single phase supply is adequate. Level-2 are called primary chargers and Level-3 chargers are fast chargers used for commercial applications requiring 3- phase power(Yilmaz and Krein, 2012).

Life cycle cost analysis when both grid and PV / diesel generator is available are studied, and the analysis of the data reveals that the cost of charging system was found to be cheaper if maximum power is obtained from grid and minimum from solar/ diesel generator(Yilmaz and Krein, 2012). But as the diesel prices go up and the technology in PV improves with improved efficiencies, the costs actually are recovered in 3 to 5 years promoting EV sector charging though PV source. A novel integrated bidirectional AC/DC charger and DC/DC converter for PHEVs an hybrid/plug-in-hybrid conversions is presented (Lee et al., 2009). The integrated converter is able to function as a battery charger and to transfer electrical energy between the battery pack a the high-voltage bus of the electric traction system. Higher initial cost, range anxiety, absence of charging infrastructure are the issues effecting the spread of EV. With promotion in the alternate fuel sector, lower costs due to improved technologies and economy of scale, there could be a considerable growth in the adaption of Electric Vehicle. Ultimate aim of any design in the area of power electronics is to optimize size, weight and cost, which eventually result in improving reliability and efficiency. The basic converter topology for battery charging application from PV source is the buck or boost converter. The efficiency of the boost converter is highest at low duty cycle and reduces with increase in duty cycle as been reported widely (Shreelakshmi et al., 2018).

To mitigate the effect of fuel scarcity, rising oil prices, poor air quality, and an increase in demand for personal transportation have paved the way for Battery Electric Vehicles (BEV). To charge these batteries from the conventional grid supply, AC/DC chargers are required, which meet the IEC 61000-3-2 standards. Single phase AC/DC converters were widely employed in applications such as uninterruptible power supplies and battery chargers. Conventional bridge rectifiers have over 55% Total Harmonic Distortion (THD) and a poor power factor. These converters necessitate Power Factor Correction (PFC) due to their poor power quality. The absence of PFC would result in poor efficiency, higher current pulses

being drawn at the source side, higher peak ratings of the devices, and hence increased losses. To reduce the peak currents and improve the input side power factor, filters were employed. Inductive and capacitive filters conventionally used for this application are very bulky as these need to be designed for power frequency. Inductor opposes the instantaneous change in currents, and therefore inrush current during turn-on can be reduced. The capacitor and inductor behave as complementary potential and kinetic energy storage elements, respectively, such that the input sees an impedance that is close to a resistive load.

Power factor topologies could be active or passive. Passive PFC incorporates LC filters at the source side, reduced EMI but bigger size due to the inductor. The advantage of such schemes is simpler control and inexpensive construction. Active PFC's require complex control; hence more sensors resulting in increased cost but lower weight and size due to the absence of source filters. The simplest configuration of an AC/DC converter consists of a bridge rectifier with a chopper. These choppers could be either buck or boost types. Boost converters require larger electrolytic capacitors for filtering requirement. The output voltage of the buck-based scheme would be lower than the peak of the input voltage, which can lead to a reduction of costs in terms of reduced ratings. But buck-based choppers require larger inductors to reduce the power pulsations. Buck converter-based PFC provides an alternate option for low voltage applications.

From the initial study conducted and observations made, the following objectives are framed:

- To design, simulate, mathematically analyze and develop DC-DC converters for EV battery charging application.
- Design and develop AC-DC converters with power factor correction.
- Implement appropriate algorithm for the extraction of maximum power from the PV Source.

1.2 Research Contributions

The research contribution of the thesis can be summarized as follows:

- Nature of the PV panel source and irradiance variation are studied and the observations help in estimation of the panel sizing and to work over the limitations.
- Lithium-Ion and Lead-Acid batteries were subjected to charge/discharge cycles. This was required to estimate the time required for charging and understand the nature of charge/discharge profile, which would further help in the estimation of source requirements and requirements of control schemes.
- An appropriate high gain DC-DC topology was designed and developed. Simulation and hardware studies are presented. Comparative evaluation of conventional boost converter with high gain converter was carried out and the results are disussed.
- An AC-DC converter with high step-down ratio incorporating PFC is developed. The proposed converter operates at a moderate duty cycle, due to its quadratic struture and offers higher step-down voltage
- Implementation of PSO algorithm on prototype and its study is presented.

The overall block digram of the converter model can be represented through the Figure 1.8. This thesis presents the prototype model of high gain DC/DC and AC/DC converters. For an EV which has a PV fixed within itself, and is getting charged while moving, there could be a rapid variation of irradiance occuring due to shading and other conditions. To meet the challenges of this varying irradiance, PSO algorithm was implemented.

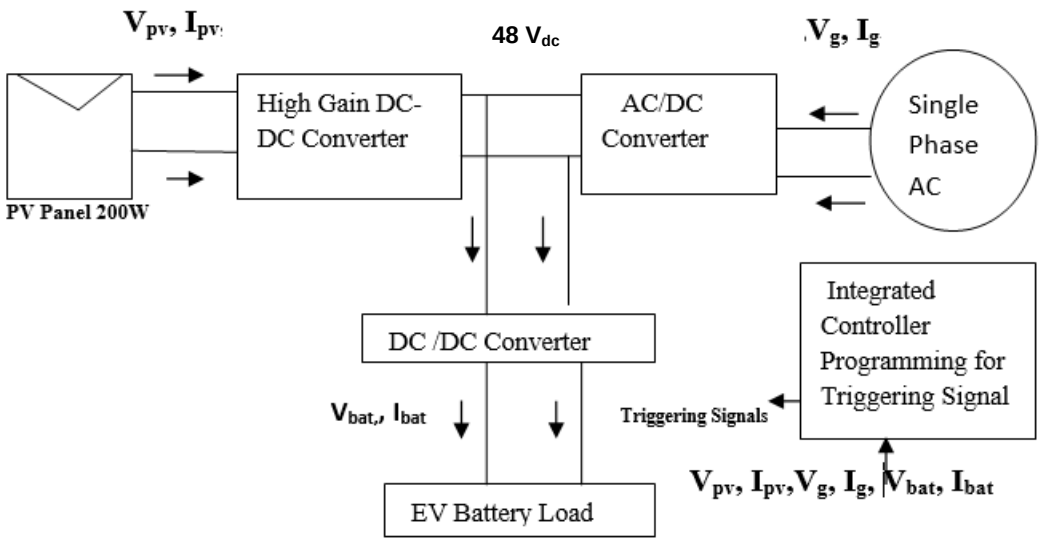


Figure 1.8: Converter Model

1.3 Thesis Organization

The proposed study will concentrate on modelling and developing different power converters. The thesis is organized into five chapters:

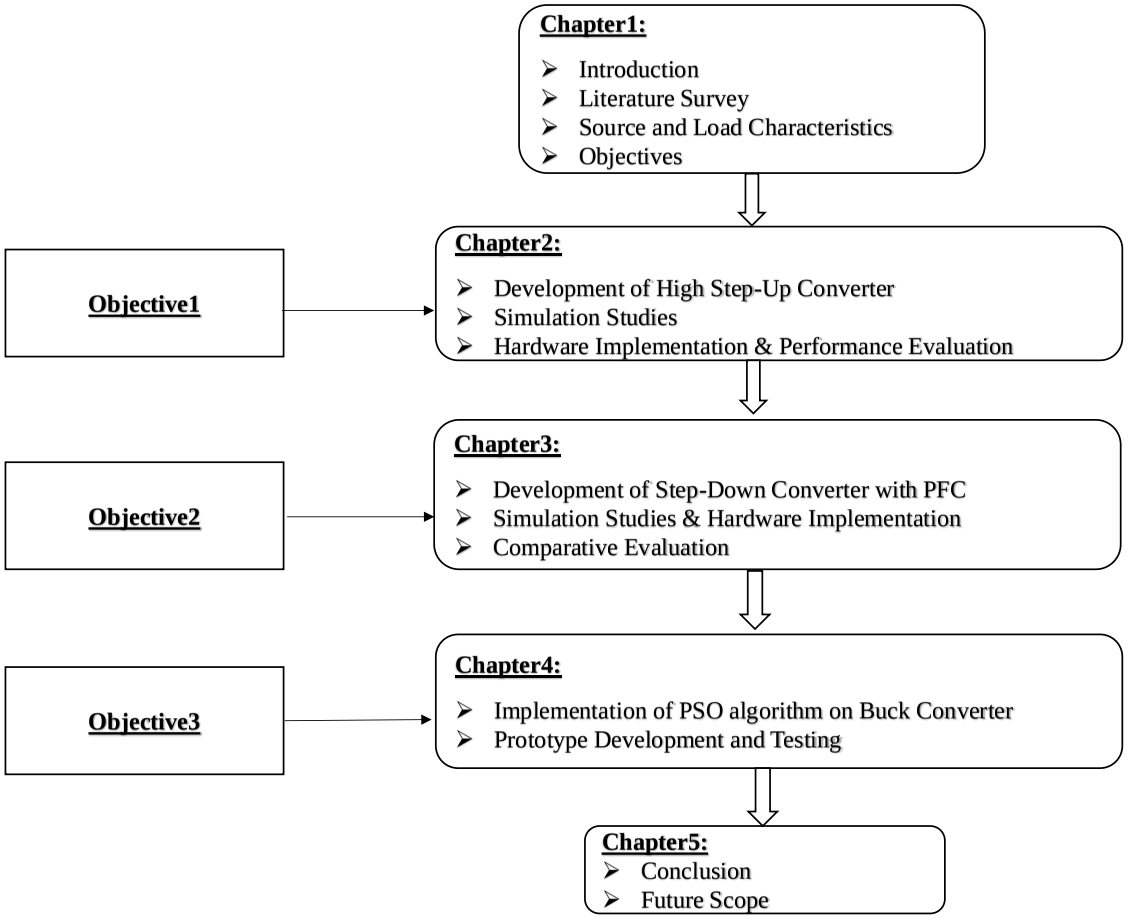
Chapter 1 : This chapter presents a brief introduction to the research work carried out. The research background, motivation for the work is described. The objectives framed to carry out the research are discussed along with organization of thesis. The chapter also discusses the PV source and battery load characteristics which are necessary for the design and development of the converter and control scheme. It also presents irradiance characteristics plotted over an average year to understand the nature of irradiance and determine the converter and controller specifications.

Chapter 2 : This chapter focusses on the the DC-DC converters and limitations of existing converter are identified. Improved high step up DC-DC boost converter topology is presented along with MATLAB based simulation studies. The operating modes of the prototype are discussed. The hardware implementation of the prototype is presented along with comparative evaluation against conventional boost converter.

Chapter 3 : This chapter presents the literature survey for AC-DC converters with PFC. Improved high step down AC-DC converter topology incorporating PFC is described and detailed simulation results are presented. The FPGA based hardware implementation of the prototype is presented.

Chapter 4 : This chapter describes the modified PSO algorithm and presents the hardware implementation.

Chapter 5 : This chapter summarizes the contributions of the research work and discusses the possible work as a future scope.


Chapter1:
Introduction
Literature Survey
Source and Load Characteristics
Objectives
Objective1
Chapter2:
Development of High Step-Up Converter
Simulation Studies
Hardware Implementation & Performance Evaluation
Objective2
Chapter3:
Development of Step-Down Converter with PFC
Simulation Studies & Hardware Implementation
Comparative Evaluation
Objective3
Chapter4:
Implementation of PSO algorithm on Buck Converter
Prototype Development and Testing
Chapter5:
Conclusion
Future Scope

Chapter 2

High Step-Up DC-DC Converter

Contents

2.1 Introduction

Converters used for battery charging in the available literature are buck, Cuk, buck-boost in non isolated categories for low power applications and flyback, forward, half-bridge, full-bridge for medium and high power categories. The low ripple content due to the filter inductor at the load side make buck derived topologies suitable for

charging. Observations made from the studies conducted on the PV panel indicate the requirement of a converter that can have a higher voltage gain and charge a battery of 54 V with 21 V PV source.

The buck converter cannot be used for charging electric vehicle battery as the load voltage is significantly higher over the source. In the buck-boost based topologies , a high duty cycle of 70% to 80% is required to charge a (48 -54/ 57) V load from (21 -26) V source which offers a low margin for control. Boost converter might be required to be operated over 62% duty cycle considering ideal conditions. Considering diode, inductor and switch drops and drop across ESR of the capacitor will require the system to operate at still higher duty cycle where efficiency reduces and the size of the components will increase.

Isolated topologies can offer a higher gain by appropriate design with turns ratio, but are bulky. The leakage inductance causes the switching spikes, which have to be tolerated or protection required through snubber network. Non-isolated high gain topologies, hence are required for higher efficiency and small size. Non-isolated topologies with single stage conversion such as quadratic and interleaved buck are reported for low voltage and high current applications(Revathi and Prabhakar, 2016).

Conventional charging of EV from the power grid results in harmonics and requires filtering or power factor correction techniques. Already the power sector is overburdened and to cater to the needs of EV sector, alternate resources need to be explored. Photovoltaic source (PV) offers a viable alternative as a local generation and utilization, reducing the burden on existing generation as well as the additional transmission and distribution loads. But PV as a source is variable and intermittent, the power converter should be capable of meeting the wide variations caused due to varying irradiance and providing dependable power.

To charge a high voltage battery (48 to 72 V), from a low voltage PV source, boost converter with higher gain would be required. Boost based topologies, though offer a filtration at the source side, due to the source inductor , load side filtering might be required.

A number of topologies for ripple minimization with interleaved, cascaded, coupled, synchronous rectification based topologies are discussed in the literature. Coupled inductor based topologies require high turns ratio, hence size of the inductor and hence conduction losses increase along with the requirement of snubber

or active clamp circuit for minimizing the switching stress(Yang et al., 2017),(Wu et al., 2016a). Switched capacitor / inductor based voltage multiplier cells which can either act in buck / boost / buck boost mode were discussed (Axelrod et al., 2008).

Study and design of boost converters using voltage multiplier cells was reported(Prudente et al., 2005). Most of the topologies are applied for a gain of over five and above which is required to step up low PV voltage to high dc link voltage through MPP extraction and processed further for inversion. Z source based and switched capacitor topologies though offer high gain has a limitation of high input current ripple. High gain high power topology was investigated (Wai et al., 2012). This topology offers twice the gain of conventional boost converter with ZVS operation of switches and ZCS operation of diodes. Extremely high gain topologies discussed above with a quadratic and above gains require a very small duty cycle for low voltage EV battery-based applications . The size of the conductor increases and hence the losses (Park and Choi, 2009). The high voltage gain topologies reported in the literature offer an extremely high gain of 6-8 times. These converters would need to be triggered at a very low duty cycle and hence the component size increases leading to higher costs and losses. An investigation into appropriate topology which can offer higher voltage gain at moderate duty cycle is essential.

This thesis presnts a modified boost converter topology for electric vehicle charging from a PV source. The proposed topology offers higher voltage gain and lower ripple content over the conventional boost converter. Simulation studies on the performance of conventional and modified boost converter are performed using MATLAB/Simulink. The proposed topology has a single switch and results indicate higher voltage gain and higher output voltage with a moderate duty cycle. The topological details of the proposed topology are described in detail and comparative evaluation with conventional boost converter is discussed. The performance of the proposed topology is validated with the experimental setup.

2.2 Problem Formulation

The power converter designed should be capable of meeting the wide variations caused due to varying irradiance and providing dependable power. The conventional boost converter has inductor on the source side and capacitor on load side. It offers a maximum gain of twice the input for higher efficiency with a limitation of 50% duty

cycle. Extremely high gain topologies discussed in the literature with a quadratic and above require a very small duty cycle for low voltage EV battery based applications. The size of the conductor increases and hence the losses.

Hence there is a need for a topology which meets the requirement of moderate gain and development of control scheme and overcome the challenges of varying source and load requirements. The reconfigured topology discussed in this chapter offers a higher gain which is linearly varying and not exponential as in the case of quadratic high gain topologies and hence more suitable for PV based EV battery charging applications.

2.3 Boost Converter

Observations made from the studies conducted on PV panel indicate the requirement of a converter that can have a higher gain and charge a battery of 54 V with 21 V PV source. The operation of conventional boost converter represented by the Figure 2.1, can be described with the assumptions that all the devices are ideal, losses across the devices are negligible and ESR of inductor and capacitor are neglected.

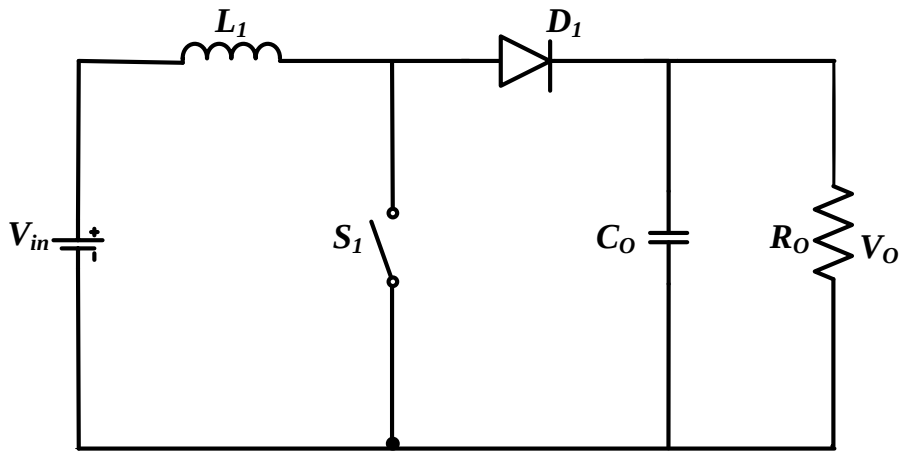


Figure 2.1: Boost converter

- **Mode1**: When switch is closed, the current flows through the inductor and the energy is stored, and hence the inductor charges. During this period, capacitor supplies the load current.

- **Mode2**: Switch is opened and the inductor discharges. The sum of input and voltage across the inductor appears across the load. Capacitor begins to charge and the voltage gain for the conventioncal boost converter is given by $V_o/V_{in} = \frac{1}{(1-k)}$,where 'k' is the duty cycle.

The operation of the conventional boost converter with a 21 V input was studied. Arduino board was used to generate a pulse of 48% duty cycle with 30 kHz. Opto coupler 4N25A was used to provide the necessary isolation. As MOSFET IRF 740 needs a higher voltage to switch at high frequency, IR 2011 was used as a driver IC. The output was observed as shown in Figure 2.2. Input was stepped up to 42 V which

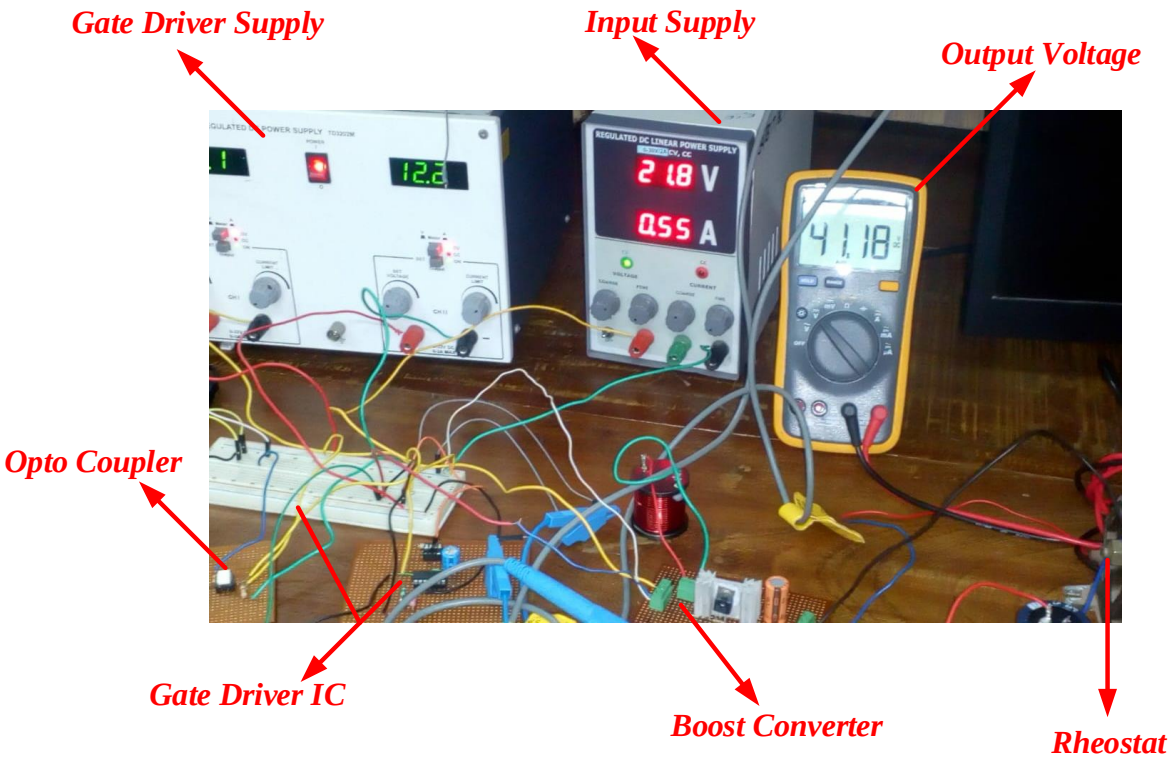


Figure 2.2: Hardware Setup of Boost converter

matches with the expected results. Observations made from the studies conducted on speifiations of the soure, indicate the requirement of a converter that can have a higher gain and charge a battery of 54 V with 21 V PV source. Conventional boost converter might be required to be operated over 62% duty cycle considering ideal

conditions. Practically considering device voltage drops across the diode, inductor, ESR of capacitor, the converter is required to operate at still higher duty cycle where efficiency reduces.

2.4 Modified Boost Converter

To improve voltage gain of the converters, a number of circuits with gain cells are available and reported in the literature as represented in Figure2.3 (Prudente et al., 2008). Topologies which offer a higher gain over the conventional boost converter can be formed by incorporating cells which can be switched capacitor, coupled inductor or based on diodes and capacitors (Zhang et al., 2015). Incorporating these cells, the required gain can be obtained. The present topology utilizes the gain cell Figure 2.3(d) for developing the converter as shown in Figure 2.4.

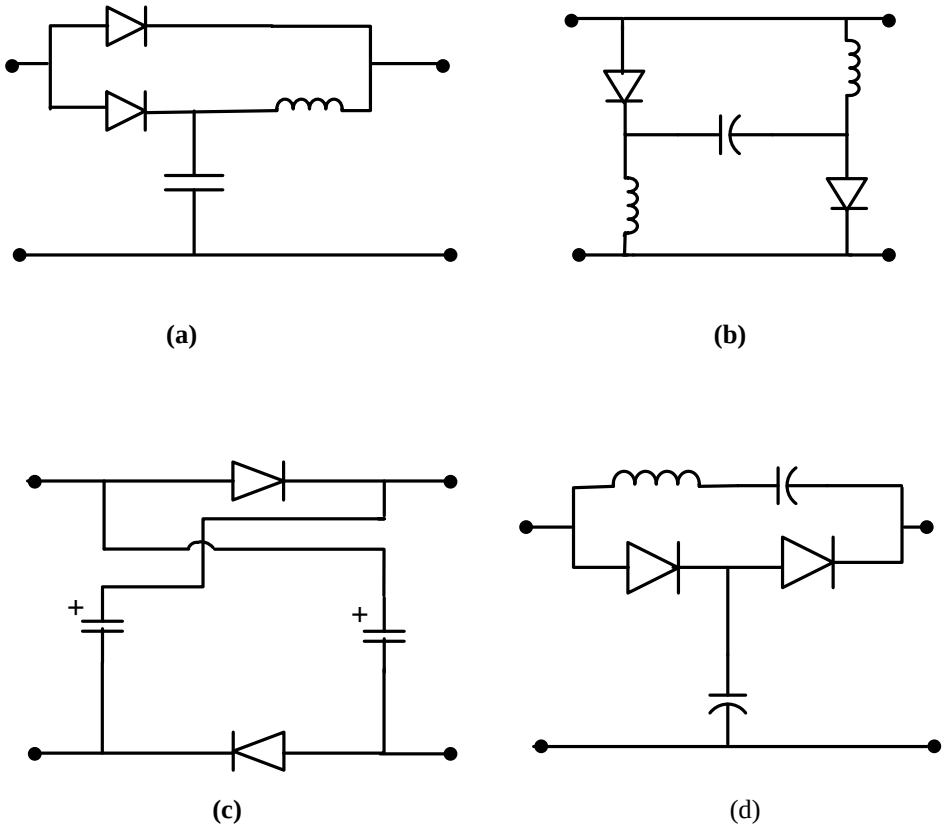


Figure 2.3: Gain Cells in Literature

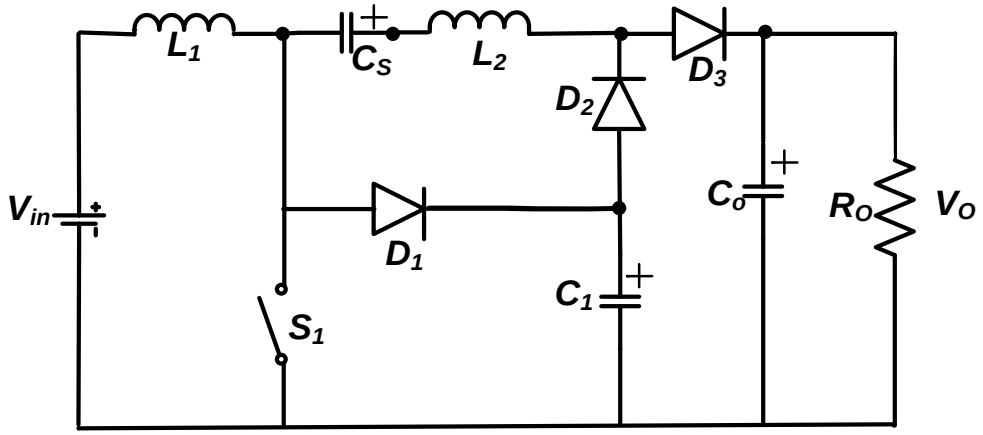


Figure 2.4: Modified Boost converter

To understand the operating modes, the following assumptions are made

- The diodes D_1 and D_3 conduct simultaneously. Similarly, the Switch S_1 and the diode D_2 conduct simultaneously.
- The parasitic resistances of the inductor and the capacitor are not considered.
- The diode and switch forward drops are not considered.
- The capacitors are large and ripple free.

The operation of the converter can be described as follows

- **Mode1**: When the switch S_1 is closed, the inductor L_1 charges through the switch and the current through the L_1 increases. C_O supplies the power to the load and get discharged as represented in Figure 2.5. In addition, through the path D_2, L_2, the series capacitor C_S gets charged through the switch S_1 connected to the ground. D_1 does not conduct as its anode gets reverse biased. The diode D_1 blocks the voltage of C_1 and needs to be rated at the load voltage. As the output capacitor is discharging to the load, the diode D_3 gets reverse biased and does not conduct. Considering the current through the inductors

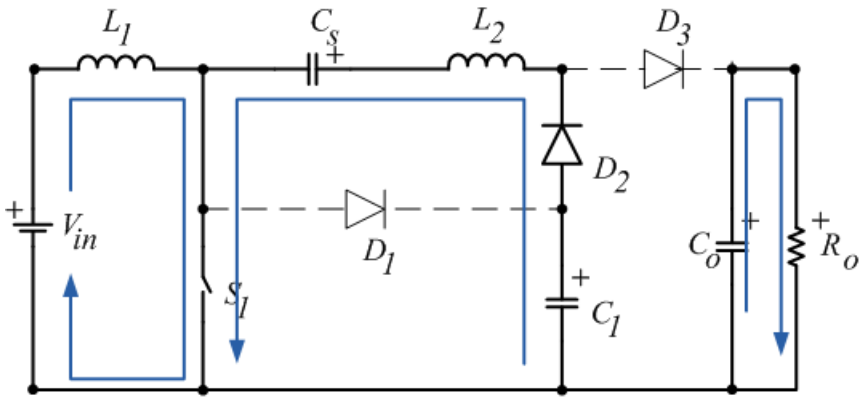


Figure 2.5: Operating mode (When S_1 is closed)

and voltage across the capacitors as state variables, $i_{L1} = X_1, V_{C1} = X_2, V_{C_S} = X_3, i_{L2} = X_4$ and V_0 & $V_{C_O} = X_5$, The Equation (2.1) can be written for the operation when tho switch S_1 is closed as follows:

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \\ \dot{X}_4 \\ \dot{X}_5 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{C_1} & 0 \\ 0 & 0 & 0 & \frac{1}{C_S} & 0 \\ 0 & \frac{1}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_O C_O} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{2.1}$$

The output Equation 2.2 can be expressed in relation to the capacitor terminal voltage $V_{C_O}$and inductor current i_{L1} as follows:

$$\begin{bmatrix} V_O \\ i_{L1} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \end{bmatrix} \tag{2.2}$$

Mode2 : The switch S_1 is turned off and the operation is showed in Figure 2.6 and expressed in Equation 2.3. The current through the inductor now flows through

D_1,the capacitor C_1 gets charged as the conventional boost converter with a gain $\frac{1}{(1-k)}$. The Conventional gain of the converter is $\frac{2}{(1-k)}$, where k is the duty cycle. The charge- discharge profile of the inductor current and various capacitor voltages are represented through Figure 2.7

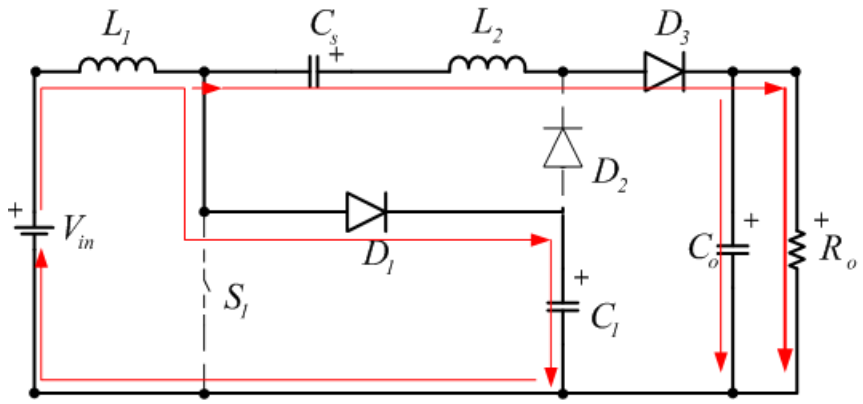


Figure 2.6: Operating mode (Switch S_1 is open)

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \\ \dot{X}_4 \\ \dot{X}_5 \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_1} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & \frac{-1}{C_1} & 0 \\ 0 & 0 & 0 & \frac{1}{C_S} & 0 \\ 0 & \frac{1}{L_2} & \frac{1}{L_2} & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{-1}{C_O} & \frac{1}{R_O C_O} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{2.3}$$

The output equation is similar to the one as expressed by Equation 2.2.

The nature of steady state voltages and currents are plotted, and represented through Figure 2.7

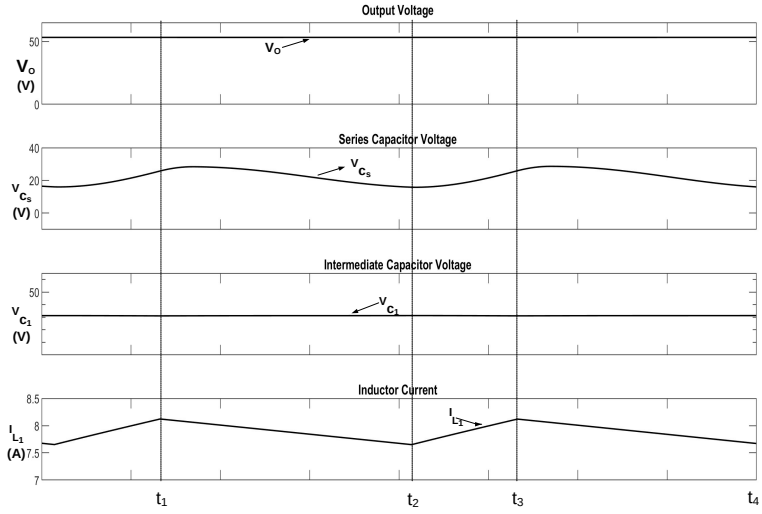


Figure 2.7: Charge- Discharge Profile of LC Components

2.5 Simulation and Harware Results

Simulation studies are conducted with MATLAB, Simulink Version R2015b. The simulation studies are performed with specifications as in Table 2.1 with *dc* source of 21 V and with a resistive load of 20 Ω. The simulation studies indicated a linear relationship with higher gain.

2.5.1 Modified Boost Converter using Arduino

To validate the simulation results, a 48% duty cycle pulse was generated using Arduino with a frequency of 30 kHz. Optocoupler 4N25A was used to provide the necessary isolation. IR 2011 was used as a driver to switch MOSFET (IRF 740) and apply sufficient voltage to control turn-on/ turn-off action at high frequency. The signals were observed on a DSO. A prototype of the modified boost converter is rigged up as in Figure 2.8 with a resistive load and tested. The study was performed with a constant duty cycle of 45% and input voltage was varied between 6 V and 22 V. The obtained values are plotted with a theoretical gain of conventional boost converter as in Figure 2.9. The results indicate the developed converter offers a higher voltage gain over conventional boost converter. For a 48% duty cycle, the converter with 22 V input gives an output voltage of 51 V, and is suitable for 48 V, EV battery charging.

Table 2.1: Parameters used for simulation and hardware studies

Inductors (L_1, L_2)	570 µH, 270 µH
Capacitors (C_S, C_O, C_1)	0.47 µF,220 µF,1000 µF
MOSFET	IRF 740
Diodes	UF 5408

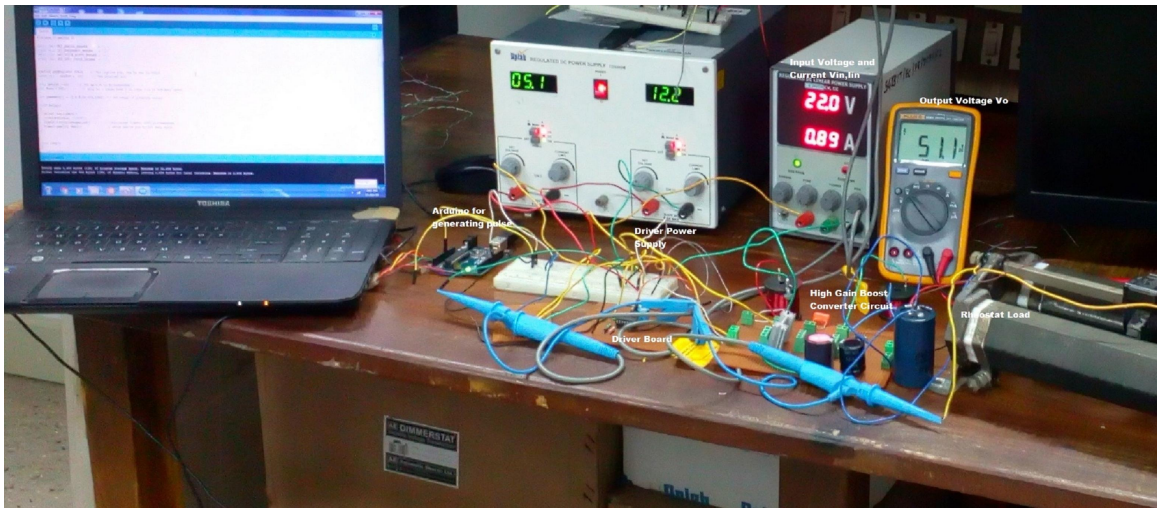


Figure 2.8: Experimental Setup of Modified Boost converter

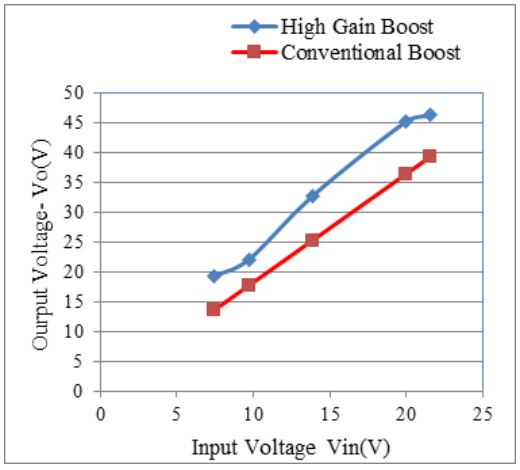


Figure 2.9: Hardware Comparative Studies with variation in input voltage

2.5.2 Simulation Results with DC and PV Source

A *dc* source of 28 V was selected and the modified boost converter topology was simulated with a load which draws 3 current was used. Simulations results show a gain of nearly 44% gain for 35% duty cycle as shown in 2.10. As the results

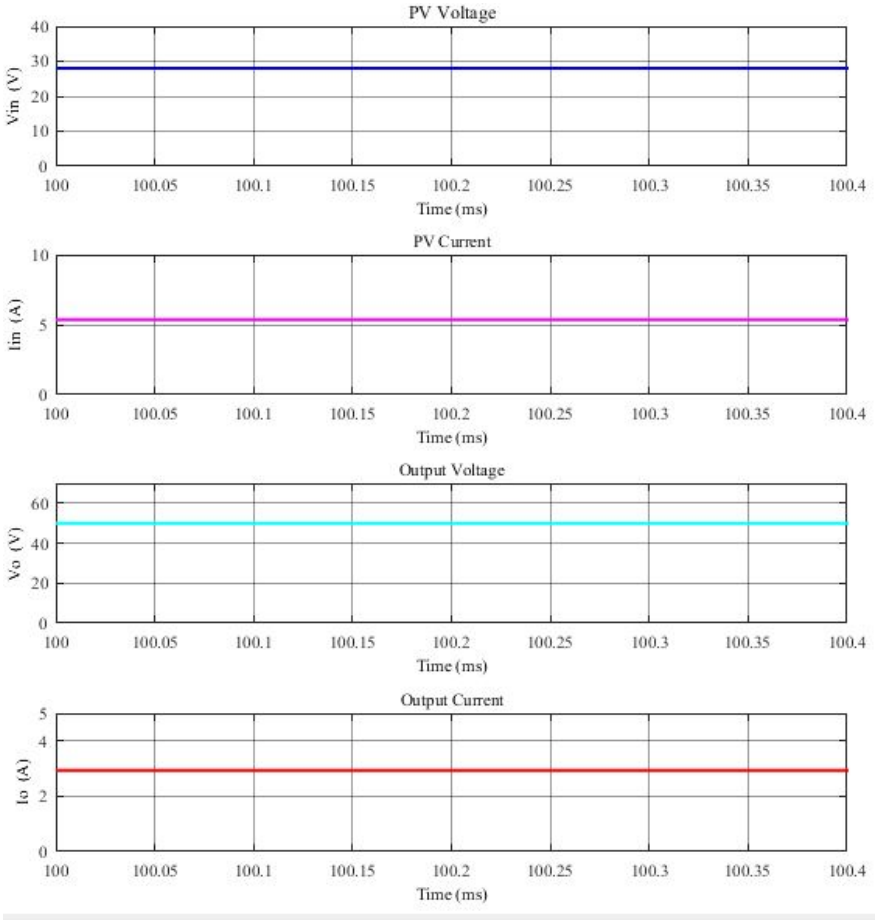


Figure 2.10: Open loop simulation results with *dc* source

are encouraging, a PV Panel of 200 W model of Waaree Energies make was used as a source and irradiance was set at 800 W/m^2. Studies were conducted with a resistive load of 16 Ω & at a temperature 25^oC and 25% duty cycle. The results indicated a higher gain. In practical systems, the device drops, temperature effect, varying irradiance and the losses of the converter could lead to lower output, but the duty cycle can be increased to meet the requirements. When the irradiance is lowered, the load resistance needs to be lowered to enable proper step-up operation and extraction of power. The conventional MPP algorithms need to be modified to

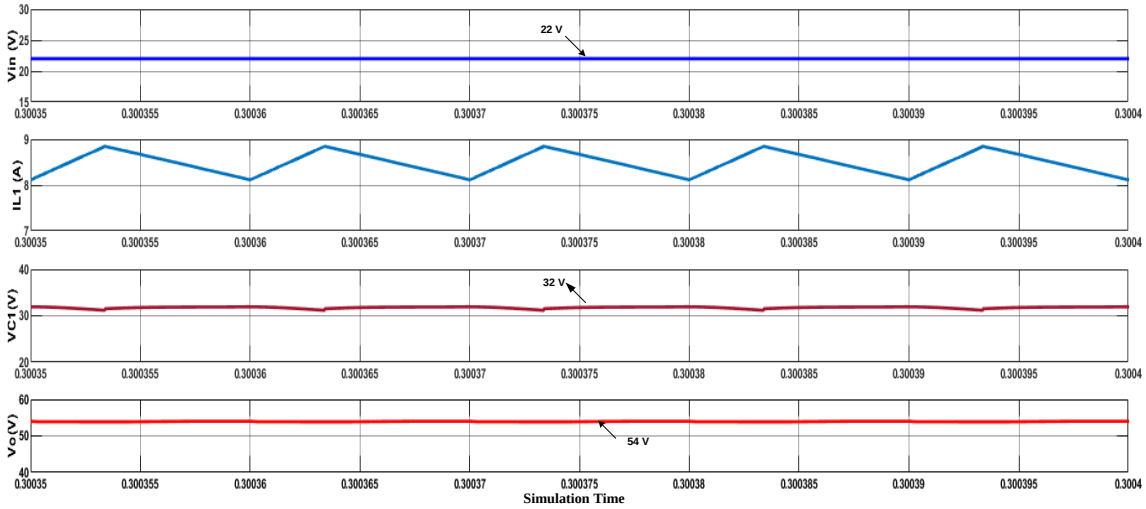


Figure 2.11: Simulation results of closed loop control using PID tuner of Simscape/MATLAB

match the requirement when the load is a standalone battery as in the case of EV. Battery peak voltage requirement of 54.5 V cannot be exceeded and the current limits needs to be considered.

Using PID tuner application of the MATLAB, tuning is done and the values of PI gains are obtained. Reference is set at 54 V as desired for the battery charging application. A closed loop simulation study is conducted. The inductor current waveform as in Figure 2.11 indicates that at a moderate duty cycle, desired output can be obtained. The converter is tested with a step change in load voltage as the battery terminal voltage slowly rises, The designed PI controller is able to appropriately track the voltage within small time with minimum overshoot as shown in Figure 2.12

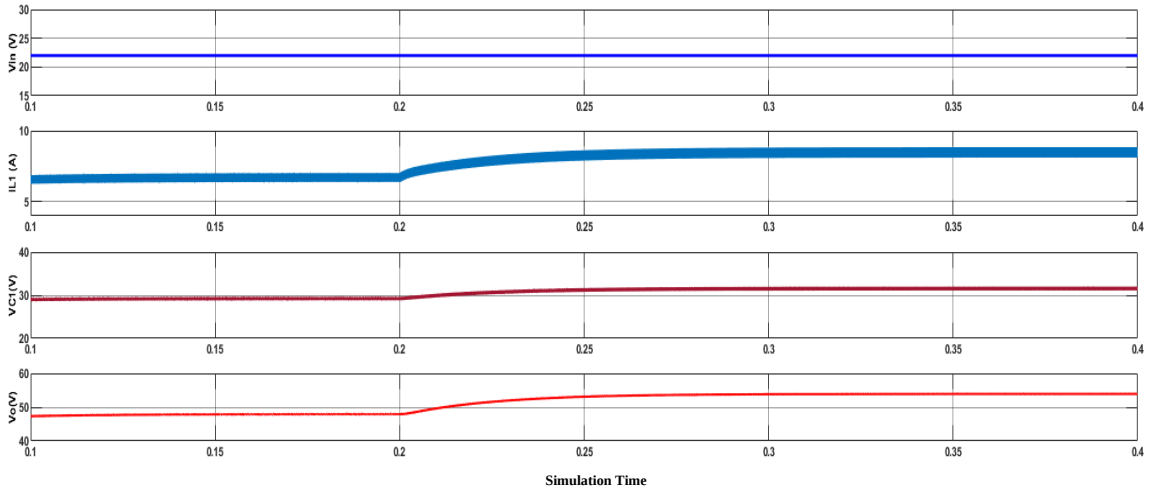


Figure 2.12: Simulation results of applied input voltage, Inductor current variation, Intermediate boost capacitor Output, Controlled output voltage from 48 V to 54 V

2.5.3 Hardware Results of Modified Boost Converter using FPGA

The gain though high was not substantial to justify additional components over conventional Boost converter. To reduce the size of the inductors, it was necessary to increase frequency. To improve further the gain of the system, the converter was redesigned with parameters as in Table 2.2.

A small inductor of 4 µH at the battery side has improved the gain of the converter. Higher efficiency is achieved by choosing MOSFETs with low R_{ds}(on), employing fast and soft recovery diodes, winding inductors with minimum series resistance at high frequency operation. Further increase in efficiency can be achieved by PCB design to reduce the connecting wire resistance. Incorporating better quality CRGO / nickel-iron/ amorphous/ mu metal and other varieties cores which offer low hysterisis and eddy current losses improves the saturation characteristics. Inductors and capacitors with low ESR were required to be used.

2.5.4 Design of the Inductor

Following the conventional boost converter, the inductor is designed using Equation (1.5), which gives a value of 270 µH for the continuous current mode. If the inductor L_1 operates in discontinuous mode, the component used was to be lesser than 270

Table 2.2: Parameters of Modified Boost Converter for 50kHz operation using FPGA

Inductors (L_1, L_2)	270 µH (Coil Craft / EE Core), 4 µH (EE Core)
Capacitors (C_S, C_O, C_1)	4.7 µF (Polystyrene),220 µF,3300 µF (Electrolytic)
MOSFET	Infineon IPP200N15N3G $R_{ds}on$ with 20 mΩ
Diodes	DPG151200PA Fast diode rated at 15 A

µH, and the estimated value for L_2 is 4 µH. Minimum value of duty cycle is assumed to 0.2 to satisfy the converter gain requirements.

$$\left.\begin{aligned} \mathrm{L_1} &= \frac{\mathrm{V_{in}} * k}{\Delta \mathrm{i_L} \mathrm{F_S}} \\ \mathrm{L_1} &= \frac{27 * 0.2}{0.4 * 50000} = 270\mu\mathrm{H} \end{aligned}\right\} \tag{2.4}$$

2.5.5 Design of the Output Capacitors

Using the output ripple constraints and the load power requirement from Equation Considering the output voltage ripple ΔV_O as 10 mV.

$$\left.\begin{aligned} \mathrm{C_O} &= \frac{\mathrm{I_O} * k}{\mathrm{F_S} * \Delta \mathrm{V_O}} \\ \mathrm{C_O} &= \frac{3 * 0.3}{0.01 * 50000} = 1800\mu\mathrm{F} \end{aligned}\right\} \tag{2.5}$$

The simulation studies are performed with specifications as in Table 2.2 with *dc* source of 21 V and with a resistive load of 17 Ω. The simulation studies indicated a linear relationship with higher gain. Study was conducted by varying the duty cycle from 20 % to 80 % and the output reflects a higher gain over the conventional boost converter as shown in Figure 2.13. Pulses are generated by using comparison of a constant value with a saw tooth wave of 50 kHz in MATLAB/Simulink, constant magnitude is varied to obtain pulses of 25% to 50% as in Figure 2.14.

These pulses were sent to the output ports of Basys 3 which is an Artrix7- 35T based FPGA from Xilinx using Vivado design suite as the user interface. The hardware expermimental setup is shown in Figure 2.15. Pmod ports $J_1, L_2, J_2, H_1, K_2, \& H_2$ are used as the output ports with each duty cycle assigned with specific port for convenience and faster analysis. These pulses are of 3.6 V, and hence not sufficient to drive MOSFET's. TLP350 is used as a driver and opto isolator. Inductor L_1, Capacitor C_O are designed using the conventional boost

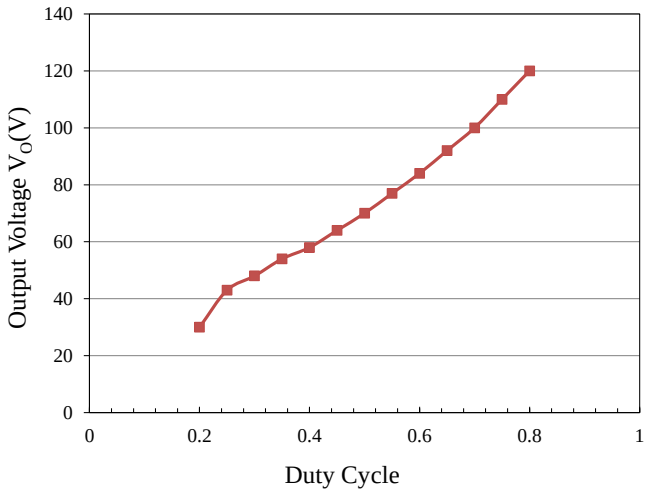


Figure 2.13: Voltage gain with duty cycle variation

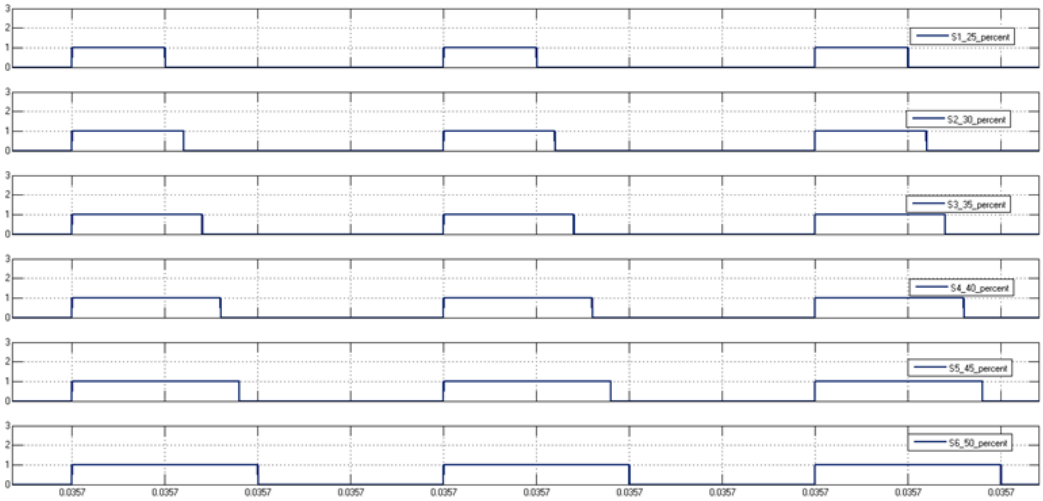


Figure 2.14: Pulses generated using system generator in MATLAB for FPGA

converter equations. C_1 and C_S are required to be very low values for high frequency switching operation for appropriate energy transfer. L_2 is a small inductor of 2 µH. The observations made with different inductors indicate that as the value of inductor L_2 increases, there is a reduction in voltage gain with a prolonged conduction of switch. Further study was performed by varying the duty cycle between 25% & 45% and the input voltage was varied between 5 V and 26 V and the results plotted.

The results indicate modified boost converter offers a higher voltage gain over

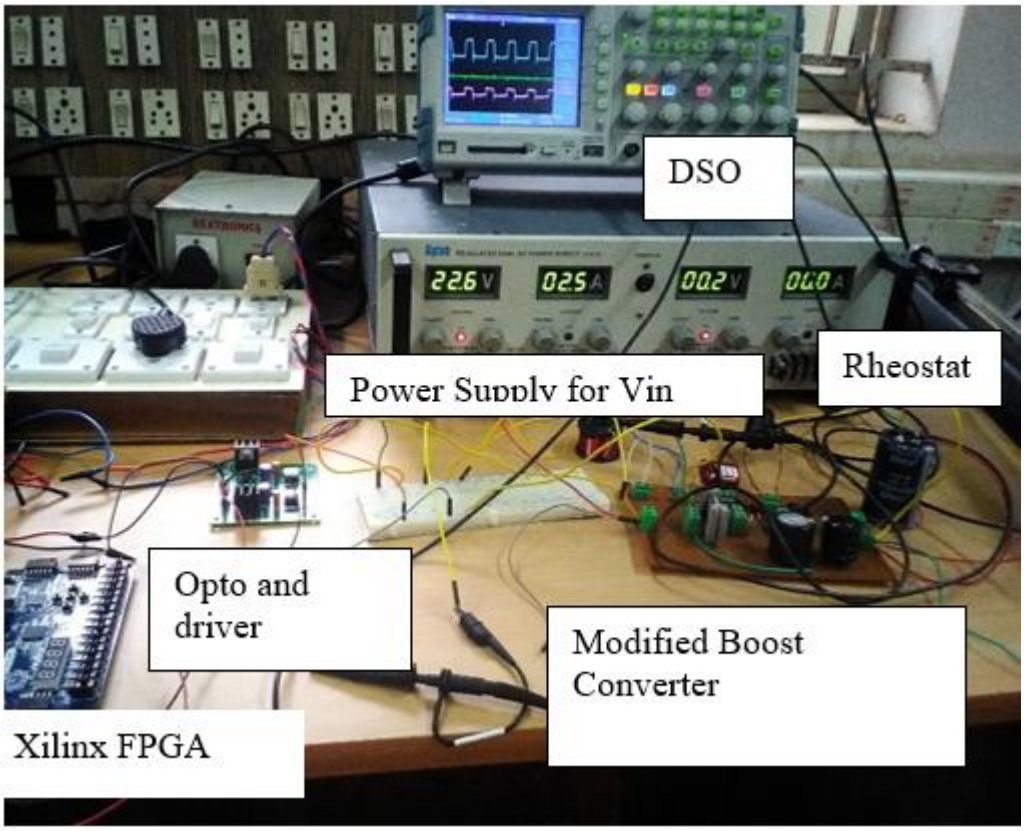
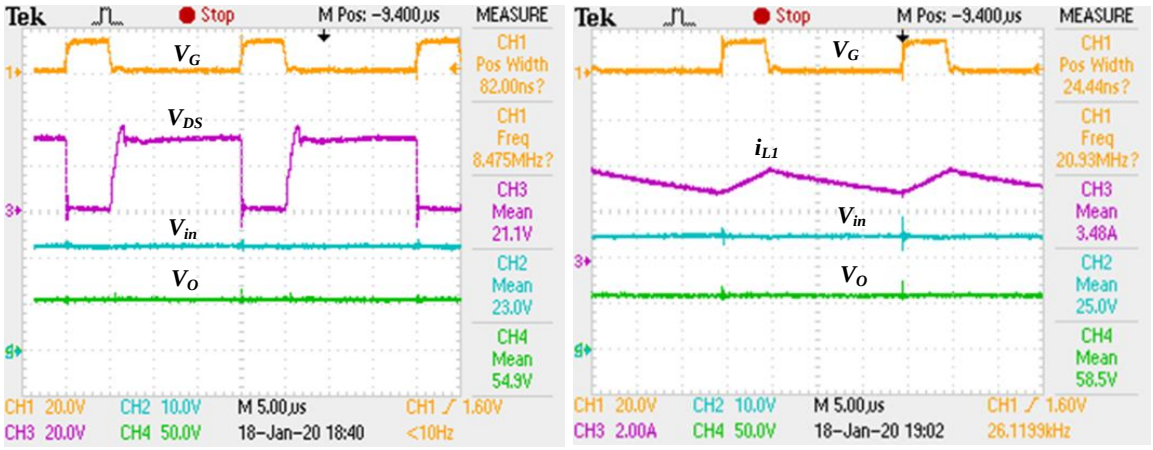


Figure 2.15: Experimental setup of modified boost converter with FPGA



(a) (b)

Figure 2.16: Experimental waveforms(a) Relation between input and output voltages at 25% duty cycle(b) Inductor Current with 25% duty cycle

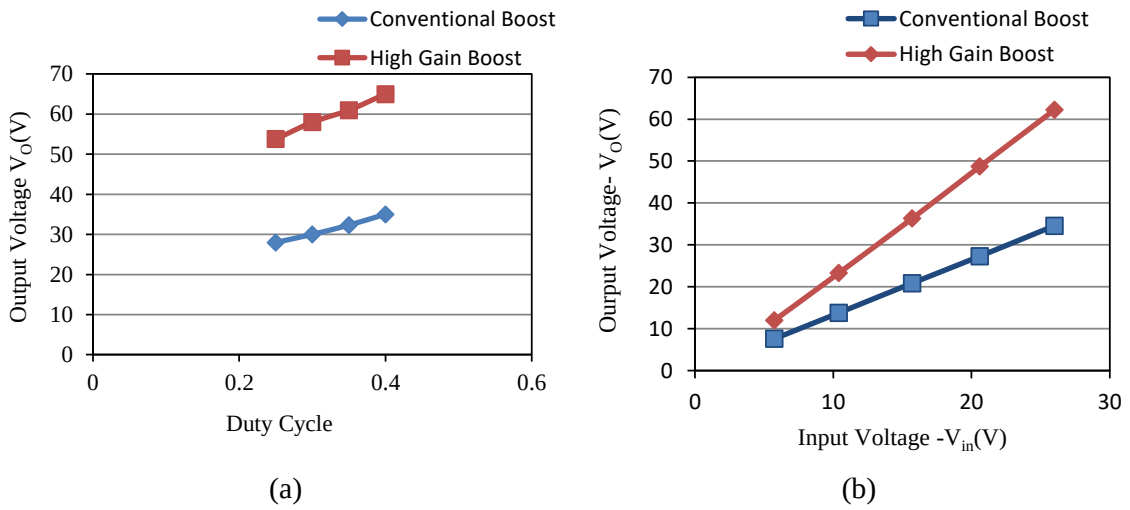


Figure 2.17: Comparative study of converters (a)Variation of output voltage with duty cycle (V_{in} constant) (b)Variation of output voltage with variable input (Duty cycle constant)

conventional converter as shown in Figure 2.17, and is suitable for PV applications. Reversal of polarity with pulse is seen across the inductors L_1&L_2. Efficiency of the converter is obtained by the experimental results. Input and output voltages are measured through the four channel DSO available in the laboratory. Current is measured through current TCP2020, 50 MHz, 20 A, AC/DC Current Probe, measured through DSO. Efficiency is estimated to be around 94% initially when the converter load is drawing low current of 1 Ampere. As the load resistance was varied from 50 Ω to 18 Ω , thereby increasing load current and hence source current has risen to around 4.8 A. The efficiency of the converter is reduced to 78% due to the increased losses.

Table 2.3: Study of various power converter topologies available in literature

Ref.No	Topology	Voltage Range	Switching Frequency	Power	Efficiency %	No. of Switches
(Shreelakshmi et al., 2018)	Coupled inductor	(40 -400) V	50 kHz	500 W	94	4
(Kwon et al., 2013)	voltage doubler	(40-60) V -400 V	100 kHz	1 kW	95	4
(Sahoo and Kumar, 2014)	Switched Capacitor	(12 V- 68 V)	100 kHz	450 W	92-95	12
(Yao et al., 2015)	Coupled Inductor	(14 V - 42 V)	50 kHz	200 W	92-97	3
(Wu et al., 2016b)	Coupled Inductor	(48V - 360 V)	100 kHz	2 kW	92-95	3
(Mishima et al., 2014)	Resonant tank	(200V-400V)	50 kHz	2.2 kW	94	3
(Sun et al., 2016)	CF -DAB	(30-60) V - 400 V	100 kHz	1 kW	91.7	6
(Pires et al., 2017)	Quadratic boost	(24-180) V	15 kHZ	80W -200 W	(83 -88)	6

2.6 MATLAB Simulations and PID Tuner

General form of PID controller can be represented as $u(t) = k(e(t) + \frac{1}{T_i}\int_0^t e(\tau)d\tau + T_d\frac{de(t)}{dt})$.To determine the values of Kp, Ki, Kd many tuning methods are developed. In MATLAB, PID Tuner app is utilized which facilitates automatically tuning the gains of a PID controller for a Single-Input Single-Output (SISO) plant, achieving a balance between performance and robustness.P, PI or PID controller blocks can be selected and controller performance can be checked both in time and frequency domains. The controller gain parameters thus obtained through pole are substituted in the MATLAB- simulink model and the output is observed with change in source voltage and load current. The output observed through scope shows that though the peak overshoot and through repeated simulations, changing the value of proportional or integral gain, the peak overshoot is substantially reduced.

2.7 Summary

In this Chapter, a unidirectional modified boost converter is described. The operating modes are discussed. Simulation results using MATLAB / Simulink are presented. The simulation studies of the open-loop operation of the proposed converter with PV source and resistive load are carried and are presented. The simulation studies indicated a higher gain over a conventional boost converter. The prototype of the conventional boost converter was tested and compared with the modified converter using Arduino and FPGA controllers. The results indicate a higher voltage gain achieved by the reconfigured modified boost topology using FPGA and in agreement with simulation results.

Chapter 3

Power Factor Corrected AC to DC Converter with High Step-Down Voltage Ratio

Contents

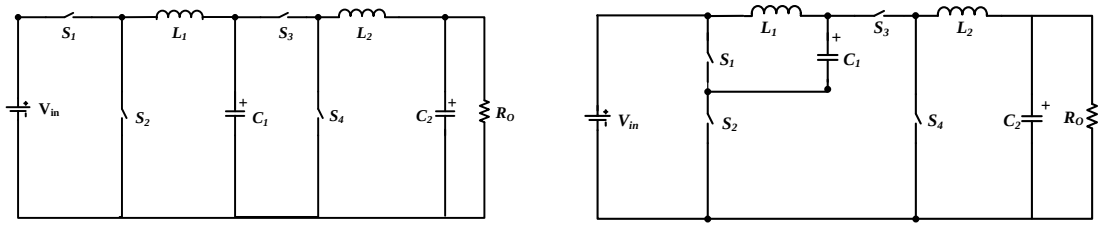
3.1 Introduction

The development of Electric Vehicle will bring in requirement of capacity expansion of the existing system. The uncertain and unorganized charging will lead to a large difference in the peak and valley loads of the power system apart from requirement of topologies with inherent power factor correction. This work presents a high step-down ratio AC-DC converter employing a QBC topology with inherent PFC. Converters need to operate at an extremely low duty cycle in applications that require a low output from higher input. Due to the limitation of the turn-on/ off of the devices, switching frequency needs to be reduced, and hence the size of the inductors and capacitors become bulkier. Conventional active power factor correction topologies employ boost-based correction schemes for unity PFC operation. This will require a still steeper step-down ratio and higher switch voltage stress apart from complexity in the control scheme with sensors.

The proposed topology presents an investigation and comparative evaluation of the conventional bridgeless buck system with the QBC PFC. MATLAB R2020b is used for carrying out simulation studies. Xilinx FPGA-based controller using system generator is implemented for the generation of pulses of appropriate duty cycle. Simulation and experimental results for a 150 W prototype are presented.

3.2 Research Background

To incorporate PFC a family of unidirectional/bi-directional, active /passive, boost, buck, buck-boost, isolated, multi-level-based PFC topologies were reported in the literature (Singh et al., 2003). The other kind of PFC topologies proposed in the literature are bridgeless. These bridgeless converters have reduced the number of devices in the current path achieving higher efficiency and lower losses. These can be further categorized into boost and buck-boost (Zhao et al., 2015),(Huber et al., 2008).A bridgeless Cuk-flyback converter has been reported operating in



(a) (b)

Figure 3.1: (a)Cascaded Buck Converter (b)Realization of QBC

discontinuous mode with a very high-power factor and lower loss(Kushwaha and Singh, 2019b). Though the system reports high efficiency and smaller size, the system is complex with more components.

A bridgeless buck topology is presented through a power factor corrected rectifier coupled with the buck topology(Fardoun et al., 2014). The conventional 230 V_{rms} system would need a higher step-down ratio to obtain a 48 V_{dc}. The conventional buck converters cannot be employed as they need to be operated at a very low duty ratio of twenty percent. The size of the components will become bulkier with lower switching frequency limitations considering the slower charging and discharging apart from the switch constraints. There are also bidirectional converters for returning power to the grid for power stability.

If two buck converters are connected in cascade, the converter, as shown in Figure 3.1a, would be realized with a wide step-down ratio. The disadvantage of the cascaded converter is that the number of active switches in the power path is more, resulting in increased switching losses. Reducing redundant states, a converter with a quadratic relationship between the output and input is realized as in Figure 3.1(b) (Maksimovic and Cuk, 1991). The converters have the cascaded buck arrangement with twice the number of inductors and capacitors and hence exhibit fourth-order dynamics. These converters were studied for lower input voltages and wider step-down ratio with an average mode of current control with dc input source and for lower power requirements of less than 20W applications (Morales-Saldana et al., 2008). A bidirectional converter with a quadratic relationship for the battery was investigated (Pires et al., 2017). The experiment has been verified with resistive loads of 7 Ω and 330 Ω for a buck and boost operation. The conversion ratio had been 24 V/180 V.

Buck converter at a very low duty cycle can yield high power factor correction(Grigore and Kyyra, 2000). A series of boost and buck-boost topologies for PFC were investigated (Tse and Chow, 1998). Quadratic gain bidirectional converters for regenerating braking application were investigated for battery/supercapacitor storage applications (Kumar et al., 2022). Topologies using transformer / coupled inductor for high step-up / step down were discussed by (Prasanna et al., 2017),(Wu and Chen, 2019),(Chavoshipour Heris et al., 2019). A bridgeless SEPIC converter with coupled inductor topology for high step-up was investigated for motor drive application (Prabhu and Urundady, 2020). Cascaded Cuk -Buck, quadratic buck-boost topologies were designed and reported for low voltage stress and reduced ripple conditions. Performance evaluation of PFC boost was investigated (Huber et al., 2008). However, many of these topologies are for step-up/step-down DC /DC conversion. Traditionally boost topologies are preferred for PFC, but the high output voltage stage which is above the peak of supply voltage, makes the system more complex. There is also a requirement of feedback and multiple sensors and switches for a low voltage step-down application.
Interleaved converters were investigated for a higher step-down ratio. Studies were conducted to increase the power rating of the load, improve the efficiency, and lower switching losses using interleaved QBC topology (Lee et al., 2012), (Pan et al., 2014). The literature proposes quadratic converters interfaced with forward / flyback topology to provide isolation requirements. Interleaving reduces the current stress and offers lower loss. The proposed converters have multiple switches switching at 180-degree phase shifts(Esteki et al., 2015). Multi-phase interleaved converters were presented in (Chuang et al., 2015).

To increase the conversion ratio, delayed quadratic buck converters and semi-quadratic buck converters have been presented. However, these are for only DC-DC conversions with a high step-down ratio for low power applications (Veerachary, 2016). Switched capacitor-based quadratic buck converter was discussed, but the limitation of this topology has been an increased component count(Reyes-Malanche et al., 2015). If a non-cascading connection was used, high step-down topologies can be realized with reduced redundant power processing stages (Loera-Palomo et al., 2013).

3.3 Research Motivation

The topologies of QBC have been conventionally evaluated for low power and high step-down applications. Interleaved topologies were investigated for 400 W and higher power applications. Considering the ESR, size of the inductor, and capacitor, it was investigated and reported in (Shreelakshmi et al., 2018) that the buck converter operates at a very low efficiency of 40% when the duty cycle was 20%, and the efficiency increased to above 80% when the duty cycle reaches near to 50%. Hence, the proposed converter in this thesis is realized which is cascaded buck, which does not need very low duty cycle and hence efficiency would be improved. The present work investigates the performance characteristics of bridgeless / PFC QBC for a 150 W system.

3.4 Bridgeless QBC Topology

Figure 3.2 shows the proposed bridgeless QBC PFC topology. Converters need to operate at an extremely low duty cycle in applications that require a low output from higher input. Due to the limitation of the turn on / off of the devices, the switching frequency needs to be reduced, and hence the size of the inductors and capacitors become bulkier. It can be observed that compared to the conventional PFC of using a single inductor and capacitor at the input side, this system uses twice the inductors and capacitors, a disadvantage in terms of size and cost. At the same time, two inductors at the source yield better thermal performance, low EMI, and reduce the filtering requirement. The following assumptions are made while for analyzing the operating modes:

- The source is purely sinusoidal.
- The filter capacitors C_a and C_b are very small such that the voltage is discontinuous.
- MOSFET and diodes are ideal.
- Ripples in the inductor and capacitor are negligible.

To the *ac* source, a pair of inductors and capacitors are connected across the phase and the neutral for acting as an input filter. To this system, diodes are connected

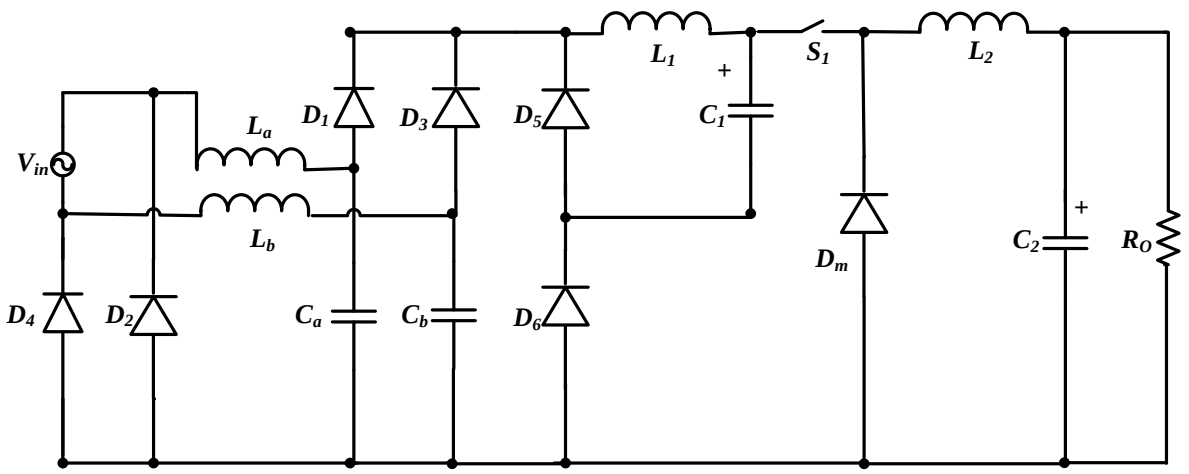


Figure 3.2: Bridgeless QBC with AC Source and PFC

which are conducting at high frequency of 50 kHz by the turn-on/ off action of the switch. When the switch is open, these high frequency diodes do not conduct and the current through the inductor gets interrupted. To avoid this interruption, a pair of diodes are connected providing a return path. The QBC stage has two LC filters, one active switch, and three passive devices. It can be assumed to be a cascaded stage of passive buck stage (L_1, C_1, D_5 and D_6) with an active buck stage (L_2, C_2, D_m and $S1$). During the positive line voltage cycle, the devices $L_a, C_a, D_1, S_1, L_1, L_2$ are active through the diode D_4, which closes the path. During the negative half cycle of the line voltage, the devices L_b, C_b, D_3, S_1, L_1, and L_2 are active through the diode D_2 for the circuit to complete. Due to the symmetry of the system, analysis of one-half cycle would represent the complete converter. The operating modes of the converter can be described as follows under the assumption of a constant input voltage over a cycle.

Mode 1: When the switch S_1 is closed, the freewheeling diode D_m and the diode D_5 are reverse biased by the source and do not conduct. The diode D_6 conducts as shown in Figure 3.3.

The current through the inductors i_{L1} and i_{L2} begins to rise. The current through the switch is the same as i_{L2}, and $i_{L1} = i_{L2} - i_{C1}$. The input filter capacitor C_a and the buck stage capacitor C_1 begin to discharge. The diode D_4 provides a return path to the source and conducts throughout the positive half cycle. Converter is considered to operate at a duty cycle of 'k', where f_L is the line frequency of supply and V_m

is the peak of the input supply voltage. In practice, the switching frequency f_S and hence the rectified input voltage can be considered as constant for a small interval of time denoted as V_{ac}. The voltage across the filter capacitor is denoted as V_{Ca}.

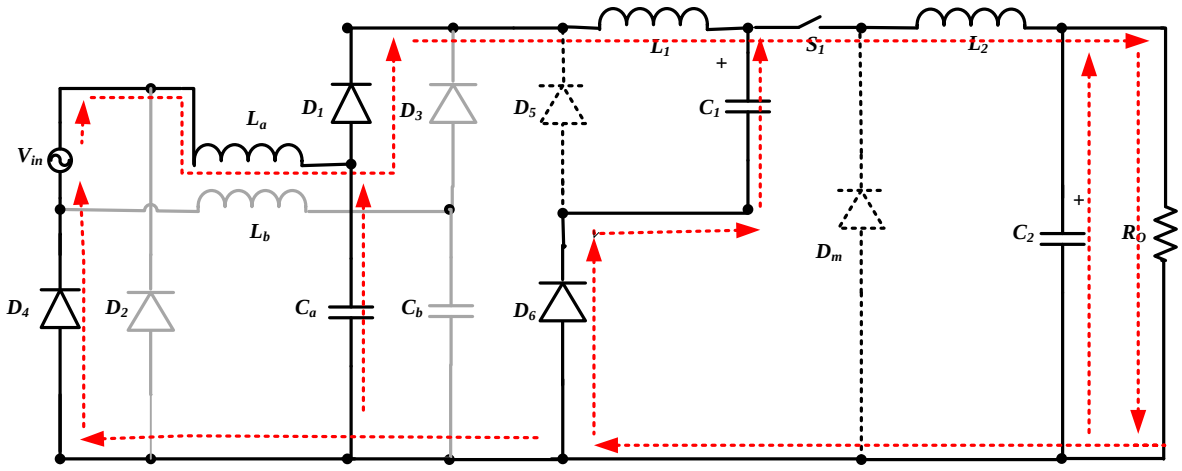


Figure 3.3: Operating mode of the converter with switch S_1 closed (Positive half cycle)

$$\left.\begin{aligned}
V_{\text{in}}\,(t) &= V_m \sin\left(2\pi f_L t\right)\\
\mathrm{V_{ac}} - \mathrm{V_{Ca}} &= \mathrm{L_a}\frac{d\mathrm{i_{La}}}{dt}\\
\mathrm{i_{La}} - \mathrm{i_{L1}} &= -\mathrm{C_a}\frac{d\mathrm{V_{Ca}}}{dt}\\
\mathrm{V_{Ca}} - \mathrm{V_{C1}} &= \mathrm{L_1}\frac{d\mathrm{i_{L1}}}{dt}\\
\mathrm{i_{L1}} - \mathrm{i_{L2}} &= -\mathrm{C_1}\frac{d\mathrm{V_{C1}}}{dt}\\
\mathrm{V_{C1}} - \mathrm{V_{C2}} &= \mathrm{L_2}\frac{d\mathrm{i_{L2}}}{dt}\\
\mathrm{i_{L2}} - \frac{\mathrm{V_{C2}}}{\mathrm{R}} &= -\mathrm{C_2}\frac{d\mathrm{V_{C2}}}{dt}
\end{aligned}\right\} \tag{3.1}$$

Considering the current through the inductors and voltage across the capacitors as state variables, $i_{La} = X_1$, $i_{L1} = X_2$, $i_{L2} = X_3$, $V_{Ca} = X_4$, $V_{C1} = X_5$ and $V_{C2} = X_6$,

The equation can be represented in state variable form as

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \\ \dot{X}_4 \\ \dot{X}_5 \\ \dot{X}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{\mathrm{L_a}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_1} & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ -\frac{1}{\mathrm{c}_a} & \frac{1}{\mathrm{c}_a} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{\mathrm{C_1}} & \frac{1}{\mathrm{C_1}} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{\mathrm{C_2}} & 0 & 0 & \frac{1}{R\mathrm{C_2}} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \mathrm{V_{ac}} \qquad (3.2)$$

Considering the voltage across the capacitor and current through the inductor L_1, The output equation can be written as

$$\begin{bmatrix} V_O \\ i_{L1} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} \qquad (3.3)$$

Mode 2: The operating mode of the converter when the switch is open is as shown in Figure 3.4. The energy stored in the inductor L_2 is discharged through the filter capacitor, the load, and the freewheeling diode D_m. The energy stored in the inductor L_1 charges the capacitor C_1 with a constant current. As the current through the inductor L_1 cannot be interrupted, the diode D_5 provides the path for the circuit. HenceD_1 and D_6 do not conduct. The energy stored in inductor L_a is transferred to the capacitor C_a through the path L_a, C_a, and the diode D_4, and the capacitor C_1 charges with the constant current i_{Ca}.

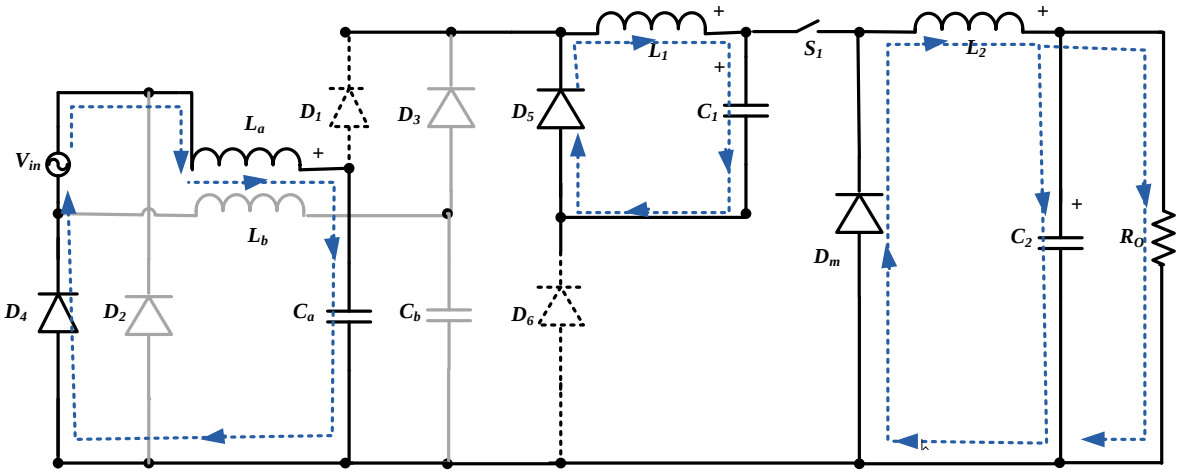


Figure 3.4: Operating mode of the converter when swith S_1 is open (positive half cycle)

$$\left.\begin{aligned} \mathrm{V_{ac}} - \mathrm{V_{Ca}} &= \mathrm{L_a}\frac{d\mathrm{i_{La}}}{dt} \\ \mathrm{i_{La}} &= \mathrm{C_a}\frac{d\mathrm{V_{Ca}}}{dt} \\ \mathrm{V_{C1}} &= \mathrm{L_1}\frac{d\mathrm{i_{L1}}}{dt} \\ \mathrm{i_{L1}} &= \mathrm{C_1}\frac{d\mathrm{V_{C1}}}{dt} \\ \mathrm{V_{C2}} &= -\mathrm{L_2}\frac{d\mathrm{i_{L2}}}{dt} \\ \mathrm{i_{L2}} - \frac{\mathrm{V_{C2}}}{\mathrm{R}} &= -\mathrm{C_2}\frac{d\mathrm{V_{C2}}}{dt} \end{aligned}\right\} \tag{3.4}$$

The equation can be represented in state variable form as

$$\begin{bmatrix} \dot{X}_1 \\ \dot{X}_2 \\ \dot{X}_3 \\ \dot{X}_4 \\ \dot{X}_5 \\ \dot{X}_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{\mathrm{L_a}} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{\mathrm{c}_a} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{\mathrm{C_1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{\mathrm{C_2}} & 0 & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \mathrm{V_{ac}} \tag{3.5}$$

Mode 3: When the supply voltage reverses and the switch S_1 is closed, the input current flows through L_b, D_3, L_1, L_2, filter capacitor C_2 and the load resistor R_O. Only the QBC input current shifts through the inductor L_b. Hence the quadratic

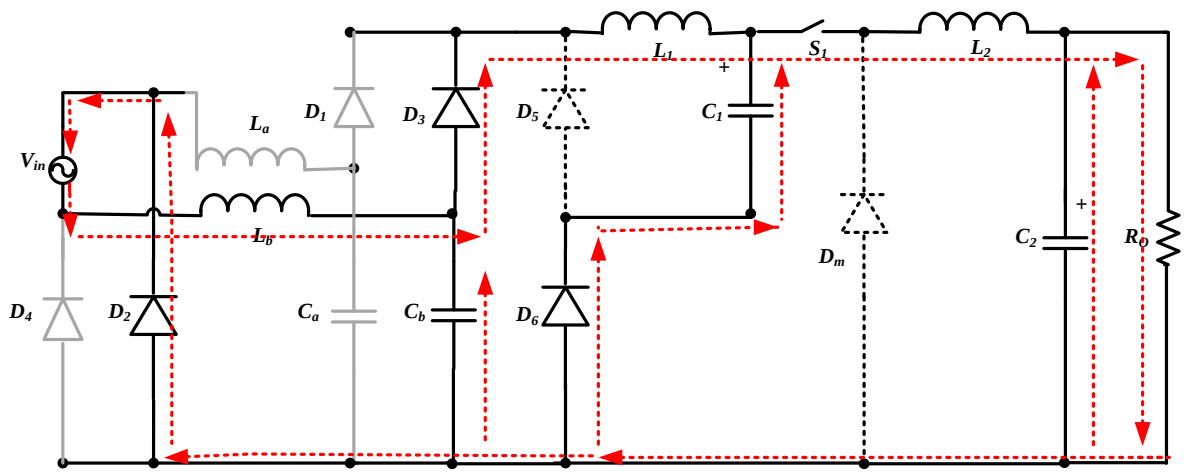


Figure 3.5: Operating mode of the converter when S_1 is closed (negative half cycle)

stage equations remain the same. The freewheeling diode D_m and the diode D_5 are reverse biased by the source and do not conduct. The diode D_6 conducts as shown in Figure 3.5. The current through the inductors $i_{L1}$and i_{L2} begins to rise. The current through the switch is the same as i_{L2}. The current (through the inductor L_1)$i_{L1} = i_{L2} - i_{C1}$. The input filter capacitor C_b discharges. The voltage through the capacitor begins to fall.

Mode 4: The energy stored in the inductor L_2 is discharged through the filter capacitor, the load, and the freewheeling diode D_m. The energy stored in the inductor L_1 charges the capacitor C_1. As the current through the inductor L_1 cannot be interrupted, the diode D_5 provides the path for the circuit. Hence D_3 and D_6 do not conduct as shown in Figure 3.6. The energy stored in inductor L_b is transferred to the capacitor C_b through the path L_b, C_b, and the diode D_2, and the capacitor charges with the current $I_{Lb} = I_{Cb}$. The cycle continues till S_1 is switched on again after the time T_s. D_2 provides a path for the return in the negative half cycle and conducts during the entire half cycle. D_1/D_3 switch at a high frequency, and therefore fast recovery diodes have to be used. D_2, D_4 switch at a power frequency which is 50 Hz for the proposed study. The operating current waveform across the various devices for the proposed prototype is presented in Figure 3.7.

When the switching pulse is applied, the current through the switch increases. The inductors L_1, L_2, and the capacitor C_2 begin to charge through the Diode D_1 and the switch S_1 as shown by rising $i_{ds}, i_{L1}, i_{L2}, i_{C2}$. When the pulse is withdrawn,

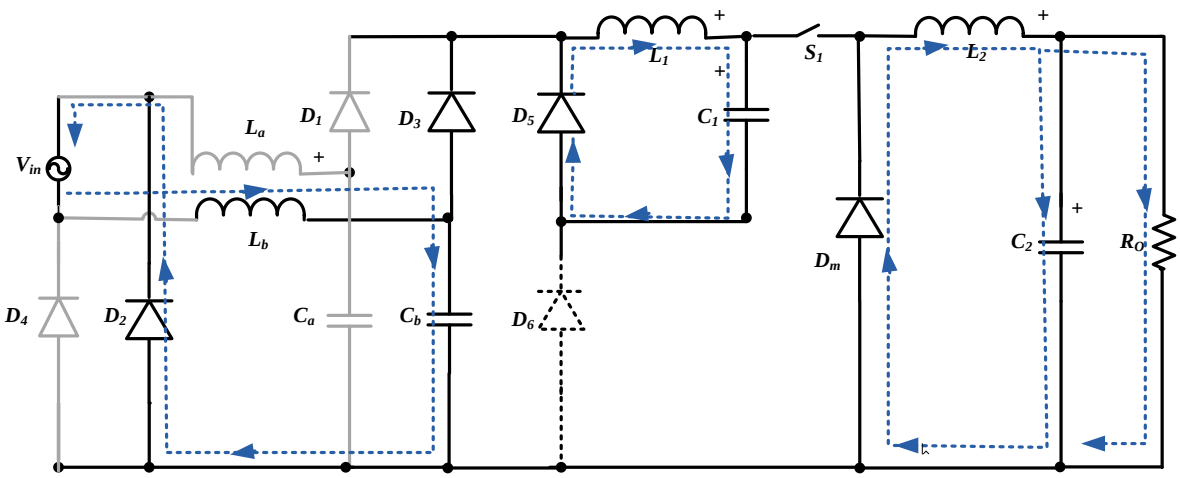


Figure 3.6: Operating mode of the converter when S_1 is open (negative half cycle)

the freewheeling diode begins to conduct, indicated by the i_{dm} rising. The inductors L_1 and L_2 begin to discharge, indicated by the falling i_{L1}, i_{L2}, i_{C2}. The QBC stage capacitor C_1 charges quickly through the diode D_5. The filter inductors L_a/L_b charge alternately during this mode. The operating modes as discussed, confirming to the simulation waveforms obtained.

The size of electrolytic capacitor in a conventional PFC using Boost converter with diode bridge-based rectification schemes is heavy. For step-down applications, single-stage buck conversion imposes the burden having to operate at 25% duty cycle. Here load side inductor would also be heavy, having to supply load current for 75% of the time. Hence losses will also increase, resulting in lesser efficiency. Whereas the present scheme has the advantage of offering high step-down ratio at a moderate 45% duty cycle. Hence filtering requirement is reduced. Rectifier stage electrolytic capacitor is eliminated. Requirement of costly sensors for close loop control is reduced compared to boost topology-based schemes. The inherent passive PFC takes care power factor correction and only output voltage/ current control will be required to be done. The size of the components also reduces, resulting in more economy and indirectly increase in efficiency, apart from the benefit of thermal cooling due to current sharing (similar to interleaved topologies). Further reduction is size can be obtained by increasing switching frequency, but due to the limitations of available components, frequency was limited to 50 kHz.

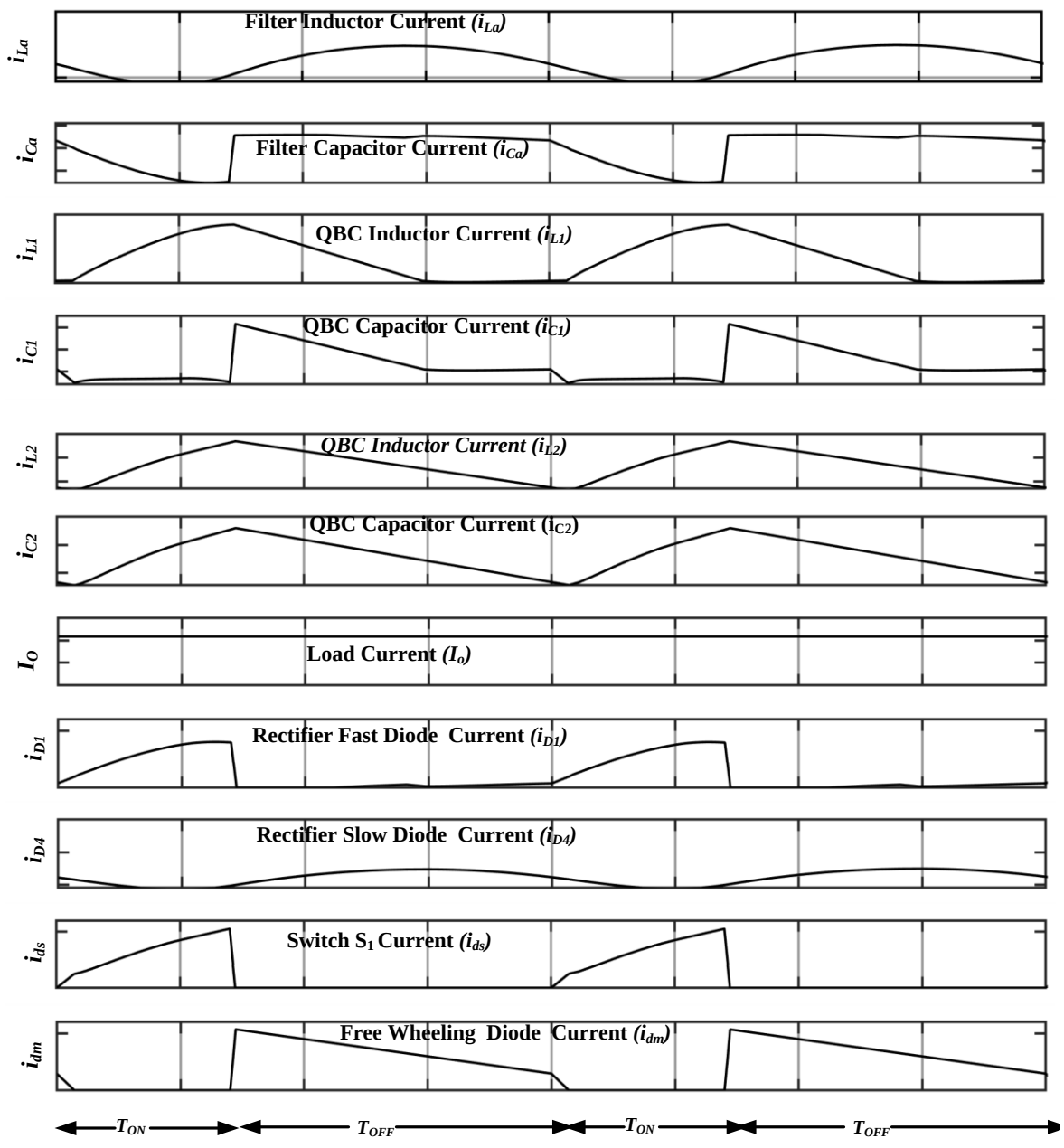


Figure 3.7: Key waveforms of the various components of proposed QBC PFC Converter

Table 3.1: Estimated Device Voltage and Current Ratings

Device	Estimated Value
V_S	207 V
V_{C1}	104 V
V_{C2}	52 V
I_{L2}	2.6 A
I_{L1}	1.3 A

3.5 Design of Components

Considering supply of 230 V_{rms}, 50 Hz, the rectified output voltage of a full-bridge is given by $(2Vm)/\pi$. As per the standards of IS 12360 (1988) , 10% voltage variation at the source side, the supply voltage varies between 207 V and 253 V. The corresponding *dc* voltage varies from 186 V to 227 V. Considering a 48 V battery charging application with a load current of 2.5 A, equivalent load resistance R_O is estimated as 20 Ω. The maximum power output is P_O is assumed to be 150 W. The relation between output and input for a quadratic converter is given by $V_O = k^2 * V_S$, where k is the duty cycle, and therefore $k = \sqrt{V_o/V_s}$. Assuming V_S as the rectified dc voltage, the voltage across the capacitors can be computed as $V_{C1} = k * V_S, V_{C2} = k^2 * V_S$. The load current $I_O = V_O/R_O, I_O = k^2 * V_S/R_O$, an average of the current through the inductor $L_2(iL2)$, is the same as the load current I_O, Therefore $i_{L1} = k^3 * V_S/R$. The duty cycle is minimum (0.45) when the output voltage is minimum and source voltage is at maximum (48, 227), and the duty cycle is maximum (0.55) when the output voltage is maximum with source voltage minimum (54, 186) Substituting the values, the theoretical limits of the duty cycle (k) vary between 0.45 to 0.55 and is assumed as 0.5 for computation. The average value of inductor current i_{L2} will be the same as that of the load current. The computed values with a moderate duty cycle of 50% are presented in Table 3.1

3.5.1 Design of Filter Capacitors

The filter capacitors (C_a, C_b) can be designed using the equations below. For the higher values of constant 'p', the capacitor current is continuous for a longer period of time, and the input current is distorted. For shorter values of 'p', there would be

higher voltage stress on the switch.

$$\mathrm{C_a, C_b} = \frac{\mathrm{pTs}}{2\mathrm{R_o}} \tag{3.6}$$

A value of p= 0.03 was considered for design. f_L is the line frequency of 50 Hz, and the switching frequency F_S is 50 kHz. C_a and C_b are estimated to be 15 nF from Equation (3.6). A 47 nF capacitor was used for the study based on the component availability. As the capacitors are subjected to voltage stress of $2V_m$, the Voltage rating should be above 650 V. The equivalent resistant it considered to be equal to load resistance for the purpose of design.

3.5.2 Design of Filter Inductors

There is LC loop with equivalent inductance L_e and C_a, and hence resonance can occur. In order to avoid resonance, the constraints to be met are represented though the Equation (3.7).

$$\left.\begin{aligned} &\mathrm{f_r} \ll \mathrm{f_S} \\ &\mathrm{L_{min}} \gg \frac{1}{\mathrm{C}}\left[\frac{(1-\mathrm{k})\mathrm{T_s}}{2\pi}\right]^2 \\ &\mathrm{L_{max}} \ll \frac{1}{\mathrm{C}}\left[\frac{(1-\mathrm{k})^2\ \mathrm{T_S}}{4\pi \mathrm{f_L}}\right] \\ &f_\mathrm{r} = \frac{1}{2\pi\sqrt{(L_e C_a)}} \end{aligned}\right\} \tag{3.7}$$

Substituting the values, the filter inductor can be estimated to be between 54 µH and 169 mH, and the resonating frequency of the equivalent inductance with filter capacitance is estimated as 13.3 kHz . The value of filter inductance used is 2.6 mH. The RMS value of source current at the input side is around 1 A, so that the filter inductor can be selected which can have a 2 A rating. It was observed that inductor ESR increases with an increase in switching frequency. To reduce the size of the inductor higher frequency is required. There could be losses due to the internal resistance of various components. Hence lower ESR components are desirable. The inductor was wound in lab using toroid core and the value of inductance and ESR is

measured with the help of LCR meter.

3.5.3 Design of QBC Inductors

Following the conventional buck converter, the inductor is designed using Equation (3.8), which gives a value of 384 µH for the continuous current mode. If the inductor L_1 operates in discontinuous mode, the component used was to be lesser than 384 µH, and the estimated value for L_2 is 190 µH. Duty cycle k_{min}= 0.45, the peak-to-peak ripple currents were limited to 3 A.

$$\left.\begin{aligned} \mathrm{L_1} &= \frac{\mathrm{V_{C1}(1-k)}}{\Delta \mathrm{i_L F_S}} \\ \mathrm{L_2} &= \frac{\mathrm{V_{C2}(1-k)}}{\Delta \mathrm{i_L F_S}} \\ \mathrm{L_1} &= \frac{104(1-0.45)}{3*50000} = 384\mu\mathrm{H} \\ \mathrm{L_2} &= \frac{52(1-0.45)}{3*50000} = 190\mu\mathrm{H} \end{aligned}\right\} \tag{3.8}$$

3.5.4 Design of the Output Capacitors

Using the output ripple constraints and the load power requirement from Equation (3.9), the critical value of capacitor C_c is greater than 763 µF. Considering the output voltage ripple ΔV_O as 10 mV.

$$\left.\begin{aligned} C_\mathrm{c} &= \frac{(1-\mathrm{k})}{16\ \mathrm{L_2 f_s}^2} \\ C_2 &= \frac{\mathrm{P_o}}{\mathrm{V_o \Delta V_o 4 f_s}} \\ C_2 &= \frac{150}{54*0.01*4*50000} = 1388\mu\mathrm{F} \end{aligned}\right\} \tag{3.9}$$

3.5.5 Diodes and Switch

The rectifier stage diodes are expected to withstand a peak input voltage of $2V_m$ and hence are rated above 650 V. There are two slow switching diodes at 50Hz, and 5 fast switching diodes at 50 kHz in the designed prototype. The voltage across the switch is desired to withstand $2V_m + V_O$. Though rectifier stage diodes have a low current rating requirement as the current drawn from the source is low, the QBC

Table 3.2: Parameter Values Used for Simulation and Experimental Study

Device	Component Value
L_a, L_b	2.6 mH,0.05 Ω (Toroidal core inductor, wound in lab and tested with LCR meter)
L_1	274-10L, PCV2 inductor, (270 µH, DC resistance 0.06 Ω, 7.2 A irms) (coil craft)
L_2	184-10L, PCV2 coil inductor(180 µH, DC resistance 0.048 Ω, 8 A irms) (coil craft)
C_a, C_b	0.047 µF, Wima capacitors, 1600 V_{dc}, 650 V_{ac}
C_1	Two electrolytic capacitors of 100 µF, and 400 V (series to obtain 50 µF, 800V)
C_2	Two 3300 µF Electrolytic capacitors, 200 V. (parallel to obtain 6600 µF).
D_1 - D_6 , Dm	MUR 880, 800 V, 8 A
Switch	(MOSFET)17N80C3 V_{ds}=800V, $R_{ds(on)}$ =0.29 Ω, $i_d = 17A$/ (IGBT15N120), $V_{ce} = 1200V, i_{ce} = 15A$

stage diodes have a higher current rating. As the entire inductor current is carried by these diodes during freewheeling operation, diodes of rating 8 A were chosen. The components are designed based on equations derived through available literature resources. While selecting components, the nearest values available in the laboratory were chosen, keeping the literature as reference.

3.6 Simulation and Experimental Results

3.6.1 Comparative results of Buck and QBC with DC Source

Advances in semiconductor technology have motivated the development of integrated circuits, which require 3.3 and 1.5 V power supplies. At the same time, the battery technology is upgrading from 12 V to 36/ 48 V systems. To obtain such low voltages, conventional DC-DC converters do not offer a high step-down ratio. The relation between the input and output of a conventional buck converter is given by $k = V_O/V_S$ where k is the duty cycle, V_O is the output, and V_S is the dc input voltage. When a wider conversion ratio is required, the conventional buck converter fails due to the limitation of the T_{ON} requirement of a switch.
As switching frequency increases, there exists a limitation due to the minimum duty

cycle of the switch. Quadratic Buck Converters satisfy the requirements. The quadratic converters can be Single-Stage(SS) or Multi-Stage(MS), isolated / non-isolated. SS conversion is always more efficient. An increase in the number of stages increase the components in the power path, and hence reduced efficiency apart from complexity in the control scheme. Quadratic converters have the relation of duty cycle as $V_O = k^2 V_S$.

To test the quadratic stage of the prototype, the simulation studies of the conventional buck converter and QBC as represented in Figure 3.1 were conducted using MATLAB / Simulink with parameters as shown in Table 3.1. A *dc* source of 30 V was used to apply a variable dc input voltage. A 20 Ω resistor was used as a load. The experimental and comparative results for the Buck and QBC are shown in Figure 3.8 depicts a higher step-down ratio for the same duty cycle. The duty cycle is varied from 25% to 50%, and the variation in output voltage for a conventional buck converter with QBC is plotted as shown in Figure 3.9.
The efficiency of the conventional buck converter was observed to be over 94% with a *dc* source. An extra stage of cascaded combination gives lower efficiency of 70% for light loads. Efficiency increases with an increase in load current. 5 V power supplies have applications with relays, mobile charging, stepper motors in 3D printers, robotics, and surveillance cameras.

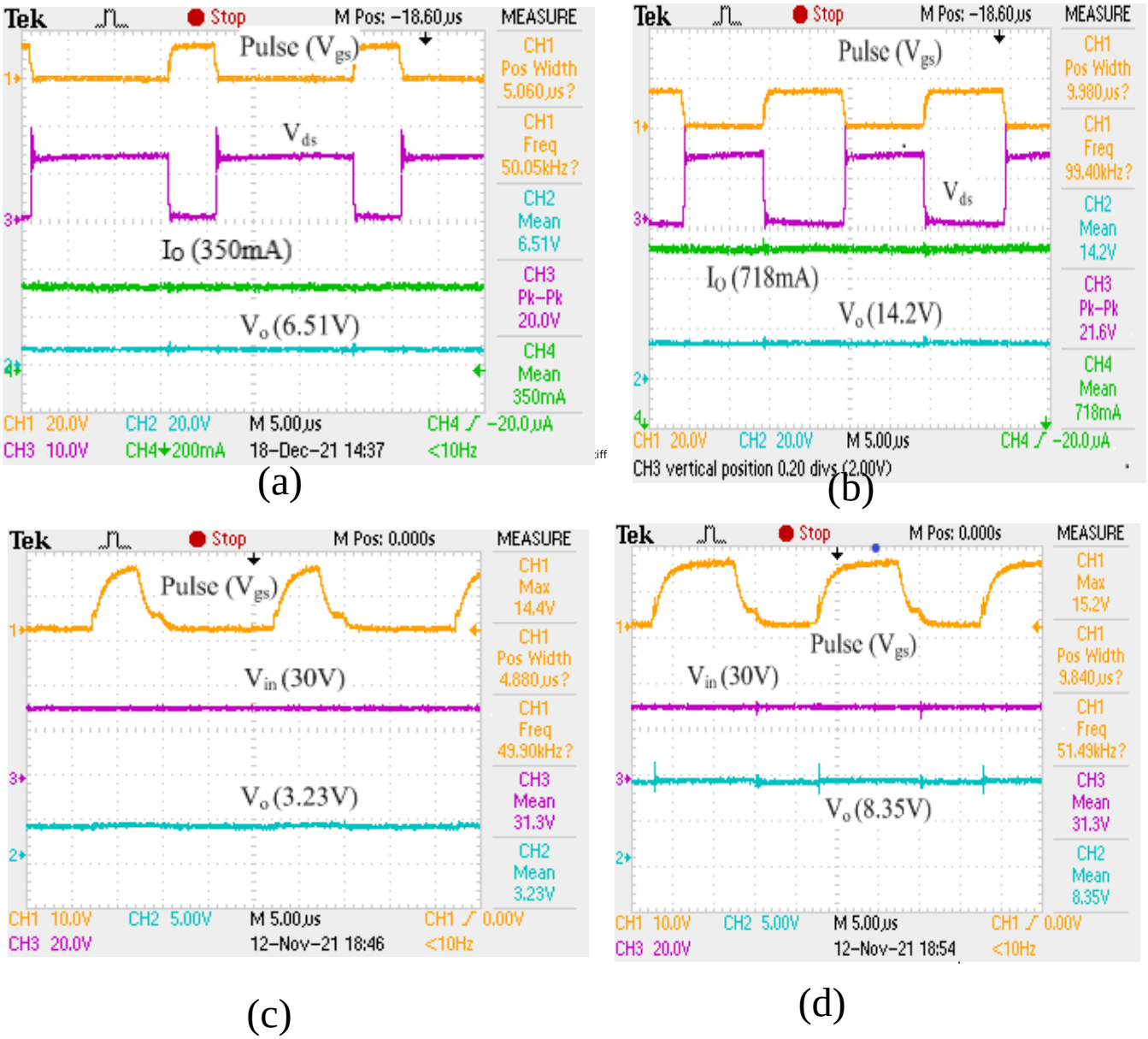


Figure 3.8: (a) Buck converter with 25% duty cycle(b) Buck Converter with 50% duty cycle(c) QBC with 25% duty cycle(d) QBC with 50% duty cycle

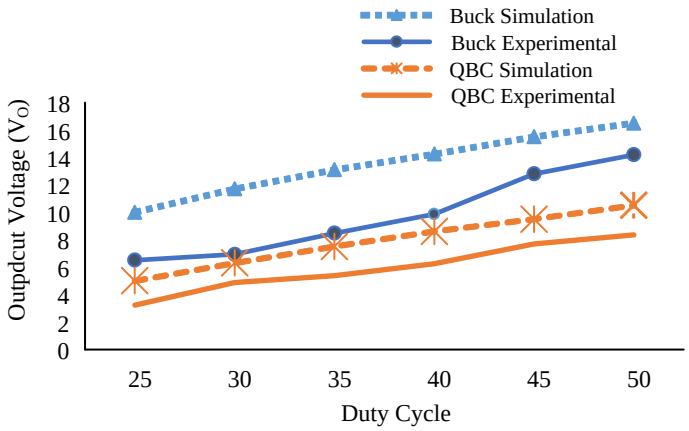


Figure 3.9: Comparative study of variation of output voltage with duty cycle

3.6.2 Simulation Results of QBC with AC Source

The circuits of conventional buck and QBC as shown in Figure 3.2 are simulated with parameters as presented in Table 3.2 using MATLAB R 2020b. Figure 3.10 shows the input voltage and the sinusoidal current drawn through the rectifier circuit, which indicates a higher power factor compared to the bridge rectifier circuit with a capacitive filter. The V, I stress of the switching device, and the freewheeling diode is not constant due to pulsating dc being applied. The source is varied from 30 V to 230 V. Figure 3.11 a indicates the V, I stress of the rectifier stage diodes. The fast diodes (D_1, D_3) are operated at 50 kHz as expected, and the slow diodes (D_2, D_4) operate at 50 Hz. Both the inductors charge and discharge together, as discussed in modes of operation indicated by Figure 3.11 (b). Inductor L_1 current is discontinuous, and this is due to the small size of the inductor. The voltage stress across the switch is also pulsating, and instantaneous stress of 400 V respresented by 3.11(c). 3.11(d) represents the voltage and current waveforms of the input filter capacitors C_a and C_b.

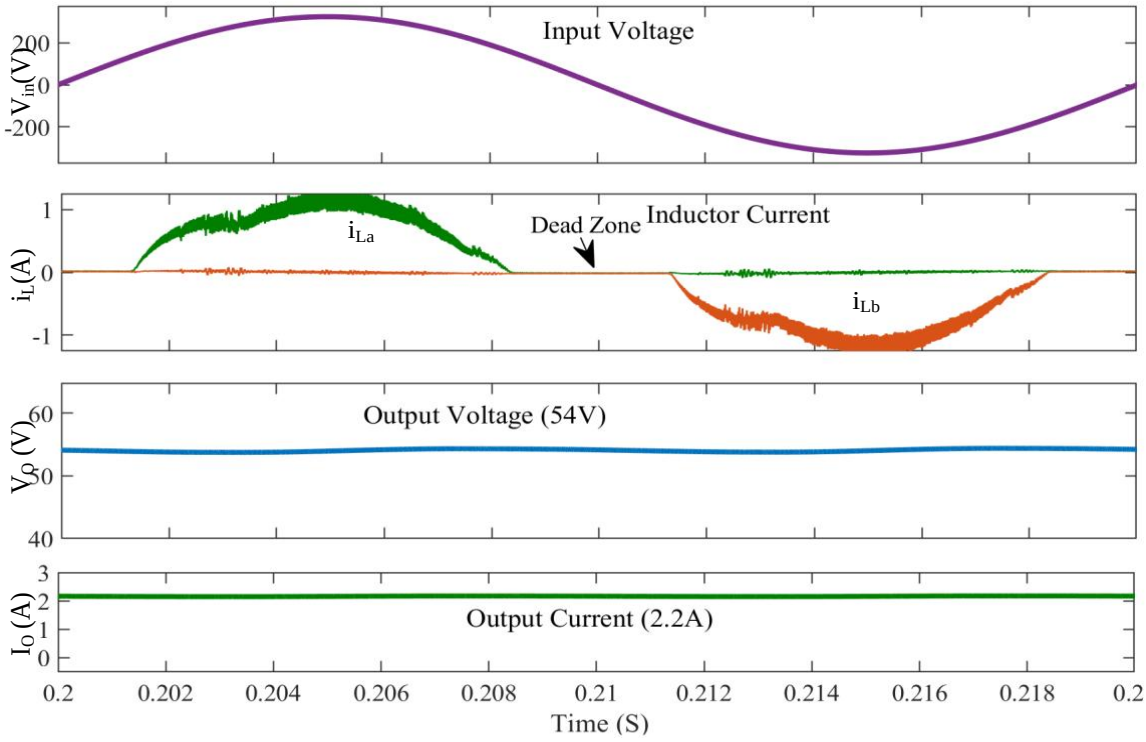


Figure 3.10: Simulation results of QBC with PFC for an AC input of 230 V at 35% duty cycle with output of 54 V and 2.2 A.

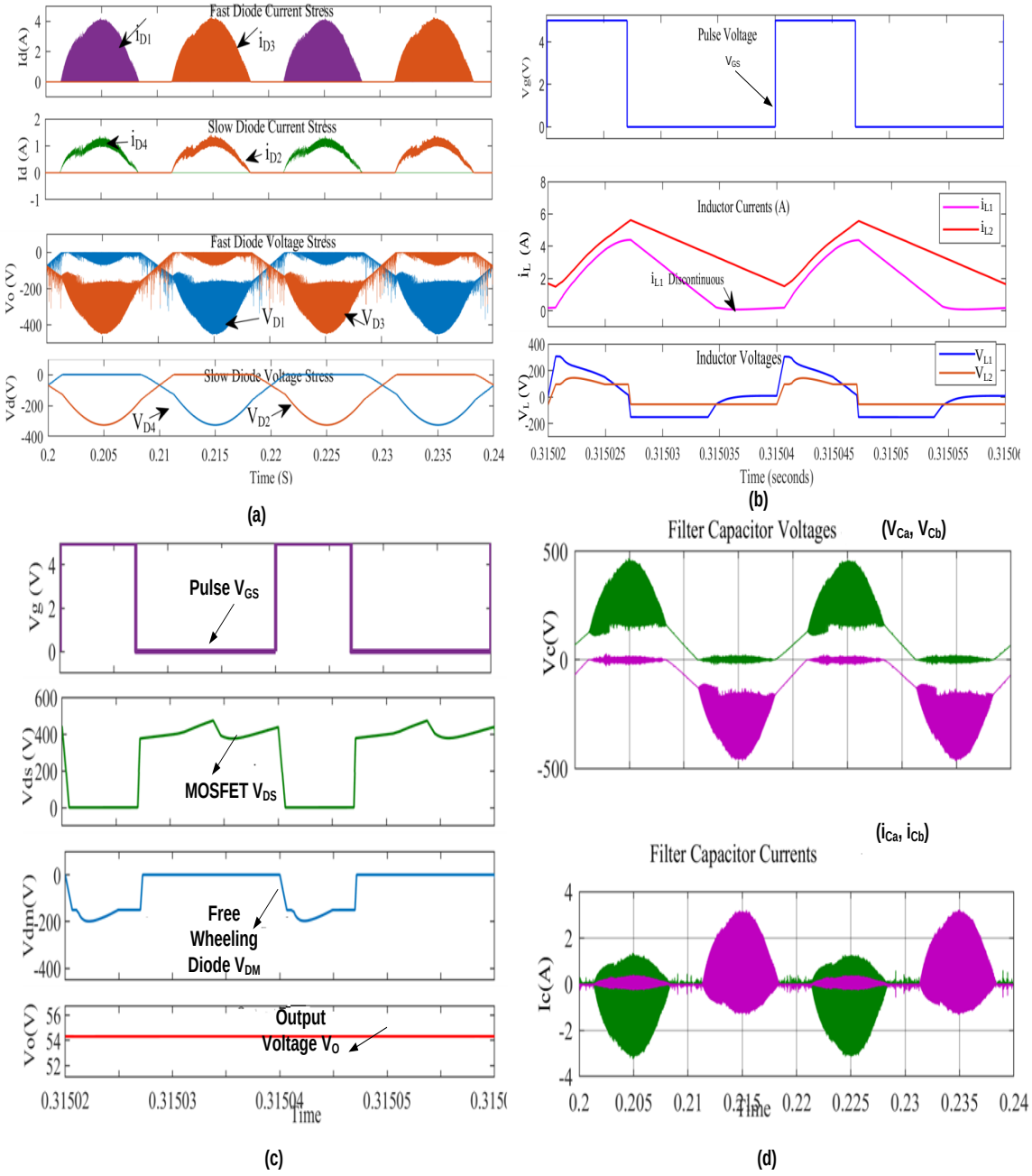


Figure 3.11: (a) Fast and slow diode stress(b) V,I across the QBC stage inductor(c) Voltage stress across the switch and freewheeling diode. (d) Input filter capacitor voltage and current

3.6.3 Hardware Results of QBC Converter

The experimental prototype is rigged up as shown in Figure 3.12. MATLAB is interfaced with a system generator tool for the transfer of logic. Previous working experience of Register Transfer Logic (RTL) is not required when the system generator is interfaced with MATLAB. Simulink block sets such as waveform generators and comparators can be used. It has 'gateway in' and 'gateway out' ports helping to transfer generated logic into a controller. An 'xpr' file is generated, which is further processed using Vivado design suite. This project is opened using the Vivado interface, and several steps such as block design, adding sources and sinks, selecting clock etc., are performed.The generated design is simulated, run, and implemented using the appropriate features available. Once the simulation runs smoothly, a bit stream is generated. This bit stream is transferred to FPGA using the hardware manager.

For the duty cycle generation, pulses are generated by using a comparison of a constant with a sawtooth wave of 50 kHz. The magnitude of 'constant' is varied to obtain pulses of 25 % to 50 % using a system generator for the MATLAB interface. These pulses were sent to the output ports of Basys3, which is an Artrix7- 35 T-based FPGA from Xilinx using the 'Vivado design suite' as the user interface. 'Pmod' ports $J_1, L_2, J_2, H_1, K_2, \& H_2$ are used as the output ports with each duty cycle assigned with the specific port for convenience and faster analysis. As the output of FPGA is 3.6 V, a MOSFET driver would be required. An isolator is required to help in the protection of the low voltage control circuit from high power load. TLP 350, an 8 pin opto isolator and driver is used to step up the pulses to 15V and drive the power switch in addition to offering isolation protection.

The embedded figure describes source voltage, load voltage, the voltage across the switch, and the freewheeling diode for a duty of 35%. The applied voltage is varied in steps of 20 V from 30 V to 230 V, and the variation in output voltage is studied. Figure 3.13 indicates the source current being sinusoidal and the power factor as estimated from the dead band between the voltage and the current is 0.89. The fast charge and discharge at 50 kHz operation of the switching diodes (D_1 and D_3), 50 Hz switching of the slow diodes (D_2 and D_4), the filter capacitor voltages, and the inductor current are illustrated in Figure 3.14. Figure 3.15 depicts the output voltage (with a QBC converter giving a low voltage of 54 V at a medium-duty of 50%), the voltage across

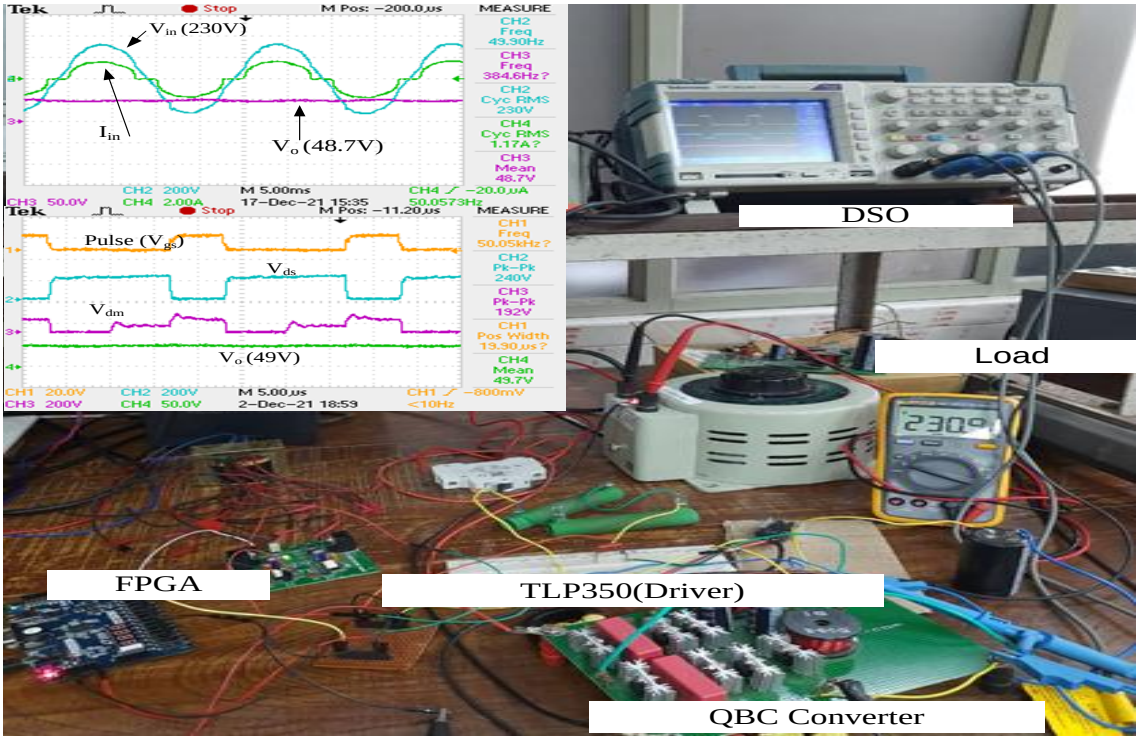
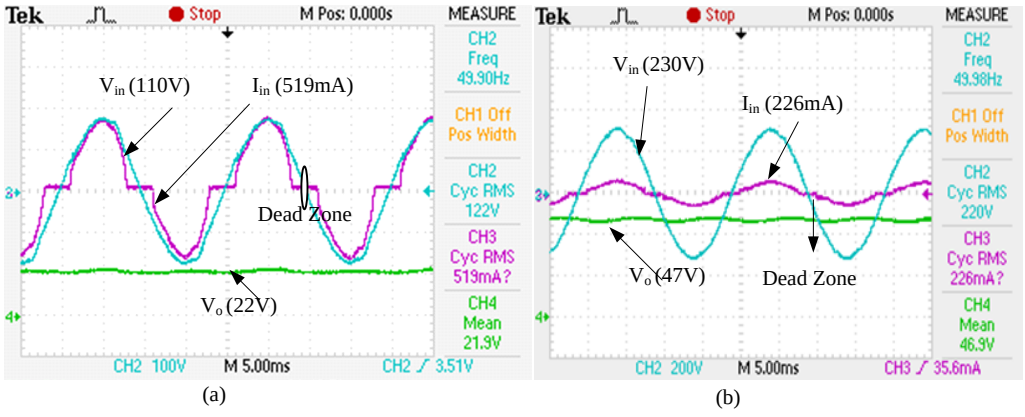


Figure 3.12: Prototype rig up for QBC with PFC converter with AC 230 V input and 48 V DC output



(a) (b)

Figure 3.13: AC Source voltage and current waveform(a) 110 V input voltage. (b) 230 V input voltage.

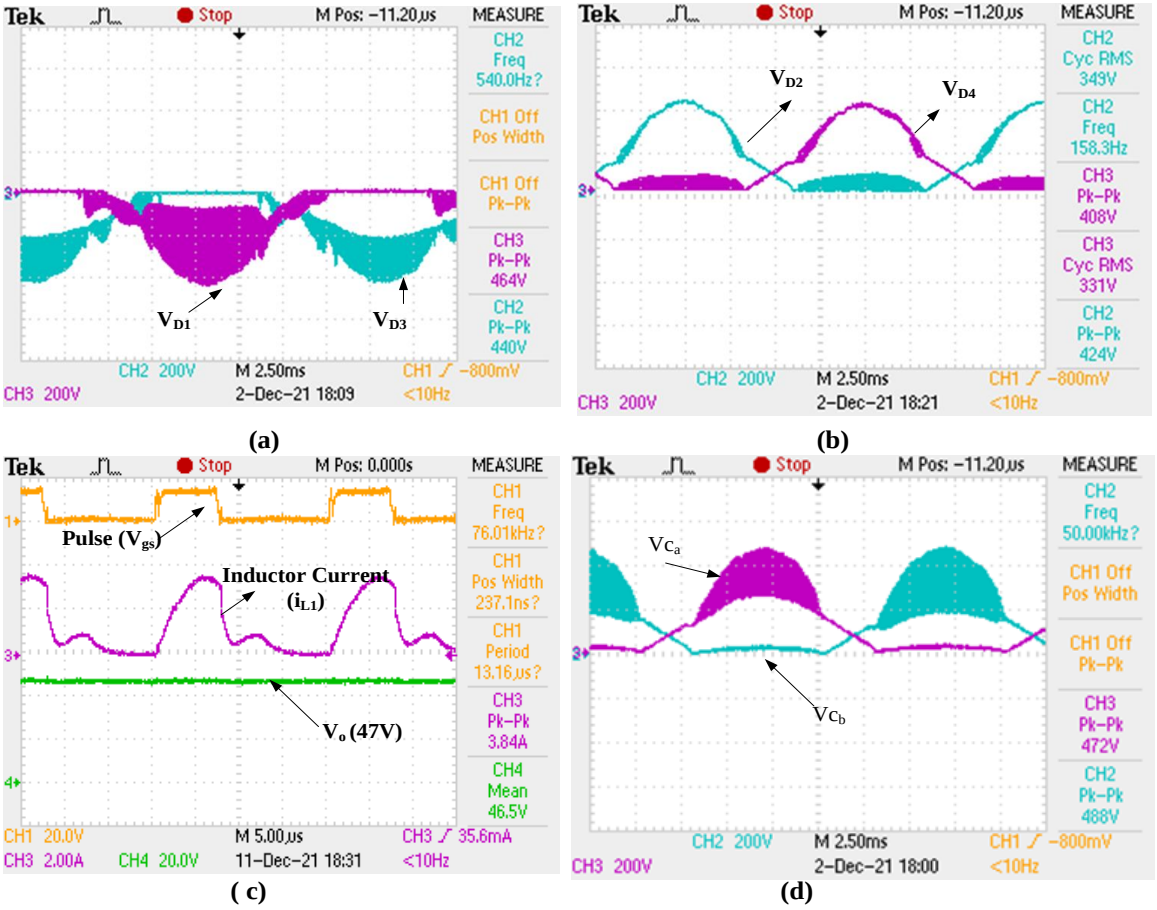


Figure 3.14: Rectifier stage fast diode stress. (b) slow diode voltage stress. (c). Inductor current. (d). Voltage across the filer capacitors

the switch (V_{ds}), load voltage, and current for the 150 W application QBC stage inductor L_2 was not accessible for the current measurement. Figure 3.16 presents the comparative results between the simulation and the experimental observations.

The representative hardware results are in confirmity with the modes of operation as discussed and observed with simulation study results. Voltage stress across the switch is observed to be high due to DICM with passive PFC topology and selection of the small size of inductors. For a 150 W operation, peak stress was observed to be over 740 V, and it increases with an increase in the load currents. Protection was incorporated by using an RCD snubber. As the MOSFET samples were limited in number and IGBT was compatible at the switching frequency, it was used at a later stage. There is a difference in the simulation and practical results beyond 35%.

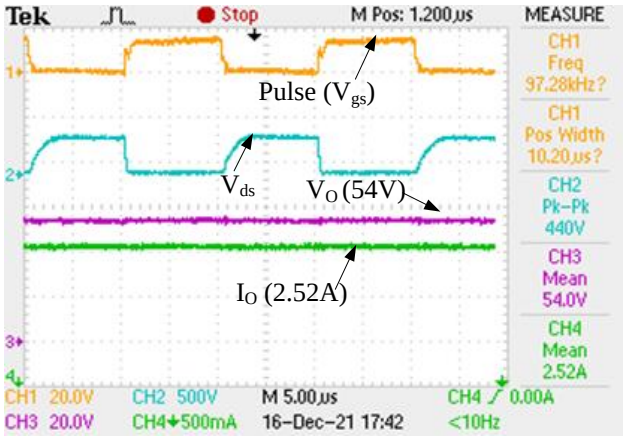


Figure 3.15: Experimental results of QBC with PFC for an AC input of 230 V at 50% duty cycle with output of 54 V and 2.2 A.

For a moderate duty cycle of 25% to 35%, the results show a linear relationship, and thereafter the simulation and hardware results deviate. With a higher duty cycle, there is a higher current being drawn from the source, resulting in higher I^2R losses across the series resistance of the components, inductors, and capacitors. As the resistance increases with frequency for inductors, the additional loss could have resulted in a lowered voltage at the load side. It was observed that the ESR of the inductor core is not constant but increases with the frequency of operation, which could have led to the difference in the simulation and hardware studies.

3.6.4 Comparative Evaluation of PFC Converters (Buck Converter versus QBC)

The hardware circuit of the Buck converter was rigged up, and the output of the rectifier stage PFC was connected to compare the conventional Buck circuit with the proposed QBC topology. It was observed that the switching capacitors exhibited DCVM as against CCVM in the QBC converter. The stress of the capacitors was around 324 V at 110 V_{rms} source, increasing to beyond 510 V at 200 V_{rms}. Figure 3.17 presents the variation of output voltage with load. Load resistance is varied to study the nature of output voltage variation with load. There has been a decrease in voltage. Figure 3.18 presents the experimental results with the variation of output voltage with

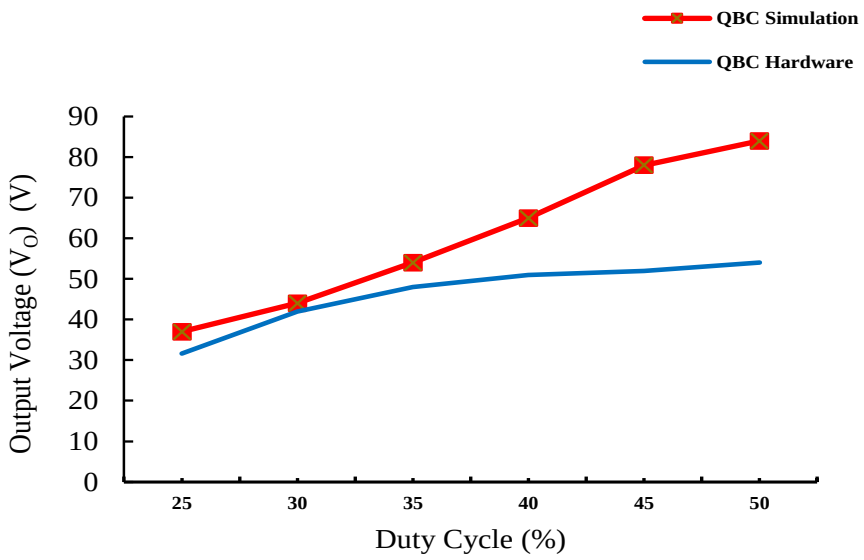


Figure 3.16: Comparative study of variation of output voltage with duty cycle for QBC with PFC

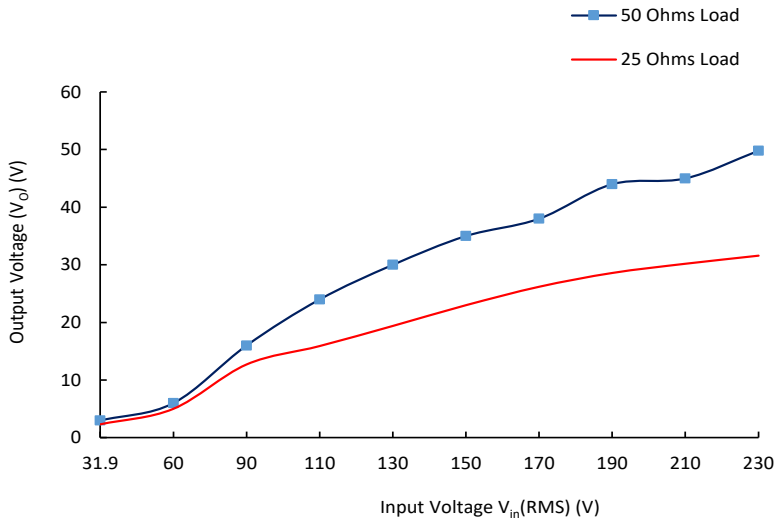


Figure 3.17: Comparative study of variation of PFC -QBC with load

duty cycle from 25% to 35% for both QBC and conventional buck converter for a load of 20Ω. The experimental results indicate the variation of output voltage for QBC topology but lesser response with a change in duty cycle in buck converter-based system. This shows a better control of load voltage by the proposed QBC scheme.

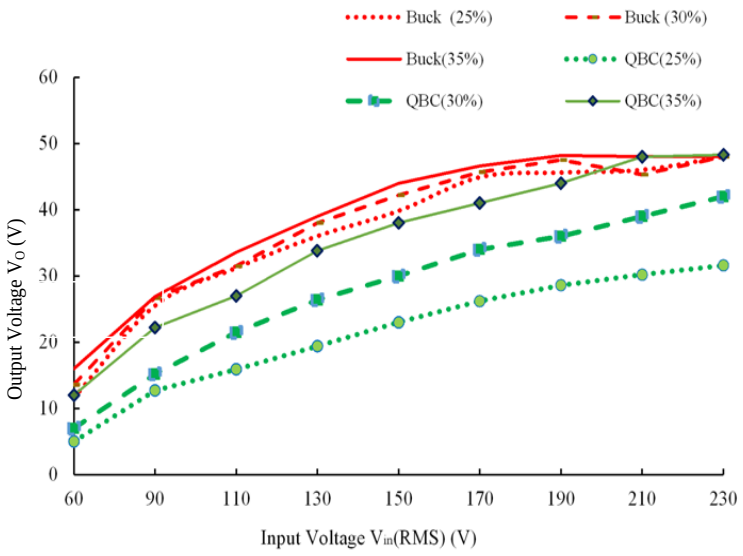


Figure 3.18: Comparative study of variation of output voltage for the conventional buck and QBC with PFC

Table 3.3: Comparision Studies of High Step-Down Topologies

Ref*.	Topology	No. of Switches	Diodes	Inductors	Capacitors	Efficiency %	Conversion Ratio	Remarks
A	QBSR PWM	3	4	4	4	91	180 /60 V	DC-DC
B	BB-QB SS PFC	1	9	4	3	83	85/5 V	Low power (20 W), High component count
C	Bridgeless flyback	2	3	Flyback	1	90	(110-220) V/ 48 V	(3 winding) power factor of 0.92. 50 W application (48 V,1 A) (AC-DC)
D	Bridgeless Cuk- 'Flyback	3	5	Flyback along with 4 normal	4	55 -90	(160-260) V/ 48 V	At 125W efficiency is 55%, 90% at 900W (Motor)
E	Boost buck cascaded	2	5	3	3	94	110/ 216	60 W (Led application)
F	Interleaved transformer- -less	4	2	2	5	93	400/ 25 V	(DC-DC Conversion)
G	QBC PFC	1	7	4	4	80	230 /54 V V	150 W

*A (Pacheco et al., 2000)

B (Al-Saffar et al., 2009)

C (Mok et al., 2011)

D (Kushwaha and Singh, 2019a)

E (Chang et al., 2015)

F (Pan et al., 2014)

G work in present chapter

Comparative studies with existing literature as described in Table 3.3 indicate that conventionally QBC was used for low power, high step-down applications. The existing literature survey indicates most of the topologies offer a lower efficiency for low-power applications, and efficiency increases with an increase in the rated power of the application. The presented prototype offers an alternative with a reduced number of switches and a comparable efficiency. Hence, the proposed high step-down ratio converter facilitates improved efficiency as the individual stages switch at a moderate duty cycle of 45% whereas due to the cascaded stage, the desired high step-down voltage ratio is obtained by the proposed converter.

3.7 Summary

A modified power factor corrected quadratic buck converter is proposed and described in this paper. The prototype of 150 W was rigged up in the laboratory and tested. The different operating modes of the operation of the converter are discussed and presented. The proposed converter has the benefit of single switch operation and reduced component counts comparable with the existing literature. The presented topology offers an improved power factor of over 0.89 at 110 V and 0.95 at 230 V. The study of variation of the output with variation in load, duty cycle and source were carried out experimentally, and the results are presented. The efficiency of the converter was observed to be over 80 %. By using low ESR components and better assembly techniques, the efficiency could be further improved.

Comparative studies of conventional and quadratic buck topologies for dc loads is conducted and presented. Though conventional buck operates at a higher efficiency due to the reduced total number of components, quadratic topology offers a higher step-down ratio for a moderate duty cycle with equivalent components in the power path. The proposed converter is suitable for 24 V - 48 V dc power requiring applications such as small motors and UPS/ battery charging applications. It provides a high step-down voltage ratio and inherent power factor correction. The present work focussed on open loop control and investigated for power applications of 150 W. The study indicates higher stress on the switch during commutation with increasing load power. A passive RCD clamp was used for the reduction of the same. Further work is required in exploring close loop control with emphasis on stress reduction on switch.

Chapter 4

PSO Algorithm Implementation

Contents

4.1 Introduction

This chapter presents hardware construction and testing of portable device, which reconverges faster with change in irradiance and under partial shading condictions. Conventional MPPT implementations utilize algorithms that read PV panel voltages, currents, and then calculate the maximum power available at in that particular time.

The Perturb and Observe (P&O) method needs a periodic sweep along the power curve to detect the maxima(can be local or global). The time taken to converge at MPP is significant, and thus the efficiency of conversion is drastically reduced. This work incorporates Particle Swarm Optimization (PSO) technique in replacement with the traditional P&O method to enhance the tracking speed and ensure the global maxima is achieved. In PSO technique, multiple search elements are introduced and a quantitative decision is evaluated among these search elements, and thus the convergence speed is increased by a factor of the number of elements used in the search. The hardware construction is compact and reliable, enhancing its application in various fields like unmanned aerial vehicles for long endurance The simulation studies were conducted on MATLAB / Simulink, and hardware design of the same was implemented. Contributions were made in finding practical testing and validation procedures for customized MPPT devices.

4.2 Research Background

Extracting the electrical energy from PV source is one of the way of generating electric power by tapping the solar energy. Since the efficiency of solar panel is low, the system needs to maximize the energy generated. For all variations in the temperature or solar irradiation the PV current and power are changed, thus changing the new point of operation. The use of an optimal MPPT algorithm will result in the extraction of maximum power under standard conditions. Temperature and irradiation are the major factors on which this maximum power depends.In case of partial shaded conditions, several MPP's occur on the P-V curve. Therefore, a Global MPPT (selecting the global maxima) algorithm is required. There are many techniques that are straightforward and easy to implement, but they cannot track the global peak under all operating conditions which involve dynamically varying irradiation and temperature. Researchers implemented many algorithms with the aim to track the MPP with smallest possible time . PSO algorithm was used to be much more efficient in tracking single and multiple peaks faster and accurately (Obukhov et al., 2020), (Sangrody et al., 2024). Number of algorithms were reported in literature describing the implementation challenges and tracking of MPP under partial shaded conditions (Koad et al., 2016), (Dutta et al., 2017).

Comparative evaluation of MPP tracking techniques was discussed(Rezk et al.,

2017). Mathematical modelling of PV arrays and implementation in MATLAB based environment was dicussed (Nguyen and Nguyen, 2015). The P&O method needs a periodic sweep of the duty (search element) from 0 % to 100 % (upper bound). The time taken to converge to MPP is significant, and thus the efficiency of conversion is drastically reduced(Brunton et al., 2010). If the perturbation is small, oscillations are reduced at the result of reduction in speed. If there is a rapid variation in insolation, the conventional P&O algorithm fails to track. Incremental conductance,adaptive pertubation, fuzzylogic, Artificial neural network based controllers are proposed in literature but these controllers have limitation of extensive computation requirements(Alajmi et al., 2010).

In the present study, a modified PSO technique is implemented using Arduino based controller, wherein the introduction of multiple search elements results in improvement in the convergence speed. MATLAB-based simulation studies were conducted along with hardware implementation of the proposed scheme.

4.3 I-V Characteristics of PV Panel

The current (I)-voltage (V) characteristic of the PV panel is non-linear in nature. Figure 4.1 shows the I-V characteristics of a typical silicon PV cell operating under normal conditions. The power graph is obtained by instantaneous multiplication of voltage and current and thus a MPP is located.

4.3.1 Effect of Partial Shading

In order to get the required voltage and power output PV modules are connected in series. Since many modules are connected in series and parallel, it has a large surface area. It is more likely to be shaded by objects that pass or stay nearby or even by the clouds. Shading results in the reduction of the output voltage and maximum power as described in Figure 4.2, heating of cells (creating local hot spots), and also causing damage to devices due to fluctuations caused by the movement of shading objects. In order to prevent the damage created to cells by hot-spots, a bypass diode is generally connected in parallel with the PV module so that the current is bypassed through the diode, and it is to be noted that the net output power from the module which is passed is zero. Therefore it is essential to have a robust algorithm to find

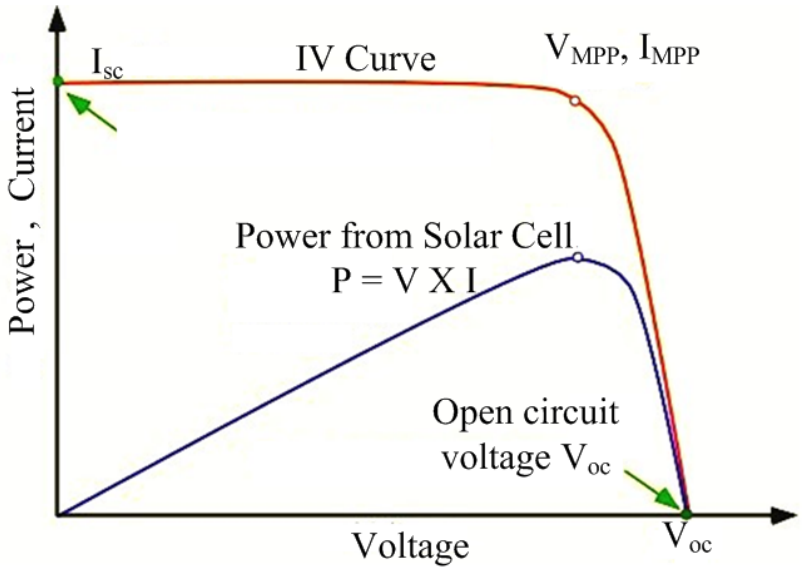


Figure 4.1: Current voltage (I-V) curve and *MPP* of a solar PV panel

the global peak both efficiently and accurately by finding the best available operating point. Thus the output power from the panel is maximized under all circumstances. Perturb and observe algorithm was used conventionally, and the required output was obtained, P&O was able to track the MPP, but when solar cells have partially shaded, the algorithm couldn't track the MPP as there were multiple peaks, and the algorithm was stuck among any one of the peaks.

4.3.2 PSO Algorithm

The PSO algorithm contains search elements that search for the local optimum solution and exchange their status and data with other existing search elements, and finally, all the search elements converge at the global optimum solution. The modified algorithm for PSO implementation is shown in Figure 4.3. In this model, there is a need to find the duty at which the buck converter should operate, which in turn extracts the maximum power from the panel and delivers the same to load. Here the calculation of the velocity plays a vital role in the algorithm. The duties are updated in such a way that the convergence is met faster. In order to ensure that they drift towards the global MPP accurately, we use the following expressions.

$$V_{i+1} = w * V_i + c_1 * r_1(P_b - X_i) + c_2 * r_2(G_b - X_i) \tag{4.1}$$

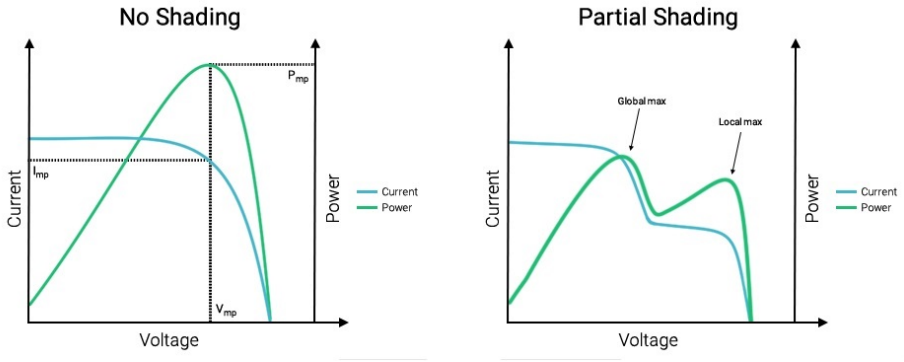


Figure 4.2: Current voltage (I-V) curve and *MPP* of a solar PV panel under partial shading

$$X_{i+1} = X_i + V_{i+1} \tag{4.2}$$

$V_{i+1} \rightarrow$ modified velocity
$V_i \rightarrow$ previous velocity
$c_1, c_2 \rightarrow$ acceleration constants
$r_1, r_2 \rightarrow$ random number between 0 and 1
$P_b \rightarrow$ personal best of search element
$G_b \rightarrow$ global best of all search elements
$X_i \rightarrow$ current position of search element
$X_{i+1} \rightarrow$ modified position of search element

4.3.3 Buck Converter Construction

The buck converter is a basic dc-dc step-down converter represented in Figure 4.4. Here the converter is designed using conditions such as maximum input and output voltages, currents, and the ripple constraints using expressions obtained theoretically. The converter components are designed for a 100 kHz frequency of operation and are presented in Table 4.1.

$$L = \frac{(V_{IN} - V_{SW} - V_{OUT}) * (V_D + V_{OUT})}{(V_{IN} - V_{SW} + V_D) * F_S * I_{rip}} \tag{4.3}$$

$$C_{IN} = \frac{(1 - \frac{V_{OUT}}{V_{IN}}) * I_{O(MAX)*V_{OUT}}}{F_S * \Delta V_{IN} * V_{IN}} + (1 - \frac{V_{OUT}}{V_{IN}}) * I_{O(MAX)} * ESR * V_{PP} \tag{4.4}$$

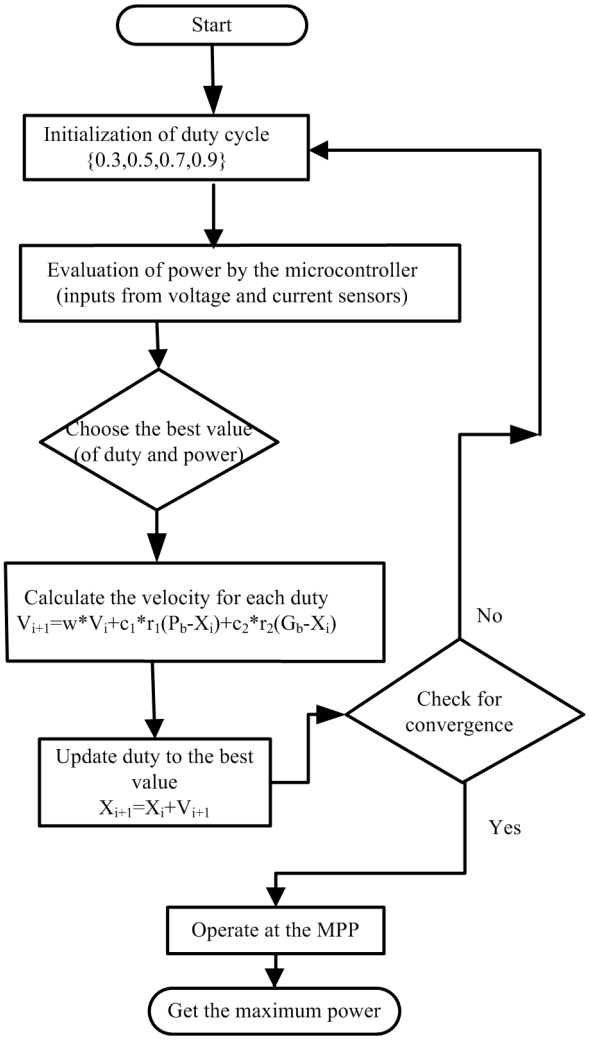


Figure 4.3: Flowchart of the PSO Algorithm

$$C_{OUT} = \frac{I_{RIP}}{8 * F_S * (V_{rip} - \frac{ESL*V_{INmax}}{L} - (I_{RIP*ESR}))} \tag{4.5}$$

$L \rightarrow$ Inductance.

$C_{IN} \rightarrow$ Input Capacitance

$V_{IN} \rightarrow$ Input Voltage

$V_{SW} \rightarrow$ Forward voltage drop of switch

$V_{OUT} \rightarrow$ Output voltage

$V_D \rightarrow$ Forward voltage drop of diode

$I_{rip} \rightarrow$ Output current ripple

$F_S \rightarrow$ Switching frequency

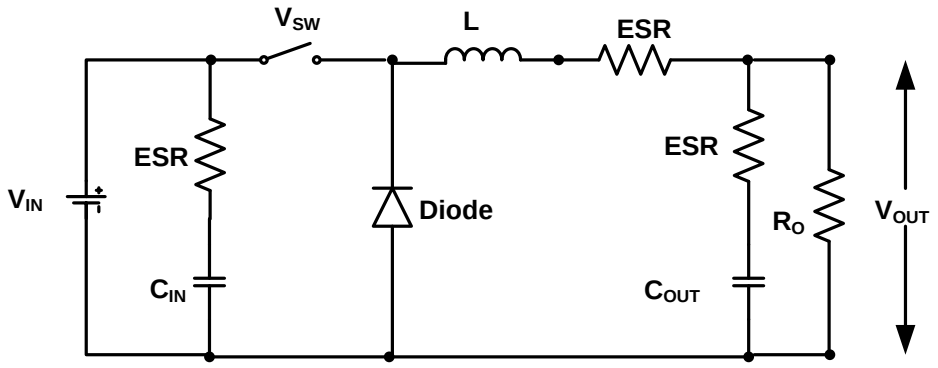


Figure 4.4: Schematic of conventional buck Converter

Table 4.1: Buck converter component values

Parameter	Value
L	189 µH
C_{IN}	20 µF
C_{OUT}	978 µF
V_{IN}	(17 -30) V
V_{OUT}	(16-24) V

.

4.4 Hardware Setup

Measurement of current was done using ACS712, the current sesing module, which comes with a precise, low-offset, linear Hall sensor circuit with a copper conduction path. A proportional voltage is created to the magnetic field generated due to the flow of current through the copper conduction path. This voltage is fed to the microcontroller with an appropriate multiplication factor based on the sensitivity of the module. Voltage divider principle was used to measure the voltage. The maximum voltage that can be measured was set to 30V and the resistor values were calculated accordingly. Since micro controller can only take signals less than or equal to 5V. So here 5V to micro controller corresponds to 30V at the panels.

$$V_{Measured} = V_{in} * \frac{R_1}{R_1 + R_2} \tag{4.6}$$

Considering V_{inmax} =30 V , $V_{Measured}$ = 5 V. The value of resistors is calculated through Equation (4.6) and are 60 k Ω and =300 k Ω respectively. The PWM pulses from the microcontroller have low current levels, which is not sufficient enough to drive the MOSFET, and hence IR2110 IC is used to drive the high side MOSFET of the buck converter. Higher the gate current faster will be charging and discharging of the gate capacitance of MOSFET and thus faster is the turn ON and OFF time. The voltage and current sensor output was first fed to the 16 bit ADC ADS1115 as shown in Figure 4.5. The ADC module has a high sampling rate. Hence the MPP

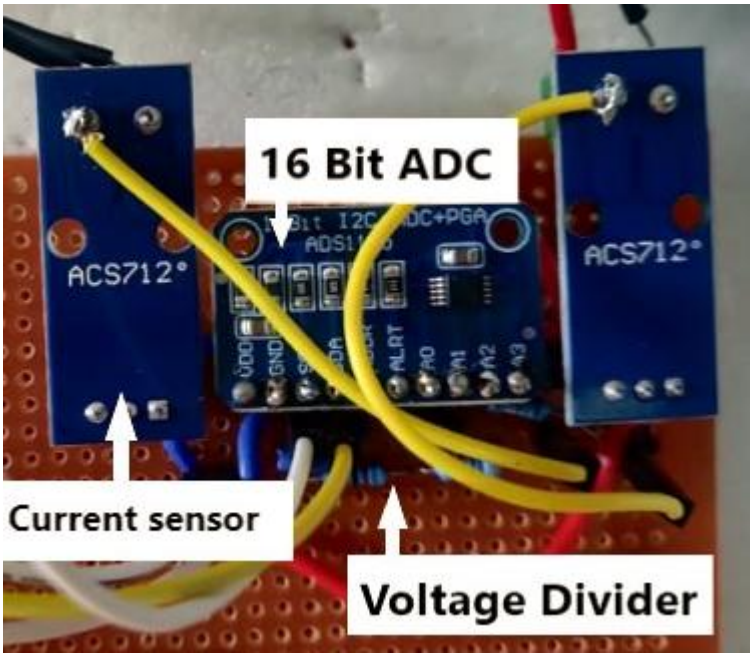


Figure 4.5: Current sensor and voltage divider system to measure power

tracking efficiency is increased. The values of the components are chosen 25% higher than the obtained values to ensure proper operation of buck converter in continuous conduction mode. The experimental setup is shown in Figure 4.6 The driver's output is connected to respective gate terminals of high and low side MOSFET. The solar panel is connected to input terminal and the load is connected to the output terminal. The Individual modules were integrated as shown in the Figure 4.7. The connections

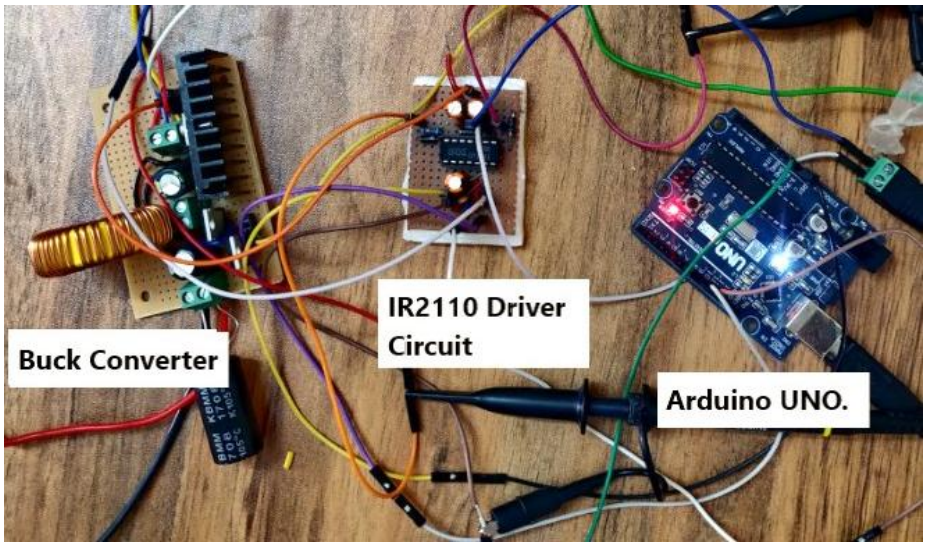


Figure 4.6: Prototype model of Buck converter with Arduino controller and Driver

were checked and it was proceeded for many test cases to ensure the functionality.

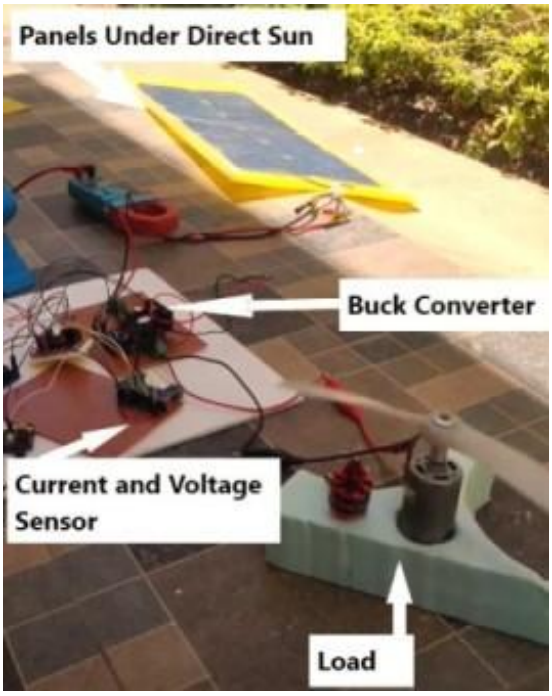


Figure 4.7: Experimental setup for variable duty cycle (10% to 95%)

4.5 Testing & Results

Necessary arrangements were made to conduct the following experiments, using a cardboard sheet for shading purposes, and serial plotter tool to plot the instantaneous data from the microcontroller. The following three basic and important tests were performed

- Peak detection verification
- Global peak detection (Partial Shading)
- Normal operation to sudden shading

4.5.1 Peak Detection Verification

The test was performed with power resistors (1.67 Ω, 40 W static load), and Arduino code was written such that the converter's duty cycle was changed from 0.1 to 1 in steps of 0.001. A constant load is connected to the buck converter output terminal, and the duty cycle is varied from 0.1 to 1. The power data from the panel is stored and plotted. The process is repeated 3 to 4 times to ensure the accuracy of the data. After the PSO algorithm is deployed to the microcontroller, the algorithm

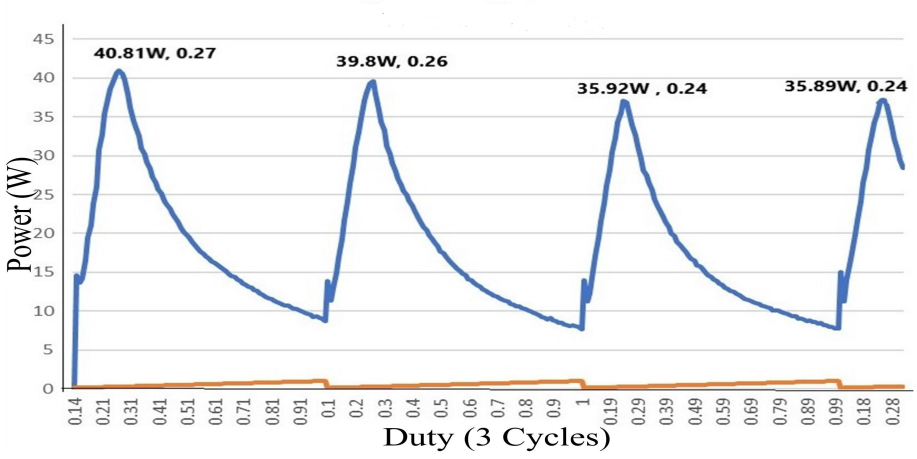


Figure 4.8: Duty sweep from 10% to 95%

will converge at a point, and the value is compared with the duty value obtained at MPP. On observing Figure 4.8, the peaks are at a duty of 0.27, 0.26, 0.24, and 0.24, respectively. Comparing it with Figure 4.9, the settling duty was found to be 0.24.

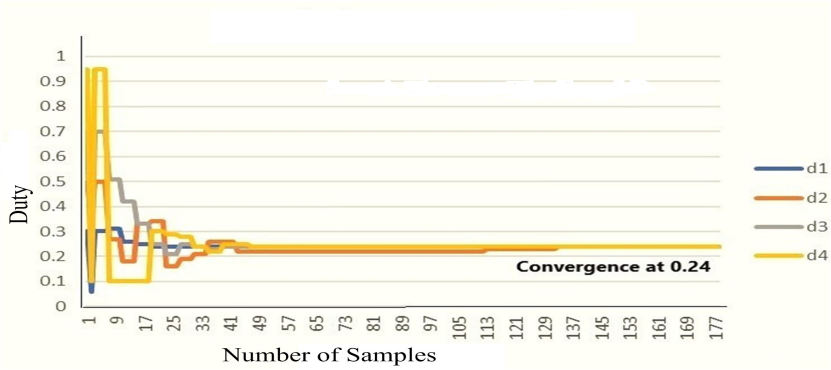


Figure 4.9: Convergence of the search elements (Unshaded)

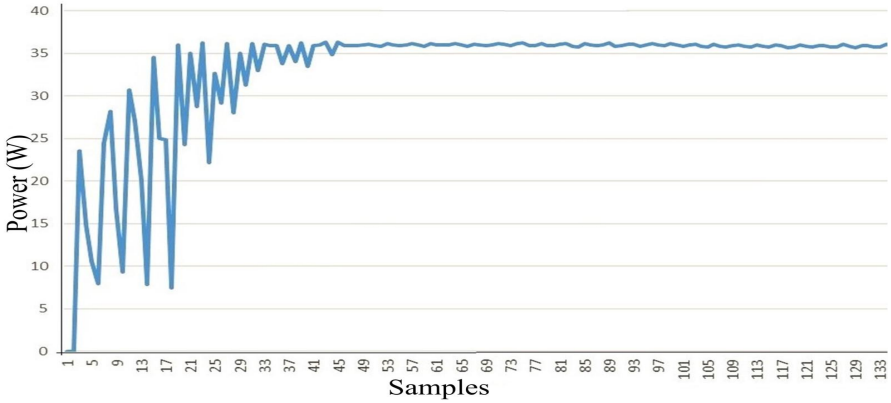


Figure 4.10: Settling of Power at MPP (Unshaded Condition)

Thus the value is almost close to the trials obtained, and thus, the functionality of MPPT is verified as in Figure 4.10 .

4.5.2 Global Peak Detection (Partial Shading)

The panels were shaded using a cardboard sheet partially, and a test was carried out, and the data was recorded. The bypass diodes play a major role in partially shaded conditions by removing the possibility of damage of panels due to local hot spots, and hence the efficiency of the MPPT device is retained. Bypass diodes are used to avoid hot-spot.At constant load connected to buck converter output terminal, the duty is varied from 0.1 to 1. The power that the panel gives is stored and later plotted,

and the process is repeated 3 to 4 times to ensure the accuracy of the data. Now immediately, the PSO algorithm is deployed to the microcontroller, the algorithm will converge at a point, and the value is compared with the duty value obtained at MPP of step 1. The values were almost equal (there may be slight variation in irradiation in this, but it was approximately the same), and thus, the global maximum peak detection functionality was verified.

The results of convergence and settling of power during partially shaded conditions are presented in Figure 4.11 and Figure 4.12. On observing Figure 4.13, Local peaks and Global Peaks are at (0.27,0.48), (0.26,0.5), and (0.27,0.48), respectively. The settling duty was found to be 0.48 at the global peak eliminating the peak close to 0.27. Thus the value is almost close to the trials conducted, and thus, the global peak detection of MPPT is verified. There may be slight variation in irradiation, and that is why trials are not exactly the same, but ideally, under constant irradiation and temperature, the MPP will be the same in all trials.

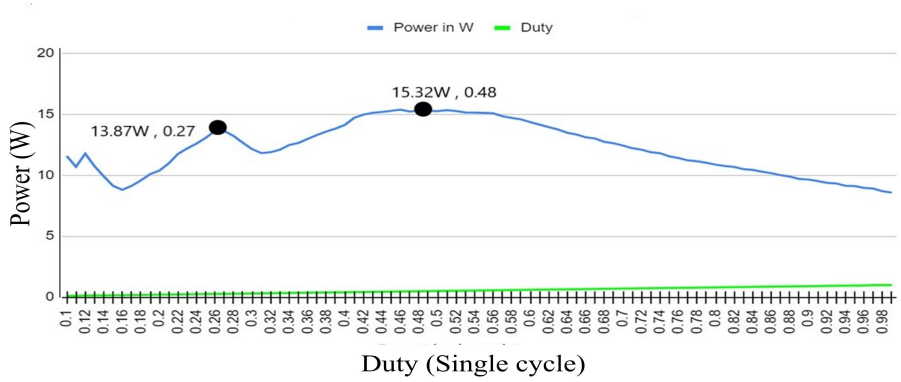


Figure 4.11: Detailed View of Local and Global Maxima (Partial shading).

4.5.3 Normal Operation to Sudden Shading

First, the panels are kept under the clear sky, and the algorithm searches for the MPP, and the searching elements converge at a point. Now the panel is covered partially using a cardboard sheet. Observations show that there will be a drastic power decrease as the previously converged duty may not be the actual MPP under shaded condition. Therefore, the algorithm detects this change and re-initializes and

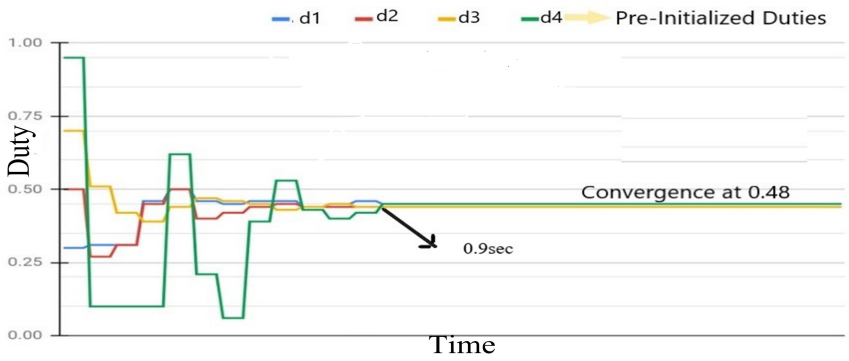


Figure 4.12: Convergence of the search elements(Partial shading)

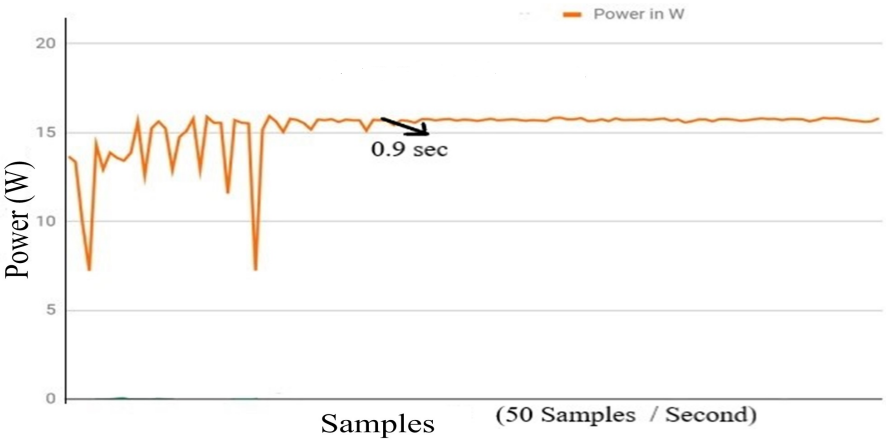


Figure 4.13: Settling of Power at MPP condition(Partial shading)

again converges at the optimum duty respectively as in Figure 4.14. From the Figure 4.15 we can see the new maximum power under shaded condition . If it is seen clearly at the shading instant the power dropped to 2W but the algorithm immediately found the new point and thus ensured the maximum power output even under harsh conditions. The developed prototype is compact and portable and is represented in Figure 4.16.

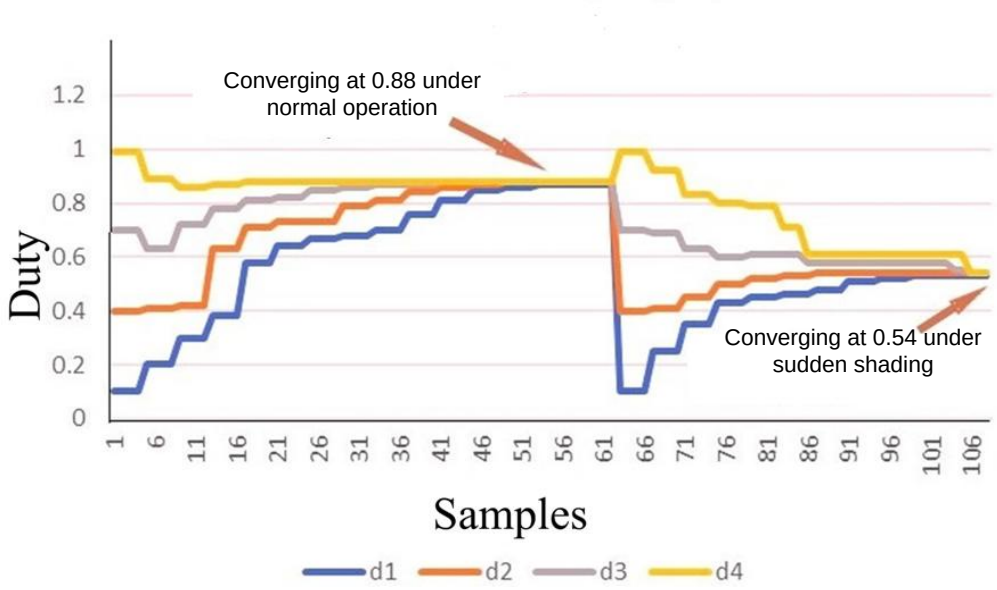


Figure 4.14: Normal operation to sudden shading transition of new optimal duty

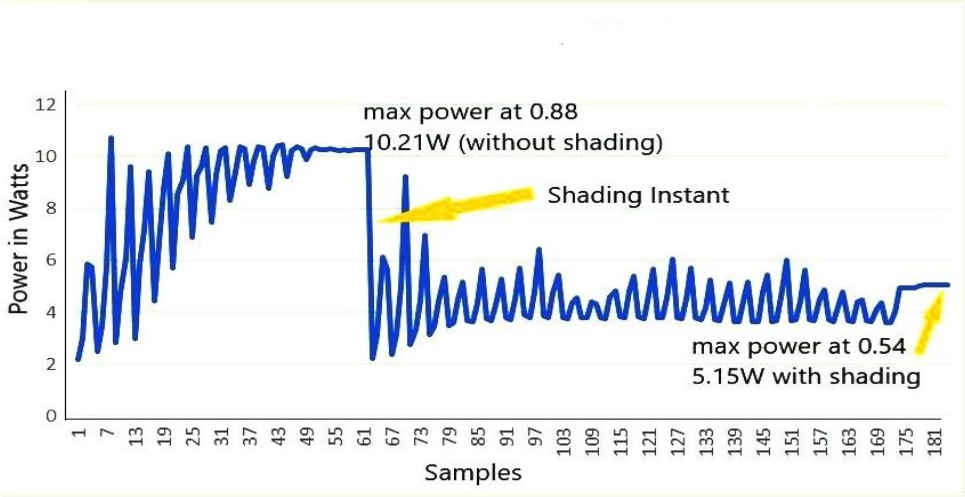


Figure 4.15: Maximum power during shaded and unshaded conditions with new optimal duty

4.6 Summary

The developed prototype was capable of detecting the global maxima, when the surrounding environmental parameter changes. The convergence was observed to be fast and accurate to the point of detecting the MPP. The reconvergence to the new

operating point when the irradiance changes due to passing clouds or other environmental conditions makes it highly efficient. This dynamic recovergence will ensure that continuous maximum available power is extracted from the panels at all the time. Apart from the speed and accuracy, the device is highly compact which is less than 200 gm in weight, and the cost is approximately ₹ 1000. Hence the device is economical, portable and also reliable as fewer specific components were used for the hardware construction which results in easy maintenance. Due to the above supporting features like optimum weight and compactness, the device can find a wide range of applications like Unmanned Aerial Vehicles, and also in devices which need to be operated continuously under varying environmental conditions. The limitation of the algorithm is the oscillations, due to the duty cycle struck in local maxima. Further work is required in this direction to overcome these shortcomings.

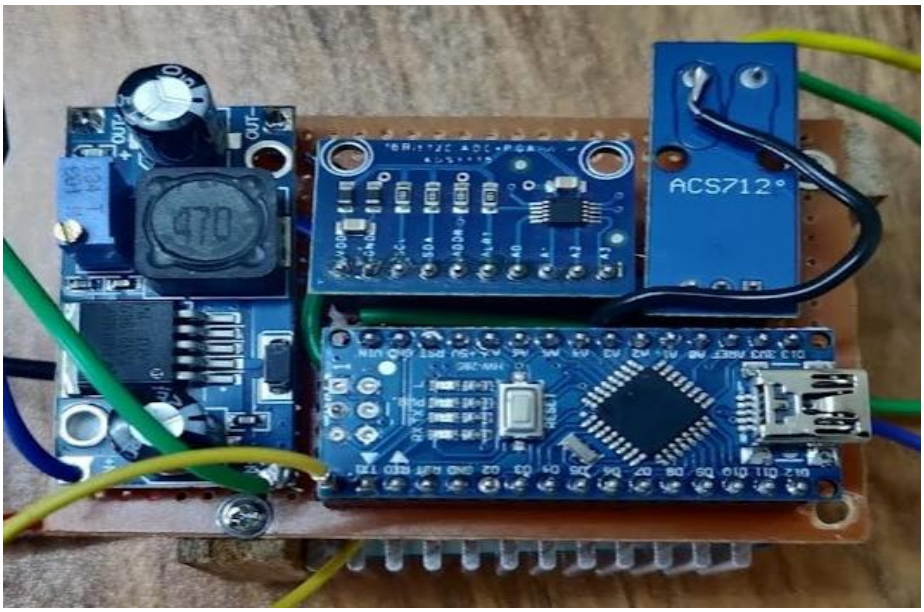


Figure 4.16: Hardware prototype of the developed buck converter

Chapter 5

Conclusions and Future Scope

Contents

5.1 Conclusion

The main conclusive remarks, and the future works of this thesis are presented. The following are the major findings of the thesis:

- NREL has made a detailed repository of temperature, irradiance, pressure, etc. data which can be used for the designing of the PV systems. Data for the irradiance for the city Mangalore was downloaded from NREL, NSRDB data viewer and 3 years' data 2012-14 was collected analyzed. From the MATLAB models, NREL 2014 details, Waaree panel of 200 W was selected for further studies. By varying temperature, the characteristics of $V_{MPP}, I_{MPP}, \& P_{MPP}$ were evaluated.

- Charging characteristics of 48 V lithium ion battery are studied. Study into the nature of battery charge characteristics reveal that the battery terminal voltage when deeply discharged is around 48 V. This voltage rises to 54.5 V when the charger is cutoff for safety as lithium ion battery cannot tolerate over voltages. The observations show that there is a linear relationship between the duty cycle

variation and the output voltage, and a higher voltage gain is achieved by the reconfigured modified boost topology and in agreement with simulation results carried out using MATLAB software.

- A modified power factor corrected quadratic buck converter is proposed and described in this chapter. The prototype of 150 W was rigged up in the laboratory and tested. The different operating modes of the operation of the converter are discussed and presented. The proposed converter has the benefit of single switch operation and reduced component counts comparable with the existing literature. The presented topology offers an improved power factor of over 0.89 at 110 V and 0.95 at 230 V. The study of variation of the output with variation in load, duty cycle and source were carried out experimentally, and the results are presented. The efficiency of the converter was observed to be over 80%. The proposed converter is suitable for 24 V - 48 V *dc* applications such as small motors and UPS/ battery charging applications. It provides a high step-down voltage ratio and inherent power factor correction without the requiring closed-loop control and complex sensor control.
- PSO algorithm was designed and implemented with faster convergence during partial shading conditions using simple buck converter.

5.2 Future Scope

Based on the research carried out in this report, the recommendations for the future research are presented.

- Exploring close loop control with emphasis on stress reduction on switch, comparative evaluation with continuous current mode for inductor and investigation for higher power applications for AC-DC converters.
- Implementation and evaluation of MPP algorithms for closed loop control in high gain DC-DC converter topology. The limtation of PSO has been the oscillations due to the duty cycle struck at local maxima. Further work is required to minimize the oscillations.
- Conventionally wireless charging is explored for fast charging and higher power loads. For such systems, there is mainly an inherent AC-DC conversion and high

frequency operation of above 18 MHz to reduce component sizes was presented in available literature. Further, for low power operations, such exploration is not much reported. Hence, wireless charging schemes can be explored.

Bibliography

Al-Saffar, M. A., Ismail, E. H., and Sabzali, A. J. (2009). Integrated buck–boost–quadratic buck pfc rectifier for universal input applications. *IEEE transactions on power electronics*, 24(12):2886–2896.

Alajmi, B. N., Ahmed, K. H., Finney, S. J., and Williams, B. W. (2010). Fuzzy-logic-control approach of a modified hill-climbing method for maximum power point in microgrid standalone photovoltaic system. *IEEE transactions on power electronics*, 26(4):1022–1030.

Altas, I. and Sharaf, A. (2008). A novel maximum power fuzzy logic controller for photovoltaic solar energy systems. *Renewable Energy*, 33(3):388–399.

Axelrod, B., Berkovich, Y., and Ioinovici, A. (2008). Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc–dc pwm converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55(2):687–696.

Brunton, S. L., Rowley, C. W., Kulkarni, S. R., and Clarkson, C. (2010). Maximum power point tracking for photovoltaic optimization using ripple-based extremum seeking control. *IEEE transactions on power electronics*, 25(10):2531–2540.

Chang, C.-H., Cheng, C.-A., Chang, E.-C., Cheng, H.-L., and Yang, B.-E. (2015). An integrated high-power-factor converter with zvs transition. *IEEE Transactions on power electronics*, 31(3):2362–2371.

Chavoshipour Heris, P., Saadatizadeh, Z., and Rostami, N. (2019). Transformerless quadratic-based high step-down dc–dc converter with wide duty cycle range. *IET Power Electronics*, 12(3):368–382.

Chuang, C.-F., Pan, C.-T., and Cheng, H.-C. (2015). A novel transformer-less interleaved four-phase step-down dc converter with low switch voltage stress and

automatic uniform current-sharing characteristics. *IEEE Transactions on Power Electronics*, 31(1):406–417.

Dutta, S., Debnath, D., and Chatterjee, K. (2017). A grid-connected single-phase transformerless inverter controlling two solar pv arrays operating under different atmospheric conditions. *IEEE Transactions on Industrial Electronics*, 65(1):374–385.

Einhorn, M., Conte, F. V., Kral, C., and Fleig, J. (2012). Comparison, selection, and parameterization of electrical battery models for automotive applications. *IEEE Transactions on Power Electronics*, 28(3):1429–1437.

Esram, T. and Chapman, P. L. (2007). Comparison of photovoltaic array maximum power point tracking techniques. *IEEE Transactions on energy conversion*, 22(2):439–449.

Esteki, M., Poorali, B., Adib, E., and Farzanehfard, H. (2015). Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses, and improved step-down conversion ratio. *IEEE transactions on industrial electronics*, 62(8):4769–4776.

Fardoun, A. A., Ismail, E. H., Khraim, N. M., Sabzali, A. J., and Al-Saffar, M. A. (2014). Bridgeless high-power-factor buck-converter operating in discontinuous capacitor voltage mode. *IEEE Transactions on Industry Applications*, 50(5):3457–3467.

Femia, N., Petrone, G., Spagnuolo, G., and Vitelli, M. (2005). Optimization of perturb and observe maximum power point tracking method. *IEEE transactions on power electronics*, 20(4):963–973.

Grigore, V. and Kyyra, J. (2000). High power factor rectifier based on buck converter operating in discontinuous capacitor voltage mode. *IEEE Transactions on Power Electronics*, 15(6):1241–1249.

Huber, L., Jang, Y., and Jovanovic, M. M. (2008). Performance evaluation of bridgeless pfc boost rectifiers. *IEEE transactions on power electronics*, 23(3):1381–1390.

Koad, R. B., Zobaa, A. F., and El-Shahat, A. (2016). A novel mppt algorithm based on particle swarm optimization for photovoltaic systems. *IEEE Transactions on Sustainable Energy*, 8(2):468–476.

Kumar, M., Singh, K. A., Chaudhary, K., Saket, R., Khan, B., et al. (2022). Regenerative braking in electric vehicle using quadratic gain bidirectional converter. *International Transactions on Electrical Energy Systems*, 2022.

Kushwaha, R. and Singh, B. (2019a). A modified bridgeless cuk converter based ev charger with improved power quality. In *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6. IEEE.

Kushwaha, R. and Singh, B. (2019b). A power quality improved ev charger with bridgeless cuk converter. *IEEE Transactions on Industry Applications*, 55(5):5190–5203.

Kwon, M., Oh, S., and Choi, S. (2013). High gain soft-switching bidirectional dc–dc converter for eco-friendly vehicles. *IEEE Transactions on Power Electronics*, 29(4):1659–1666.

Lam, L., Bauer, P., and Kelder, E. (2011). A practical circuit-based model for li-ion battery cells in electric vehicle applications. In *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, pages 1–9. IEEE.

Lee, I.-O., Cho, S.-Y., and Moon, G.-W. (2012). Interleaved buck converter having low switching losses and improved step-down conversion ratio. *IEEE transactions on power electronics*, 27(8):3664–3675.

Lee, Y.-J., Khaligh, A., and Emadi, A. (2009). Advanced integrated bidirectional ac/dc and dc/dc converter for plug-in hybrid electric vehicles. *IEEE Transactions on vehicular technology*, 58(8):3970–3980.

Loera-Palomo, R., Morales-Saldaña, J. A., and Palacios-Hernández, E. (2013). Quadratic step-down dc–dc converters based on reduced redundant power processing approach. *IET Power Electronics*, 6(1):136–145.

Lukic, S. M. and Emadi, A. (2008). Charging ahead. *IEEE Industrial Electronics Magazine*, 2(4):22–31.

Luo, X. and Chan, K. W. (2014). Real-time scheduling of electric vehicles charging in low-voltage residential distribution systems to minimise power losses and improve voltage profile. *IET generation, transmission & distribution*, 8(3):516–529.

Maksimovic, D. and Cuk, S. (1991). Switching converters with wide dc conversion range. *IEEE Transactions on Power Electronics*, 6(1):151–157.

Masoum, M. A., Moses, P. S., and Hajforoosh, S. (2012). Distribution transformer stress in smart grid with coordinated charging of plug-in electric vehicles. In *2012 IEEE PES Innovative Smart Grid Technologies (ISGT)*, pages 1–8. IEEE.

Mishima, T., Masuda, S., and Nakaoka, M. (2014). A zcs-pwm bidirectional dc-dc converter with a two-terminal resonant tank-based auxiliary switching cell. In *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 4043–4050. IEEE.

Mok, K., Lai, Y., and Loo, K. H. (2011). A single-stage bridgeless power-factor-correction rectifier based on flyback topology. In *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, pages 1–6. IEEE.

Morales-Saldana, J. A., Leyva-Ramos, J., Carbajal-Gutierrez, E. E., and Ortiz-Lopez, M. G. (2008). Average current-mode control scheme for a quadratic buck converter with a single switch. *IEEE transactions on power electronics*, 23(1):485–490.

MRTH (2022). Electric vehicles and charging stations. `https://www.pib.gov.in/PressReleasePage.aspx?PRID=1811830`. 2022.

NEMMP (2013). National electric mobility mission plan 2020. `https://emobility.araiindia.com/wp-content/uploads/2018/06/NEMMP2020.pdf`. 2013.

Nguyen, X. H. and Nguyen, M. P. (2015). Mathematical modeling of photovoltaic cell/module/arrays with tags in matlab/simulink. *Environmental Systems Research*, 4:1–13.

Obukhov, S., Ibrahim, A., Diab, A. A. Z., Al-Sumaiti, A. S., and Aboelsaud, R. (2020). Optimal performance of dynamic particle swarm optimization based maximum power trackers for stand-alone pv system under partial shading conditions. *IEEE Access*, 8:20770–20785.

Pacheco, V. M., Do Nascimento, A., Farias, V. J., Vieira, J. B., and de Freitas, L. C. (2000). A quadratic buck converter with lossless commutation. *IEEE Transactions on Industrial Electronics*, 47(2):264–272.

Pan, C.-T., Chuang, C.-F., and Chu, C.-C. (2014). A novel transformerless interleaved high step-down conversion ratio dc–dc converter with low switch voltage stress. *IEEE transactions on industrial electronics*, 61(10):5290–5299.

Park, S. and Choi, S. (2009). Soft-switched ccm boost converter with high voltage gain for high power applications. In *2009 IEEE Energy Conversion Congress and Exposition*, pages 1999–2006. IEEE.

Pires, V. F., Foito, D., and Cordeiro, A. (2017). A dc–dc converter with quadratic gain and bidirectional capability for batteries/supercapacitors. *IEEE Transactions on Industry Applications*, 54(1):274–285.

Prabhu, P. and Urundady, V. (2020). Design of coupled inductors using split winding scheme for bridgeless sepic. *IET Power Electronics*, 13(7):1434–1444.

Prasanna, U. R., Singh, A. K., and Rajashekara, K. (2017). Novel bidirectional single-phase single-stage isolated ac–dc converter with pfc for charging of electric vehicles. *IEEE Transactions on Transportation Electrification*, 3(3):536–544.

Prudente, M., Pfitscher, L., and Gules, R. (2005). A boost converter with voltage multiplier cells. In *2005 IEEE 36th Power Electronics Specialists Conference*, pages 2716–2721. IEEE.

Prudente, M., Pfitscher, L. L., Emmendoerfer, G., Romaneli, E. F., and Gules, R. (2008). Voltage multiplier cells applied to non-isolated dc–dc converters. *IEEE Transactions on Power Electronics*, 23(2):871–887.

Revathi, B. S. and Prabhakar, M. (2016). Non isolated high gain dc-dc converter topologies for pv applications–a comprehensive review. *Renewable and Sustainable Energy Reviews*, 66:920–933.

Reyes-Malanche, J. A., Vázquez, N., and Leyva-Ramos, J. (2015). Switched-capacitor quadratic buck converter for wider conversion ratios. *IET Power Electronics*, 8(12):2370–2376.

Rezk, H., Fathy, A., and Abdelaziz, A. Y. (2017). A comparison of different global mppt techniques based on meta-heuristic algorithms for photovoltaic system subjected to partial shading conditions. *Renewable and Sustainable Energy Reviews*, 74:377–386.

Safari, A. and Mekhilef, S. (2010). Simulation and hardware implementation of incremental conductance mppt with direct control method using cuk converter. *IEEE transactions on industrial electronics*, 58(4):1154–1161.

Sahoo, M. and Kumar, K. S. (2014). High gain step up dc-dc converter for dc microgrid application. In *7th international conference on information and automation for sustainability*, pages 1–5. IEEE.

Sangrody, R., Taheri, S., Cretu, A.-M., and Pouresmaeil, E. (2024). An improved pso-based mppt technique using stability and steady state analyses under partial shading conditions. *IEEE Transactions on Sustainable Energy*, 15(1):136–145.

Shreelakshmi, M., Das, M., and Agarwal, V. (2018). Design and development of a novel high voltage gain, high-efficiency bidirectional dc–dc converter for storage interface. *IEEE transactions on industrial electronics*, 66(6):4490–4501.

Singh, B., Singh, B. N., Chandra, A., Al-Haddad, K., Pandey, A., and Kothari, D. P. (2003). A review of single-phase improved power quality ac-dc converters. *IEEE Transactions on industrial electronics*, 50(5):962–981.

Sun, X., Wu, X., Shen, Y., Li, X., and Lu, Z. (2016). A current-fed isolated bidirectional dc–dc converter. *IEEE Transactions on Power Electronics*, 32(9):6882–6895.

Tse, C. K. and Chow, M. (1998). A theoretical examination of the circuit requirements of power factor correction. In *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No. 98CH36196)*, volume 2, pages 1415–1421. IEEE.

Veerachary, M. (2016). Two-switch semiquadratic buck converter. *IEEE Transactions on Industrial Electronics*, 64(2):1185–1194.

Villalva, M. G., Gazoli, J. R., and Ruppert Filho, E. (2009). Comprehensive approach to modeling and simulation of photovoltaic arrays. *IEEE Transactions on power electronics*, 24(5):1198–1208.

Wai, R.-J., Duan, R.-Y., and Jheng, K.-H. (2012). High-efficiency bidirectional dc–dc converter with high-voltage gain. *IET Power Electronics*, 5(2):173–184.

Wang, X. and Stuart, T. (2002). Charge measurement circuit for electric vehicle batteries. *IEEE Transactions on Aerospace and Electronic Systems*, 38(4):1201–1209.

Wu, H., Sun, K., Chen, L., Zhu, L., and Xing, Y. (2016a). High step-up/step-down soft-switching bidirectional dc–dc converter with coupled-inductor and voltage matching control for energy storage systems. *IEEE Transactions on Industrial Electronics*, 63(5):2892–2903.

Wu, H., Sun, K., Chen, L., Zhu, L., and Xing, Y. (2016b). High step-up/step-down soft-switching bidirectional dc–dc converter with coupled-inductor and voltage matching control for energy storage systems. *IEEE Transactions on Industrial Electronics*, 63(5):2892–2903.

Wu, Y.-E. and Chen, I.-C. (2019). Novel integrated three-port bidirectional dc/dc converter for energy storage system. *IEEE Access*, 7:104601–104612.

Yang, J., Yu, D., Cheng, H., Zan, X., and Wen, H. (2017). Dual-coupled inductors-based high step-up dc/dc converter without input electrolytic capacitor for pv application. *IET Power Electronics*, 10(6):646–656.

Yao, J., Abramovitz, A., and Smedley, K. M. (2015). Steep-gain bidirectional converter with a regenerative snubber. *IEEE Transactions on Power Electronics*, 30(12):6845–6856.

Yilmaz, M. and Krein, P. T. (2012). Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. *IEEE transactions on Power Electronics*, 28(5):2151–2169.

Zhang, N., Sutanto, D., Muttaqi, K. M., Zhang, B., and Qiu, D. (2015). High-voltage-gain quadratic boost converter with voltage multiplier. *IET Power Electronics*, 8(12):2511–2519.

Zhang, S. S. (2006). The effect of the charging protocol on the cycle life of a li-ion battery. *Journal of power sources*, 161(2):1385–1391.

Zhao, B., Abramovitz, A., and Smedley, K. (2015). Family of bridgeless buck-boost pfc rectifiers. *IEEE Transactions on Power Electronics*, 30(12):6524–6527.

Publications

Papers published in refereed journals

1. Lalitha T.S. Annambhotla, P Parthiban,"Non isolated power factor corrected AC / DC converter with high step-down voltage ratio for low power applications", *International Transactions on Electrical Energy Systems, (Hindawi)*, vol. 2022, 2022 [SCIE].
   DOI:[10.1155/2022/7142957]

Papers published in refereed conference proceedings

1. Mahesh P, Lalitha T.S. Annambhotla, P Parthiban,"Hardware Prototype for Portable Automatic MPPT Solar Charger Using Buck Converter and PSO Technique " *IEEE Delhi Section International Conference on Electrical, Electronics and Computer Engineering (DELCON-2022)*, IEEE, 2022. DOI:[10.1109/DELCON54057.2022.9764362].

2. Lalitha Darbha, Parthiban P,"High Gain Modified Boost Converter for Electric Vehicle Battery Charging " 1^{st} *IEEE International Conference on Energy, Systems and Information Processing (ICESIP-2019)*, Kanchipuram, IEEE, 2019. DOI:[10.1109/ICESIP46348.2019.8938258].

3. Lalitha Darbha, Parthiban P, "High Gain Bidirectional DC-DC Converter with Reduced Component Count " 8^{th} *National Power Electronics Conference (NPEC-2017)*, IEEE, 2017. DOI:[10.1109/NPEC.2017.8310477].

Bio-data

Name : A.O. L Tripura Sundari
Date of birth: 01-05-1977
Marital status: Married
E-mail: lalithadarbha@gmail.com
Mobile: +91-8277445794

Address
Research Scholar (External Registration),
Department of Electrical & Electronics Engineering,
National Institute of Tehnology Karnataka,
Surathkal, Mangalore, India -575025
&
Assistant Professor
Department of Electrical & Electronics Engineering
S.G.Balekundri Institute of Tehnology
Belagavi, Karnataka, India-590010, India.

Education

- **M.Tech.**, Power Electronics , JNTUH College of Engineering, Hyderabad, TS, Aggregate-72%, 2010.
- **B.Tech.**, Electrical & Electronics Engineering, G. Pulla Reddy College of Engineering (GPREC), Kurnool, A.P, Aggregate-72%, 1998.
- **Intermediate**, Board of Intermediate Education, Maharshi Veda Vigyan Mahavidyalaya , Begumpet, Hyderabad, T.S., Aggregate-85%, 1994.
- **SSC**, Board of Secondary Education, Wesley Girls High School, Secunderabad, T.S., Aggregate-85%, 1992.